Hi3521/Hi3520A H.264 CODEC Processor

Data Sheet

Issue 09

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Contents

About This Document.....1

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About This Document

Purpose

This document describes the features, logical structures, functions, operating modes, and related registers of each module of the Hi3521. This document also describes the interface timings and related parameter in diagrams. In addition, this document details the pins, pin usages, performance parameters, and package of the Hi3521.

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3521	V100
Hi3520A	V100

Intended Audience

This document is intended for:

- Design and maintenance personnel for electronics
- Sales personnel for electronic components

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

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Symbol	Description
	Indicates a hazard with a high level of risk which, if not avoided, will result in death or serious injury.
	Indicates a hazard with a medium or low level of risk that, if not avoided, could result in minor or moderate injury.
	Indicates a potentially hazardous situation, which if not avoided, could result in equipment damage, data loss, performance degradation, or unexpected results.
	Indicates a tip that may help you solve a problem or save time.
	Provides additional information to emphasize or supplement important points of the main text.

General Conventions

The general conventions that may be found in this document are defined as follows.

Convention	Description
Times New Roman	Normal paragraphs are in Times New Roman.
Boldface	Names of files, directories, folders, and users are in **boldface**. For example, log in as user **root**.
Italic	Book titles are in *italics*.
`Courier New`	Examples of information displayed on the screen are in `Courier New`.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Content	Description
–	The cell is blank.
*	The content in this cell is configurable.

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Notes

Register Attributes

The register attributes that may be found in this document are defined as follows.

Symbol	Description	Symbol	Description
RO	The register is read-only.	RW	The register is read/write.
RC	The register is cleared on a read.	WC	The register can be read. The register is cleared when 1 is written. The register keeps unchanged when 0 is written.

Reset Value Conventions

In the register definition tables:

- If the reset value (for the Reset row) of a bit is "?", the reset value is undefined.
- If the reset values of one or multiple bits are "?", the total reset value of a register is undefined and is marked as "-".

Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity (such as the RAM capacity)	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0xFE04, 0x18	Address or data in hexadecimal
0b	0b000, 0b00 00000000	Data or sequence in binary (register description is excluded.)

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Symbol	Example	Description
X	00X, 1XX	In data expression, X indicates 0 or 1. For example, 00X indicates 000 or 001 and 1XX indicates 100, 101, 110, or 111.

Others

All frequencies in this document all comply with the SDH standard. The shortened frequency names and the corresponding nominal frequencies are as follows.

Shortened Frequency Name	Nominal Frequency
19 M	19.44 MHz
38 M	38.88 MHz
77 M	77.76 MHz
622 M	622.08 MHz

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 09 (2015-02-09)

Chapter 14 Peripherals

In section 14.1.5, I2C_SCL_L and I2C_SCL_H registers are modified.

Issue 08 (2014-09-21)

Chapter 2 Hardware

In section 2.1.1, package views are updated.

In section 2.8.2.3, Figure 2-17 and Figure 2-18 are modified.

Chapter 5 TOE

In section 5.5, the offset address for GMACN_MMC_RX1024TOMAXOCTETS_GB is changed.

Chapter 11 Video Interfaces

In section 11.1.3.2, Figure 11-6 is updated.

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Issue 07 (2014-05-09)

Chapter 2 Hardware

In section 2.8.4, Table 2-101 is modified.

Chapter 12 VOIE

In section 12.5, the VOIE_CFG register is added.

Issue 06 (2013-11-18)

This issue is the sixth official release, which incorporates the following changes:

Chapter 2 Hardware

In section 2.4.4, Figure 2-30 and Figure 2-32 are modified.

Chapter 5 TOE

In section 5.4.1, Figure 5-2 and Figure 5-4 are modified.

Issue 05 (2013-08-31)

This issue is the fifth official release, which incorporates the following changes:

Chapter 11 Video Interfaces

In Figure 11-1, HC0/1 is changed to HC0.

In section 11.2.2, the number of supported cursor layers is changed to 1. That is, only HC0 is supported.

Issue 04 (2013-04-28)

This issue is the fourth official release, which incorporates the following changes:

Chapter 1 Product Description

In section 1.2.13, the maximum CS capacity supported by the SPI NOR flash is changed.

Issue 03 (2013-01-10)

This issue is the third official release, which incorporates the following changes:

Chapter 11Video Interfaces

In section 11.1.3.2, the descriptions of the DC interface timings are updated.

Issue 02 (2012-11-30)

This issue is the second official release, which incorporates the following changes:

Chapter 1 Product Description

In section 1.2.8, the digital watermark is deleted.

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Chapter 2 Hardware

In the new section 2.2, descriptions of shutting down power supplies to the eFUSE pin are added.

In section 2.6, parameters of the temperature and thermal resistance are supplemented.

Chapter 4 Memory Interface

In section 4.1.2, the first feature is modified.

In section 4.1.4.3, step 11 and its notes are modified.

In section 4.1.4.4, step 13 and its notes are modified.

Descriptions of the registers DDRC_EMRS01 and DDRC_EMRS23 are updated.

In sections 4.3.5 and 4.3.6, contents are updated.

Chapter 11 Video Interface

In section 11.1.3.2, descriptions of the NTSC and PAL in the horizontal and vertical timings of ITU-R BT.601 YCbCr4:2:2 are updated.

Chapter 14 Peripherals

The reset value for SATA_PHY0_CTLH is modified, and bit[3:2] are reserved.

Issue 01 (2012-08-30)

This issue is the first official release, which incorporates the following changes:

Chapter 10 Intelligent Video Engine

In section 10.3.4.1, the following are added:

- Formula for calculating the 3x3 dilate operator shown in Figure 10-17
- Formula for calculating the 3x3 erode operator shown in Figure 10-18
- Thresh operation formulas
- AND operation formula
- OR operation formula
- Integral operation formula
- Histogram operation formula

Appendix 02-B Order Notice

This chapter is added.

Issue 00B10 (2012-06-30)

This issue is the fifth draft release, which incorporates the following changes:

Chapter 2 Hardware

In Table 2-14 and Table 2-80, the meaning of value 11 is changed to "reserved" for function 1 indicating the boot mode.

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Chapter 3 System

In section 3.2.5, the description of PERI_CRG16 bit[10] is changed to "reserved".

In section 3.4.5, the meaning of value 11 is changed to "reserved" for SYSSTAT bit[5:4].

Chapter 11 Video Interfaces

In section 11.2.3.5, the protocol that the HDMI complies with is added, and

In section 11.2.5, ACC lookup table registers for multiple luminance levels are added.

In section 11.2.6, the description "this field must be set to 0" is added to WBC2VSP bit[25].

Chapter 14 Peripherals

In section 14.8.5.4, the registers values in Step 4 and Step 8 are changed in the procedure for initializing the SATA PHY.

Issue 00B04 (2012-06-08)

This issue is the fourth draft release, which incorporates the following changes:

Chapter 1 Introduction

In Table 1-1, the function of the address space ranging from 0x0000_0000 to 0x03FF_FFFF is changed.

Chapter 2 Hardware

In Table 2-14 and Table 2-80, the meaning of value 11 is changed to "reserved" for function 1 indicating the boot mode.

Chapter 3 System

The value for PERI_CRG16 bit[10] is changed to reserved.

The boot mode corresponding to the value 11 for SYSSTAT bit[5:4] is changed to reserved.

Issue 00B03 (2012-04-20)

This issue is the third draft release, which incorporates the following changes:

Chapter 3 System

This chapter is added.

Chapter 4 Memory Interfaces

This chapter is added.

Chapter 6 Video Decoder

This chapter is added.

Chapter 7 Video Encoder

This chapter is added.

Chapter 8 Video and Graphics Processing

This chapter is added.

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Chapter 9 Motion Detect Unit

This chapter is added.

Chapter 10 Intelligent Video Engine

This chapter is added.

Chapter 11 Video interfaces

This chapter is added.

Chapter 12 VOIE

This chapter is added.

Chapter 13 Audio Interfaces

This chapter is added.

Chapter 14 Peripherals

This chapter is added.

Issue 00B02 (2012-03-29)

This issue is the second draft release, which incorporates the following changes:

Chapter 1 Introduction

The descriptions are updated.

Chapter 2 Hardware

The descriptions are updated.

Issue 00B01 (2012-03-20)

This issue is the draft release.

Only chapter 1 "Introduction" and chapter 2 "Hardware" are provided.

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Contents

1 Introduction.....1-1
1.1 Application Scenarios.....1-1
1.1.1 DVRs (Each with a Hi3521).....1-1
1.1.2 NVR with a Hi3521.....1-2
1.2 Architecture.....1-3
1.2.2 Processor Core.....1-4
1.2.3 Video Encoding and Decoding Protocols.....1-4
1.2.4 Video Encoding and Decoding.....1-5
1.2.5 Intelligent Video Analysis.....1-5
1.2.6 Video and Graphic Processing.....1-5
1.2.7 Audio Encoding and Decoding.....1-5
1.2.8 Security Engine.....1-5
1.2.9 Video Interfaces.....1-5
1.2.10 Audio Interfaces.....1-6
1.2.11 Ethernet Port.....1-6
1.2.12 Peripherals.....1-6
1.2.13 Memory Interfaces.....1-6
1.2.14 Boot Modes.....1-7
1.2.15 SDK.....1-7
1.2.16 Physical Specifications.....1-7
1.3 Boot Modes.....1-8
1.3.1 Booting from the BOOTROM.....1-8
1.3.2 Booting from the NAND Flash.....1-8
1.3.3 Booting from the SPI NOR Flash.....1-8
1.3.4 Address Space Mapping.....1-8

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Figures

Figure 1-1 DVR with a Hi3521 1-2
Figure 1-2 NVR with a Hi3521 1-3
Figure 1-3 Logic block diagram 1-4

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Tables

Table 1-1 Address space mapping 1-9

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1 Introduction

1.1 Application Scenarios

The Hi3521 is a professional high-end system-on-chip (SoC) designed for multi-channel D1 and high-definition (HD) digital video recorders (DVRs) and network video recorders (NVRs). With a high-performance A9 processor, a dedicated TCP/IP offload engine (TOE), and an engine supporting up to 8-channel D1 real-time encoding and decoding, the Hi3521 meets the rising demand for HD and network applications. The Hi3521 also provides an outstanding video engine, various encoding/decoding algorithms, and multi-channel HD output capability. These features guarantee users a high-quality image experience. In addition, the Hi3521 supports various highly-integrated peripheral interfaces to meet customer requirements for functionality, features, and image quality, while reducing the engineering bill of material (EBOM) cost. The Hi3521 is applicable to the following typical scenarios:

- DVRs (Each with a Hi3521)
- NVR with a Hi3521

1.1.1 DVRs (Each with a Hi3521)

- DVR for 8D1+8CIF encoding+4D1 decoding
  - 8D1+8CIF dual-stream real-time encoding+4D1 real-time decoding
  - HDMI+VGA 1080p@60 fps outputs from the same source+2-channel CVBS outputs
- DVR for 8x960H+8CIF encoding+1x960H decoding
  - 8x960H+8CIF encoding+1x960H real-time decoding
  - HDMI+VGA 1080p@60 fps outputs from the same source+2-channel CVBS outputs
- DVR for 16CIF encoding+16QCIF encoding+16CIF decoding
  - 16CIF +16QCIF dual-stream real-time encoding+16CIF real-time decoding
  - HDMI+VGA 1080p@60 fps outputs from the same source+2-channel CVBS outputs

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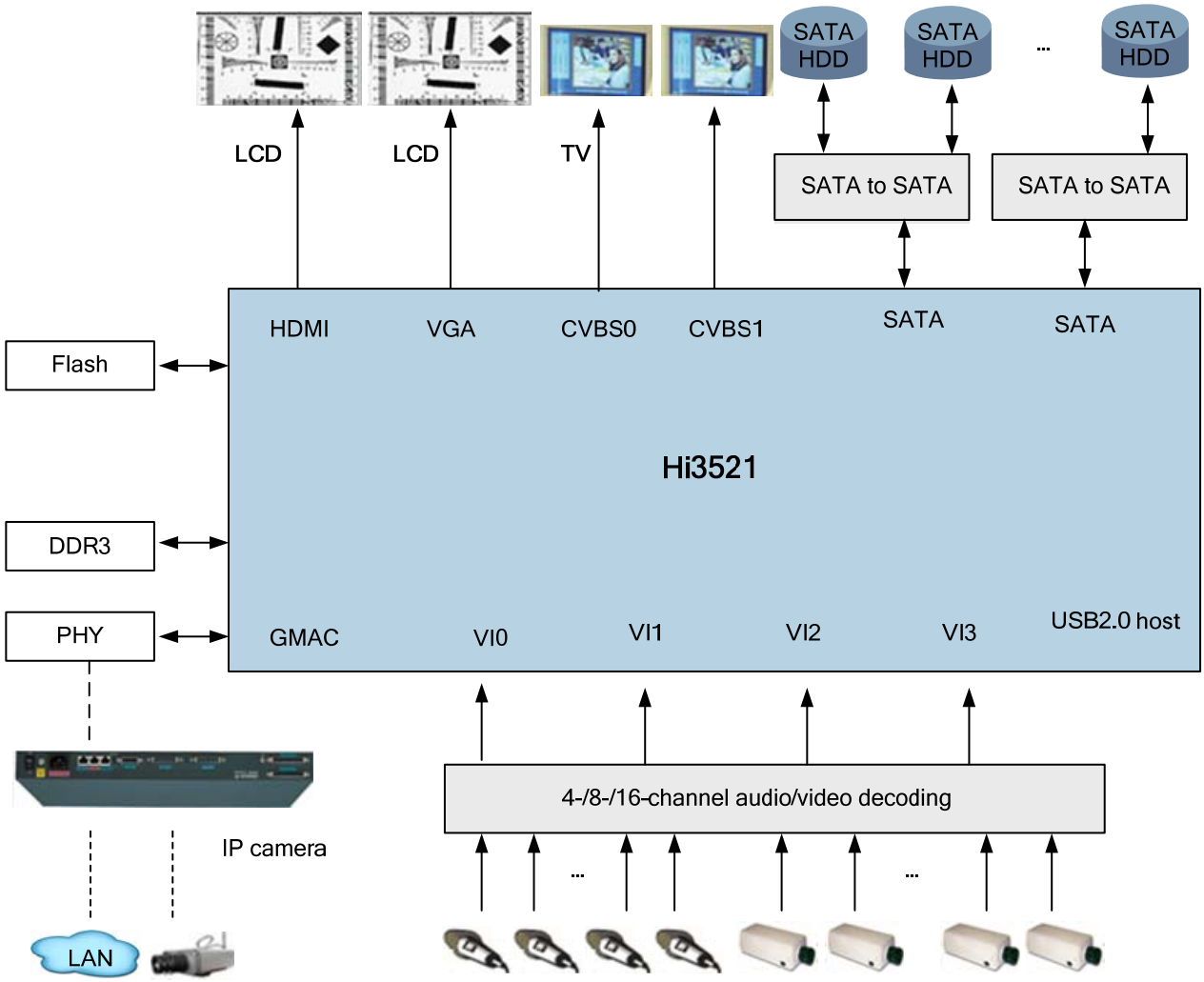
Figure 1-1 DVR with a Hi3521



1.1.2 NVR with a Hi3521

- 4x720p real-time decoding
  - 4x720p decoding
  - HDMI+VGA 1080p@60 fps outputs from the same source+2-channel CVBS outputs

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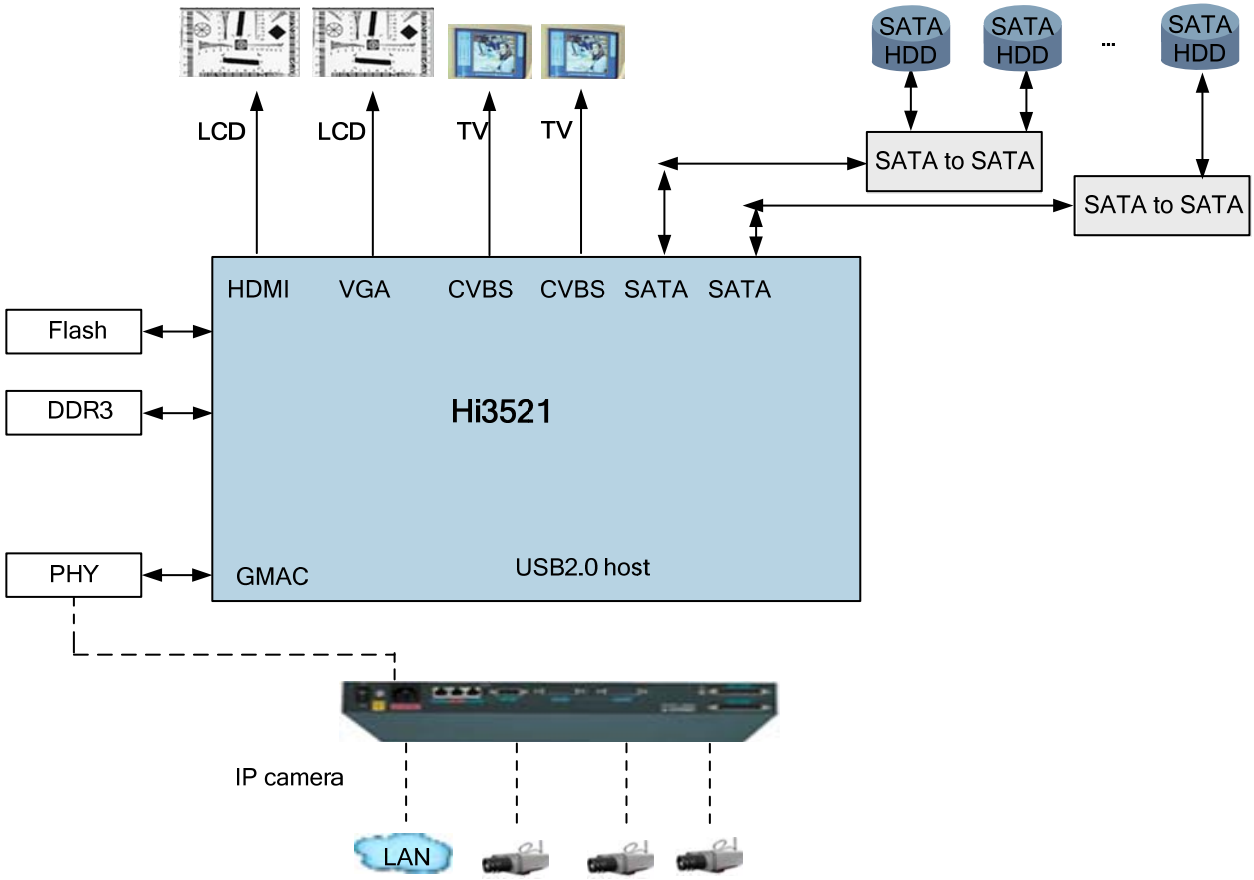
Figure 1-2 NVR with a Hi3521



1.2 Architecture

Figure 1-3 shows the logic block diagram.

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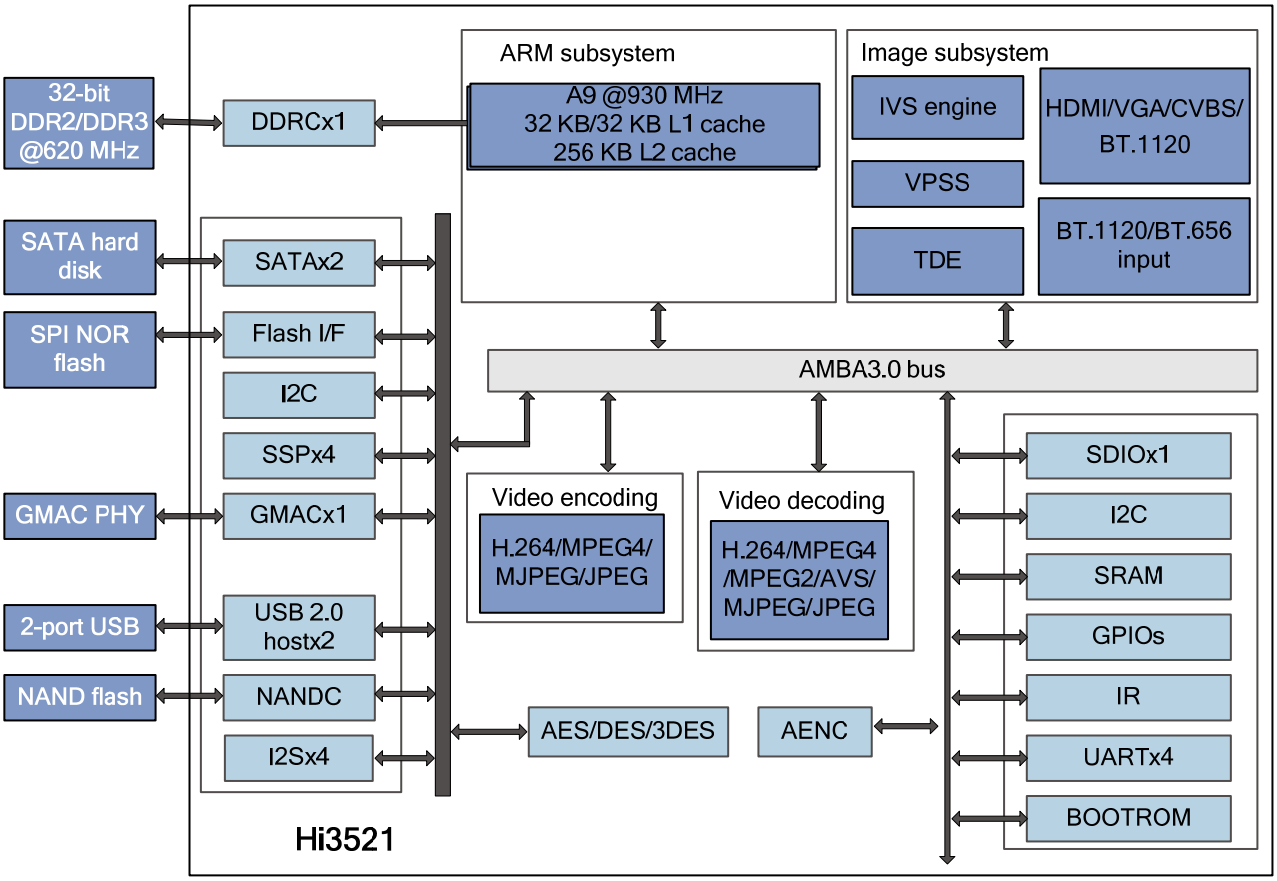
Figure 1-3 Logic block diagram



1.2.2 Processor Core

The Hi3521 uses the ARM Cortex A9 with the maximum frequency 930 MHz.

- 32 KB L1 instruction-cache (I-cache) and 32 KB L1 data-cache (D-cache)
- 256 KB L2 cache

1.2.3 Video Encoding and Decoding Protocols

- H.264 Baseline/Main Profile@Level 1–4.2 encoding
- H.264 High Profile@Level 4.2 decoding
- MPEG-4 SP@Level3,ASP@Level 5 decoding
- MJPEG/JPEG Baseline encoding and decoding
- Constant bit rate (CBR), variable bit rate (VBR), or average bit rate (ABR) ranging from 16 kbit/s to 40 Mbit/s
- Encoding frame rate ranging from 1 fps to 60 fps
- Region of interest (ROI) encoding
- Color-to-gray encoding

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1.2.4 Video Encoding and Decoding

H.264&JPEG encoding and decoding of multiple streams:

- 16CIF@30 fps+16QCIF@30 fps encoding+16CIF@30 fps decoding+JPEG snapshot D1@8 fps
- 1x720p@30 fps+VGA@30 fps encoding+7D1@30 fps+ 7CIF@30 fps encoding+1D1@30 fps decoding+JPEG snapshot@4 fps
- 8x960H@30 fps+8CIF@30 fps encoding+1x960H@30 fps decoding+ JPEG snapshot 960H@4 fps
- 8D1@30 fps+8CIF@30 fps encoding+4D1@30 fps decoding+JPEG snapshot D1@4 fps
- 1x720p@30 fps+VGA@30 fps encoding+4D1@30 fps+ 4CIF@30 fps encoding+4D1@30 fps decoding+JPEG snapshot@4 fps
- 4x960H@30 fps+4CIF@30 fps encoding+4x960H@30 fps decoding+ JPEG snapshot 960H@4 fps
- 4x720p real-time decoding

1.2.5 Intelligent Video Analysis

The Hi3521 has an integrated intelligent analysis acceleration engine that supports motion detection, boundary security, and video diagnosis.

1.2.6 Video and Graphic Processing

- Video pre- and post-processing, including de-interlacing, image enhancement, edge enhancement, and 3D denoising
- Anti-flicker for output videos and graphics
- 1/8x to 8x video scaling
- 1/2x to 2x graphic scaling
- On-screen display (OSD) overlay of eight regions before encoding
- Alpha blending of video layers and graphics layers

1.2.7 Audio Encoding and Decoding

- ADPCM, G.711, and G.726 hardware encoding
- Software decoding complying with various protocols

1.2.8 Security Engine

- Advanced encryption standard (AES), data encryption standard (DES), and triple data encryption standard (3DES) encryption and decryption

1.2.9 Video Interfaces

- Video input interfaces
  - 4xBT.656@108/144 MHz for 16CIF/8x960H real-time inputs
  - 2xBT.1120@148.5 MHz for 2x1080p real-time inputs
  - 4xBT.656@148.5 MHz for 4x720p real-time inputs
- Video output interfaces

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- HDMI 1.3+VGA+CVBSx2 outputs, The HDMI and VGA outputs can share the same source
- 1xLCD, 1xBT1120@148.5 MHz, or 1xBT656@27 MHz digital video output. The LCD and BT.1120 outputs share the same source. The BT.656 and CVBS outputs share the same source
- Maximum 1080p@60 fps for HDMI or VGA
- Three graphics layers in RGB1555 or RGB8888 format, with the maximum resolution of 1920x1080
- One hardware cursor layer in RGB1555 or RGB8888 format, with the maximum resolution of 128x128
- One independent video PIP layer

1.2.10 Audio Interfaces

The Hi3521 has four inter-IC sound (I^2S) interfaces. The details are as follows:

- Two for input
- One for input or output
- One for high-definition multimedia interface (HDMI) I^2S output

1.2.11 Ethernet Port

The Hi3521 has one gigabit media access controller (GMAC) port. The details are as follows:

- RGMII or MII mode
- 10/100 Mbit/s full-duplex or half-duplex mode
- 1000 Mbit/s full-duplex mode
- TOE for reducing the CPU usage

1.2.12 Peripherals

The Hi3521 has the following peripheral interfaces:

- Two serial advanced technology attachment 2.6 (SATA 2.6) interfaces
  - Port multiplier (PM)
  - external serial advanced technology attachment (eSATA)
- Four universal asynchronous receiver transmitter (UART) interfaces
- One serial peripheral interface (SPI), supporting four chip selects (CSs)
- One infrared (IR) interface, one inter-integrated circuit (I^2C) interface, and multiple general-purpose input/output (GPIO) interfaces
- One secure digital input/output 2.0 (SDIO 2.0) interface, supporting a maximum of 32 GB capacity
- Two universal serial bus 2.0 (USB 2.0) host ports, supporting hub

1.2.13 Memory Interfaces

The Hi3521 has the following memory interfaces:

- One 16- or 32-bit DDR2/DDR3 synchronous dynamic random access memory (SDRAM) controller interface

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  - Maximum frequency of 620 MHz
  - On-die termination (ODT)
  - Maximum capacity of 1 GB
  - Automatic power consumption control
- SPI NOR flash interfaces
  - 1-, 2-, or 4-bit SPI NOR flash interfaces
  - Two CSs
  - Maximum capacity of 8 Gbit for each CS
- NAND flash interfaces
  - 8-bit data width
  - Single-level cell (SLC) or multi-level cell (MLC)
  - 1-, 4-, or 24-bit error checking and correcting (ECC)
  - Built-in 2 KB BOOTROM and 10 KB SRAM

1.2.14 Boot Modes

- BOOTROM
- SPI NOR flash
- NAND flash

1.2.15 SDK

- Linux 3.0-based SDK
- High-performance H.264 PC decoding library

1.2.16 Physical Specifications

- Power consumption
  - 3.5 W typical power consumption
  - Multi-level power-saving control
- Operating voltage
  - 1.0 V core voltage
  - 3.3 or 2.5 V I/O voltage and 5 V margin voltage
  - 1.5 V or 1.8 V DDR2/DDR3 SDRAM interface voltage
  - Operating temperature ranging from 0°C (32°F) to 70°C (158°F)
- Package
  - Restriction of the use of certain hazardous substances (RoHS) EHS flip-chip ball grid array 449 (FCBGA449)
  - Ball pitch: 0.8 mm (0.031 in.) in the core power area or 0.65 mm (0.026 in.) in other areas
  - Body size: 19 mm x 19 mm (0.75 in. x 0.75 in.)

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1.3 Boot Modes

The Hi3521 can boot from:

- BOOTROM
- SPI NOR flash
- NAND flash

1.3.1 Booting from the BOOTROM

Before the Hi3521 boots from the on-chip BOOTROM, the level of BOOTROM_SEL (multiplexed with the NF_WEN pin) must be set.

When BOOTROM_SEL is set to 1, the Hi3521 boots from the BOOTROM.

When the Hi3521 boots from the BOOTROM, the communication mechanism over the serial port is enabled. Then the Hi3521 communicates with the software installed on the PC over the serial port. In addition, a boot program is downloaded. For details, see the *Fastboot Burning Tools Applications Notes* in the software development kit (SDK). If the communication timeout occurs when the Hi3521 boots from the BOOTROM, the system checks the levels of BOOT_SEL1 (multiplexed with the NF_ALE pin) and BOOT_SEL0 (multiplexed with the NF_CLE pin) and boots from the NAND flash or SPI flash. The details are as follows:

- When BOOTROM_SEL is 1 and communication timeout occurs, the Hi3521 boots from the external NAND flash mounted over the NANDC interface if BOOT_SEL1 is 1 and BOOT_SEL0 is 0.
- When BOOTROM_SEL is 1 and communication timeout occurs, the Hi3521 boots from the external SPI flash mounted over the SFC interface if BOOT_SEL1 is 0 and BOOT_SEL0 is 0.

1.3.2 Booting from the NAND Flash

When the Hi3521 directly boots from the NAND flash instead of jumping from the BOOTROM, the external memory must be a NAND flash. In this case, you must set the levels of BOOTROM_SEL (multiplexed with the external pin NF_WEN), BOOT_SEL1 (multiplexed with the external pin NF_ALE), and BOOT_SEL0 (multiplexed with the external pin NF_CLE) to select the boot memory.

When BOOT_SEL is 0, BOOT_SEL1 is 1, and BOOT_SEL0 is 0, the Hi3521 boots from the NAND flash mounted over the NANDC interface.

1.3.3 Booting from the SPI NOR Flash

When the Hi3521 directly boots from the SPI flash instead of jumping from the BOOTROM, the external memory must be a SPI flash. In this case, you must set the levels of BOOTROM_SEL (multiplexed with the external pin NF_WEN), BOOT_SEL1 (multiplexed with the external pin NF_ALE), and BOOT_SEL0 (multiplexed with the external pin NF_CLE) to select the boot memory.

When BOOTROM_SEL is 0, BOOT_SEL1 is 0, and BOOT_SEL0 is 0, the Hi3521 boots from the SPI flash mounted over the SFC interface.

1.3.4 Address Space Mapping

Table 1-1 describes the address space mapping.

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Table 1-1 Address space mapping

Start Address	End Address	Function	Capacity	Remarks
0xC000_0000	0xFFFF_FFFF	Reserved	1 GB	None
0x8000_0000	0xBFFF_FFFF	Address space for connecting a double data rate (DDR) to an external DDR	1 GB	None
0x5C00_0000	0x7FFF_FFFF	Reserved	576 MB	None
0x5800_0000	0x5BFF_FFFF	Storage space of the SPI flash	64 MB	None
0x5400_0000	0x57FF_FFFF	Reserved	64 MB	None
0x5000_0000	0x53FF_FFFF	Storage space of the NANDC	64 MB	None
0x4000_0000	0x4FFF_FFFF	Reserved	256 MB	None
0x3000_0000	0x3FFF_FFFF	Reserved	256 MB	None
0x2082_0000	0x2FFF_FFFF	Reserved	248 MB	None
0x2081_0000	0x2081_FFFF	Reserved	64 KB	None
0x2080_0000	0x2080_FFFF	Reserved	64 KB	None
0x2070_0000	0x207F_FFFF	L2 cache space	1 MB	None
0x206E_0000	0x206F_FFFF	Reserved	128 KB	None
0x206D_0000	0x206D_FFFF	DDR test module	64 KB	None
0x206C_0000	0x206C_FFFF	Motion detection (MD) register	64 KB	None
0x206B_0000	0x206B_FFFF	Video compress (VCMP) register	64 KB	None
0x2067_0000	0x206A_FFFF	Reserved	256 KB	None
0x2066_0000	0x2066_FFFF	JPEG encoder (JPGE) register	64 KB	None
0x2065_0000	0x2065_FFFF	Reserved	64 KB	None
0x2064_0000	0x2064_FFFF	Voice encoder (VOIE) register	64 KB	None
0x2063_0000	0x2063_FFFF	Video decoder for high-definition (VDH) register	64 KB	None
0x2062_0000	0x2062_FFFF	Video encoding (VENC) register	64 KB	None
0x2061_0000	0x2061_FFFF	Two-dimensional engine (TDE) register	64 KB	None
0x2060_0000	0x2060_FFFF	Video process subsystem (VPSS) register	64 KB	None
0x205F_0000	0x205F_FFFF	Reserved	64 KB	None
0x205E_0000	0x205E_FFFF	Intelligent video engine (IVE) register	64 KB	None

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Start Address	End Address	Function	Capacity	Remarks
0x205D_0000	0x205D_FFFF	HDMI register	64 KB	None
0x205C_0000	0x205C_FFFF	Video display (VDP) register	64 KB	None
0x2058_0000	0x205B_FFFF	Video capture (VICAP) register	256 KB	None
0x2052_0000	0x2057_FFFF	Reserved	384 KB	None
0x2040_0000	0x2051_FFFF	ARM debugging	1152 KB	None
0x2031_0000	0x203F_FFFF	Reserved	896 KB	None
0x2030_0000	0x2030_FFFF	Internal registers of ARM watchdog (WDG), timer or global interrupt controller (GIC)	64 KB	None
0x2024_0000	0x202F_FFFF	Reserved	768 KB	None
0x2023_0000	0x2023_FFFF	GPIO14 register	64 KB	None
0x2022_0000	0x2022_FFFF	GPIO13 register	64 KB	None
0x2021_0000	0x2021_FFFF	GPIO12 register	64 KB	None
0x2020_0000	0x2020_FFFF	GPIO11 register	64 KB	None
0x201F_0000	0x201F_FFFF	GPIO10 register	64 KB	None
0x201E_0000	0x201E_FFFF	GPIO9 register	64 KB	None
0x201D_0000	0x201D_FFFF	GPIO8 register	64 KB	None
0x201C_0000	0x201C_FFFF	GPIO7 register	64 KB	None
0x201B_0000	0x201B_FFFF	GPIO6 register	64 KB	None
0x201A_0000	0x201A_FFFF	GPIO5 register	64 KB	None
0x2019_0000	0x2019_FFFF	GPIO4 register	64 KB	None
0x2018_0000	0x2018_FFFF	GPIO3 register	64 KB	None
0x2017_0000	0x2017_FFFF	GPIO2 register	64 KB	None
0x2016_0000	0x2016_FFFF	GPIO1 register	64 KB	None
0x2015_0000	0x2015_FFFF	GPIO0 register	64 KB	None
0x2014_0000	0x2014_FFFF	Timer3 register	64 KB	None
0x2013_0000	0x2013_FFFF	Timer2 register	64 KB	None
0x2012_0000	0x2012_FFFF	Reserved	64 KB	None
0x2011_0000	0x2011_FFFF	DDRC register	64 KB	None
0x2010_0000	0x2010_FFFF	Reserved	64 KB	None
0x200F_0000	0x200F_FFFF	I/O configuration register	64 KB	None

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Start Address	End Address	Function	Capacity	Remarks
0x200E_0000	0x200E_FFFF	Reserved	64 KB	None
0x200D_0000	0x200D_FFFF	I^2C register	64 KB	None
0x200C_0000	0x200C_FFFF	SPI register	64 KB	None
0x200B_0000	0x200B_FFFF	UART3 register	64 KB	None
0x200A_0000	0x200A_FFFF	UART2 register	64 KB	None
0x2009_0000	0x2009_FFFF	UART1 register	64 KB	None
0x2008_0000	0x2008_FFFF	UART0 register	64 KB	None
0x2007_0000	0x2007_FFFF	IR register	64 KB	None
0x2006_0000	0x2006_FFFF	Real-time clock (RTC) register	64 KB	None
0x2005_0000	0x2005_FFFF	SYS_CTRL register	64 KB	None
0x2004_0000	0x2004_FFFF	WDG register	64 KB	None
0x2003_0000	0x2003_FFFF	CRG register	64 KB	None
0x2002_0000	0x2002_FFFF	Reserved	64 KB	None
0x2001_0000	0x2001_FFFF	Timer1 register	64 KB	None
0x2000_0000	0x2000_FFFF	Timer0 register	64 KB	None
0x101E_0000	0x1FFF_FFFF	Reserved	256 MB	None
0x101C_0000	0x101D_FFFF	GMAC register	128 KB	None
0x1018_0000	0x101B_0000	Reserved	256 KB	None
0x1017_0000	0x1017_FFFF	JPEG decoder (JPGD) register	64 KB	None
0x1016_0000	0x1016_FFFF	Reserved	64 KB	None
0x1015_0000	0x1015_FFFF	Start code detect (SCD) register	64 KB	None
0x100E_0000	0x1014_FFFF	Reserved	448 KB	None
0x100D_0000	0x100D_FFFF	direct memory access controller (DMAC) register	64 KB	None
0x100C_0000	0x100C_FFFF	CIPHER register	64 KB	None
0x100B_0000	0x100B_FFFF	USB enhanced host controller interface (EHCI) register	64 KB	None
0x100A_0000	0x100A_FFFF	USB open host controller interface (OHCI) register	64 KB	None
0x1009_0000	0x1009_FFFF	Reserved	64 KB	None
0x1008_0000	0x1008_FFFF	SATA register	64 KB	None

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Start Address	End Address	Function	Capacity	Remarks
0x1007_0000	0x1007_FFFF	eFUSE register and operation space	64 KB	None
0x1006_0000	0x1006_FFFF	Sonic input/output 3 (SIO3) register	64 KB	HDMI audio
0x1005_0000	0x1005_FFFF	SIO2 register	64 KB	Bidirectional talkback
0x1004_0000	0x1004_FFFF	SIO1 register	64 KB	Only for input
0x1003_0000	0x1003_FFFF	SIO0 register	64 KB	Only for input
0x1002_0000	0x1002_FFFF	SDIO register	64 KB	None
0x1001_0000	0x1001_FFFF	SPI NOR flash register	64 KB	None
0x1000_0000	0x1000_FFFF	NANDC register	64 KB	None
0x0402_0000	0x0FFF_FFFF	Reserved	192 MB	None
0x0401_0000	0x0401_FFFF	On-chip RAM address space	64 KB	The actual capacity is 10 KB.
0x0400_0000	0x0400_FFFF	BOOTROM address space	64 KB	The actual capacity is 4 KB.
0x0000_0000	0x03FF_FFFF	During address remapping, the address space points to the boot address space. After address remapping clear, the address space points to the on-chip RAM of the Hi3521.	64 MB	During address remapping, the storage space pointed by the boot address space varies according to boot mode. 1. If the system boots from the BOOTROM, the boot address space is the storage space of the on-chip BOOTROM. 2. If the system boots from the SPI flash, the boot address space is the storage space of the SPI NOR flash. 3. If the system boots from the NAND flash, the boot address space is the

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Start Address	End Address	Function	Capacity	Remarks
				storage space of the NAND flash. For details about boot modes, see section 1.3 "Boot Modes."

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Contents

2 Hardware 2-1
2.1 Package and Pinout 2-1
2.1.1 Package 2-1
2.1.2 Pinout 2-3
2.2 Pin Descriptions 2-13
2.2.1 Pin Types 2-13
2.2.2 DDR Pins 2-14
2.2.3 GPIO Pins 2-18
2.2.4 HDMI Pins 2-19
2.2.5 I2C Pins 2-20
2.2.6 IR Pin 2-20
2.2.7 JTAG Pins 2-21
2.2.8 GMAC Pins 2-21
2.2.9 NANDC Pins 2-24
2.2.10 SYS Pins 2-26
2.2.11 SATA Pins 2-27
2.2.12 SFC Pins 2-28
2.2.13 SIO Pins 2-29
2.2.14 SPI Pins 2-32
2.2.15 UART Pins 2-33
2.2.16 USB Pins 2-34
2.2.17 VDAC Pins 2-36
2.2.18 VIU Pins 2-37
2.2.19 VOU Pins 2-42
2.2.20 OSC Pins 2-48
2.2.21 eFUSE Pin 2-48
2.2.22 PLL Pins 2-48
2.2.23 Power Pins and GND Pins 2-49
2.3 I/O Config Registers 2-50
2.3.1 Summary of Multiplexing Control Registers 2-50
2.3.2 Descriptions of Multiplexing Control Registers 2-56
2.4 Software Multiplexed Pins 2-116

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2.5 Hardware Multiplexed Pins....2-137
2.6 Electrical Specifications....2-141
2.6.1 Power Consumption Specifications....2-141
2.6.2 Temperature and Thermal Resistance Parameters....2-141
2.6.3 Working Conditions....2-142
2.6.4 Sequence of Power-On and Power-Off....2-143
2.6.5 DC/AC Electrical Specifications....2-143
2.7 PCB Design Recommendations....2-146
2.8 Interface Timings....2-146
2.8.1 DDR Interface Timings....2-146
2.8.2 NANDC Interface Timings....2-150
2.8.3 SFC Interface Timings....2-153
2.8.4 Ethernet MAC Port Timings....2-154
2.8.5 VI Interface Timing....2-158
2.8.6 VO Interface Timing....2-159
2.8.7 SIO Interface Timings....2-159
2.8.8 I2C Interface Timing....2-161
2.8.9 SPI Timings....2-162

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Figures

Figure 2-1 Top view 2-1
Figure 2-2 Bottom view 2-2
Figure 2-3 Side view 2-2
Figure 2-4 Enlarged view of detail "A" 2-2
Figure 2-5 Pin map part 1 (A1–P14) 2-4
Figure 2-6 Pin map part 2 (R1–AH14) 2-4
Figure 2-7 Pin map part 3 (A15–P28) 2-5
Figure 2-8 Pin map part 4 (R15–AH28) 2-5
Figure 2-9 Write timing of dqs_out relative to dq_out for the DDR2 2-146
Figure 2-10 Write timing of dqs_out relative to dq_out for the DDR3 2-146
Figure 2-11 Write timing of dqs_out relative to CK for the DDR2 2-147
Figure 2-12 Write timing of dqs_out relative to CK for the DDR3 2-147
Figure 2-13 Write timing of CMD/ADDR relative to CK 2-147
Figure 2-14 Output timing of the DDRn SDRAM 2-148
Figure 2-15 NANDC command cycle timing 2-150
Figure 2-16 NANDC address cycle timing 2-151
Figure 2-17 NANDC write data timing 2-152
Figure 2-18 NANDC read data timing 2-153
Figure 2-19 SFC input timing 2-153
Figure 2-20 SFC output timing 2-154
Figure 2-21 100 Mbit/s receive timing of the MII 2-154
Figure 2-22 100 Mbit/s transmit timing of the MII 2-155
Figure 2-23 10 Mbit/s receive timing of the MII 2-155
Figure 2-24 10 Mbit/s transmit timing of the MII 2-155
Figure 2-25 Receive timing parameters of the MII 2-155
Figure 2-26 Transmit timing parameters of the MII 2-156

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Figure 2-27 1000 Mbit/s receive timing of the RGMII 2-156
Figure 2-28 1000 Mbit/s transmit timing of the RGMII 2-156
Figure 2-29 Read timing of the MDIO interface 2-157
Figure 2-30 Write timing of the MDIO interface 2-157
Figure 2-31 Receive timing parameters of the MDIO interface 2-158
Figure 2-32 VI interface timing 2-158
Figure 2-33 VO interface timing 2-159
Figure 2-34 I^2S interface receive timing 2-160
Figure 2-35 I^2S interface transmit timing 2-160
Figure 2-36 PCM interface receive timing 2-160
Figure 2-37 PCM interface transmit timing 2-161
Figure 2-38 I^2C transfer timing 2-161
Figure 2-39 SPICK timing 2-162
Figure 2-40 SPI timing in master mode (sph = 0) 2-163
Figure 2-41 SPI timing in master mode (sph = 1) 2-163

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Tables

Table 2-1 Package dimensions 2-3
Table 2-2 Pin arrangement 2-6
Table 2-3 I/O pin types 2-13
Table 2-4 DDR power pins 2-14
Table 2-5 DDR pins 2-14
Table 2-6 GPIO pins 2-18
Table 2-7 HDMI pins 2-19
Table 2-8 I^2C pins 2-20
Table 2-9 IR pin 2-21
Table 2-10 JTAG pins 2-21
Table 2-11 DVDD2533 pins 2-21
Table 2-12 MDIO pins 2-22
Table 2-13 GMAC pins 2-22
Table 2-14 NANDC pins 2-24
Table 2-15 SYS pins 2-27
Table 2-16 SATA pins 2-27
Table 2-17 SFC pins 2-28
Table 2-18 SIO0 pins 2-29
Table 2-19 SIO1 pins 2-30
Table 2-20 SIO2 pins 2-31
Table 2-21 SPI pins 2-32
Table 2-22 UART0 pins 2-33
Table 2-23 UART1 pins 2-33
Table 2-24 USB pins 2-34
Table 2-25 VDAC0 pins 2-36
Table 2-26 VDAC1 pins 2-36

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Table 2-27 VIU0 pins 2-37
Table 2-28 VIU1 pins 2-40
Table 2-29 VOU pins 2-42
Table 2-30 OSC pins 2-48
Table 2-31 eFUSE pin 2-48
Table 2-32 PLL pins 2-48
Table 2-33 DVDD10 pins 2-49
Table 2-34 DVDD33 pins 2-49
Table 2-35 VSS pins 2-49
Table 2-36 Summary of multiplexing control registers (base address:0x200F_0000) 2-50
Table 2-37 Software multiplexed pins of VIU0 2-116
Table 2-38 Description of the software multiplexed pins of VIU0 2-117
Table 2-39 Software multiplexed pins of VIU1 2-119
Table 2-40 Description of the software multiplexed pins of VIU1 2-119
Table 2-41 Software multiplexed pins of the VOU 2-121
Table 2-42 Description of the software multiplexed pins of the VOU 2-123
Table 2-43 Software multiplexed pins of SIO0 2-126
Table 2-44 Description of the software multiplexed pins of SIO0 2-126
Table 2-45 Software multiplexed pins of SIO1 2-127
Table 2-46 Description of the software multiplexed pins of SIO1 2-127
Table 2-47 Software multiplexed pins of SIO2 2-127
Table 2-48 Description of the software multiplexed pins of SIO2 2-128
Table 2-49 Software multiplexed pins of the SPI 2-128
Table 2-50 Description of the software multiplexed pins of the SPI 2-129
Table 2-51 Software multiplexed pins of the I^2C interface 2-129
Table 2-52 Description of the software multiplexed pins of the I^2C interface 2-130
Table 2-53 Software multiplexed pins of UART1 2-130
Table 2-54 Description of the software multiplexed pins of UART1 2-130
Table 2-55 Software multiplexed pins of the GMAC interface 2-131
Table 2-56 Description of the software multiplexed pins of the GMAC interface 2-131
Table 2-57 Software multiplexed pin of the IR 2-132
Table 2-58 Description of the software multiplexed pin of the IR 2-132
Table 2-59 Software multiplexed pins of the NFC 2-132

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Table 2-60 Description of the software multiplexed pins of the NFC 2-133
Table 2-61 Software multiplexed pins of the SFC 2-134
Table 2-62 Description of the software multiplexed pins of the SFC 2-134
Table 2-63 Software multiplexed pins of the USB port 2-135
Table 2-64 Description of the software multiplexed pins of the USB port 2-135
Table 2-65 Software multiplexed pins of the GPIO interface 2-135
Table 2-66 Description of the software multiplexed pins of the GPIO interface 2-136
Table 2-67 Software multiplexed pins of the SATA interface 2-136
Table 2-68 Description of the software multiplexed pins of the SATA interface 2-136
Table 2-69 Software multiplexed pins of the HDMI 2-137
Table 2-70 Description of the software multiplexed pins of the HDMI 2-137
Table 2-71 Hardware multiplexed pin of the VOU 2-137
Table 2-72 Description of the hardware multiplexed pin of the VOU 2-138
Table 2-73 Hardware multiplexed pin of SIO2 2-138
Table 2-74 Description of the hardware multiplexed pin of SIO2 2-138
Table 2-75 Hardware multiplexed pins of the SPI 2-138
Table 2-76 Description of the hardware multiplexed pins of the SPI 2-139
Table 2-77 Hardware multiplexed pin of the MDIO interface 2-139
Table 2-78 Description of the hardware multiplexed pin of the MDIO interface 2-139
Table 2-79 Hardware multiplexed pins of the NFC 2-140
Table 2-80 Description of the hardware multiplexed pins of the NFC 2-140
Table 2-81 Power consumption specifications of Hi3521 2-141
Table 2-82 Power consumption specifications of Hi3520A 2-141
Table 2-84 Working conditions 2-142
Table 2-85 DC electrical specifications (DVDD33 = 3.3 V) 2-143
Table 2-86 DC electrical specifications in DDR2 SSTL18 mode (DVDD1518 = 1.8 V) 2-144
Table 2-87 AC electrical specifications in DDR2 mode (DVDD1518 = 1.8 V) 2-145
Table 2-88 DC electrical specifications in DDR3 mode (DVDD1518 = 1.5 V) 2-145
Table 2-89 AC electrical specifications in DDR3 mode (DVDD1518 = 1.5 V) 2-145
Table 2-90 DDR2 clock parameters 2-148
Table 2-91 Parameters for the DDR2-800 SDRAM 2-149
Table 2-92 DDR3 clock parameters 2-149
Table 2-93 Parameters for the DDR3-1066 SDRAM 2-149

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Table 2-94 NANDC command cycle timing parameters 2-150
Table 2-95 NANDC address cycle timing parameters 2-151
Table 2-96 NANDC write data timing parameters 2-152
Table 2-97 NANDC read data timing parameters 2-153
Table 2-98 SFC input timing parameters 2-154
Table 2-99 SFC output timing parameters 2-154
Table 2-100 MII timing parameters 2-156
Table 2-101 RGMII timing parameters 2-157
Table 2-102 Timing parameters of the MDIO interface 2-158
Table 2-103 VI interface timing parameters 2-159
Table 2-104 VO interface timing parameters 2-159
Table 2-105 I^2S interface timing parameters 2-160
Table 2-106 PCM interface timing parameters 2-161
Table 2-107 I^2C interface timing parameters 2-161
Table 2-108 SPI timing parameters 2-163

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2 Hardware

2.1 Package and Pinout

2.1.1 Package

The Hi3521 uses the package of environmental health and safety (EHS) flip-chip ball grid array (FCBGA). It has 449 pins, its body size is 19 mm x 19 mm (0.75 in. x 0.75 in.), and its ball pitch is 0.8 mm (0.031 in.) in the core power area or 0.65 mm (0.026 in.) in other areas. Figure 2-1 to Figure 2-5 show the FCPBGA package views. Table 2-1 lists the specifications of the PBGA package.

Figure 2-1 Top view

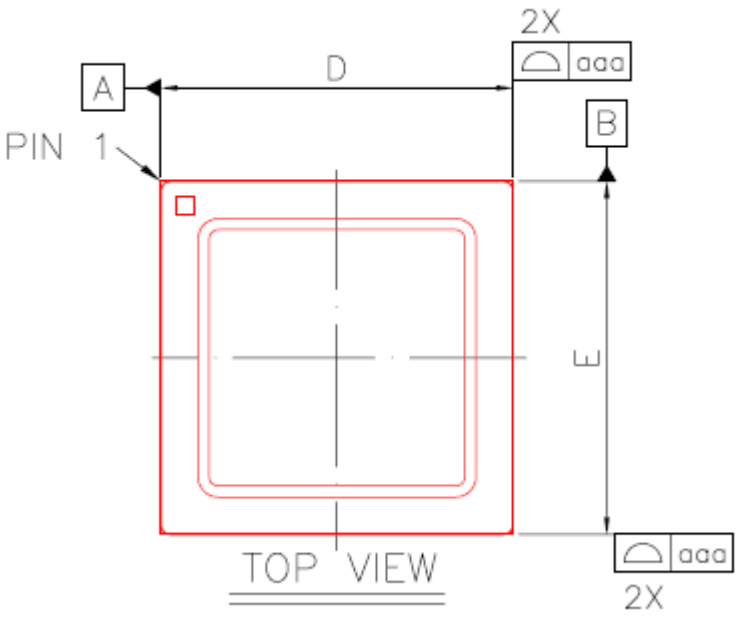

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Figure 2-2 Bottom view

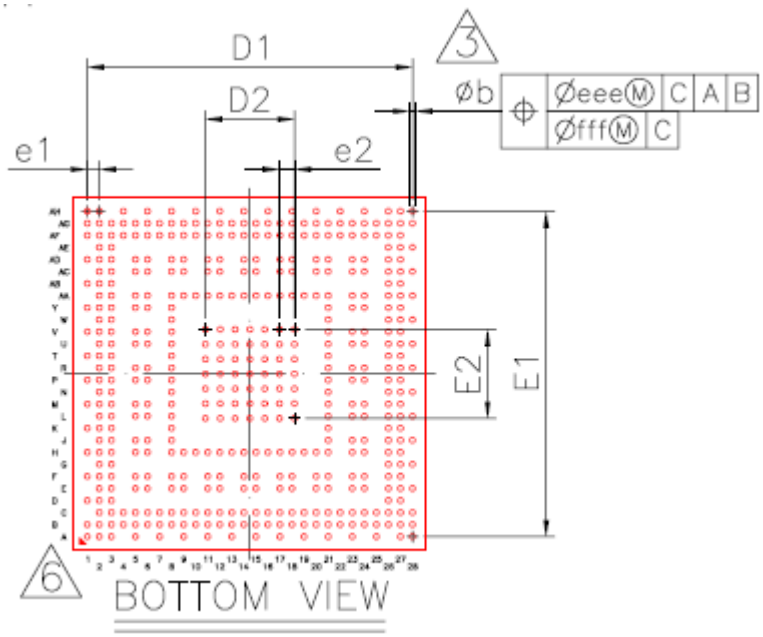

Figure 2-3 Side view

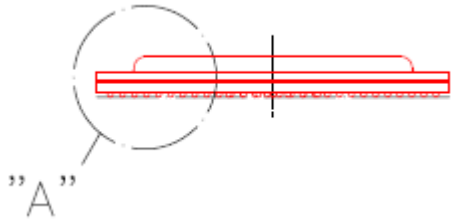

Figure 2-4 Enlarged view of detail "A"

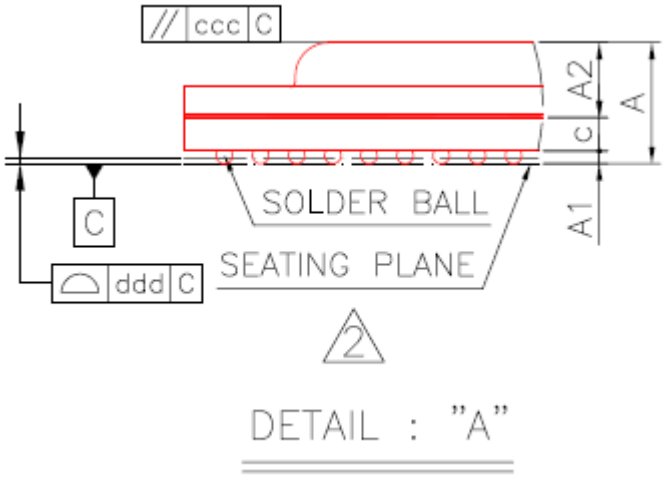

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Table 2-1 Package dimensions

Parameter	Dimensions (mm)		
	Min	**Typ**	**Max**
A	2.06	2.18	2.30
A1	0.18	0.23	0.28
A2	1.25	1.35	1.45
c	0.55	0.60	0.65
D/E	18.80	19.00	19.20
D1/E1	None	17.55	None
D2/E2	None	4.80	None
e1	None	0.65	None
e2	None	0.80	None
b	0.25	0.30	0.35
aaa	0.20		
ccc	0.25		
ddd	0.15		
eee	0.25		
fff	0.10		

2.1.2 Pinout

Pin Maps

Figure 2-5 to Figure 2-8 show pin maps.

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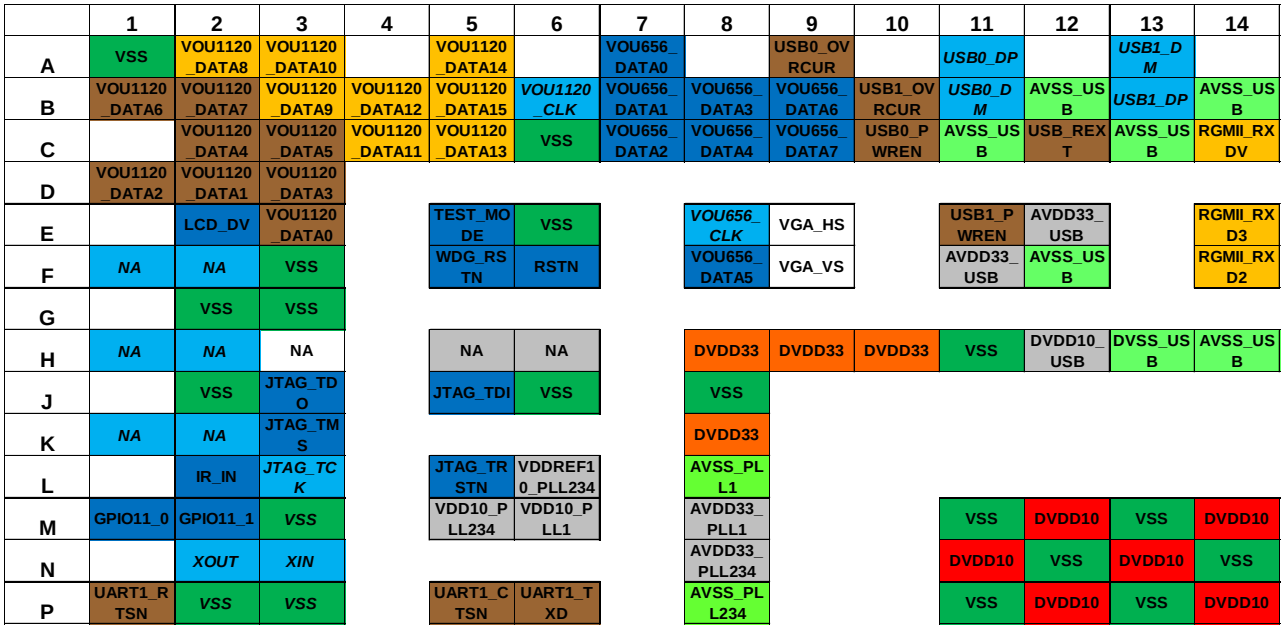
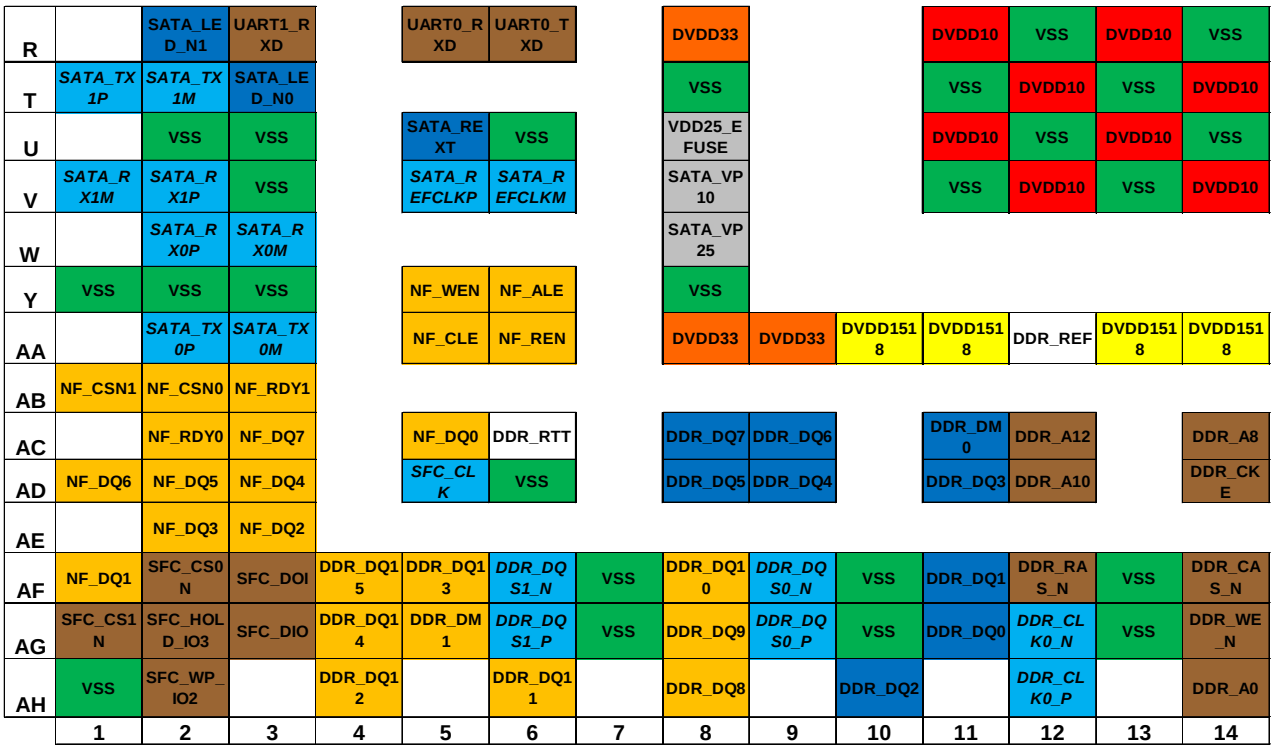
Figure 2-5 Pin map part 1 (A1–P14)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VSS	VOU1120_DATA8	VOU1120_DATA10		VOU1120_DATA14		VOU656_DATA0		USB0_OVRCUR		USB0_DP		USB1_DM	
B	VOU1120_DATA6	VOU1120_DATA7	VOU1120_DATA9	VOU1120_DATA12	VOU1120_DATA15	VOU1120_CLK	VOU656_DATA1	VOU656_DATA3	VOU656_DATA6	USB1_OVRCUR	USB0_DM	AVSS_USB	USB1_DP	AVSS_USB
C		VOU1120_DATA4	VOU1120_DATA5	VOU1120_DATA11	VOU1120_DATA13	VSS	VOU656_DATA2	VOU656_DATA4	VOU656_DATA7	USB0_PWREN	AVSS_USB	USB_REXT	AVSS_USB	RGMII_RXDV
D	VOU1120_DATA2	VOU1120_DATA1	VOU1120_DATA3											
E		LCD_DV	VOU1120_DATA0		TEST_MODE	VSS		VOU656_CLK	VGA_HS		USB1_PWREN	AVDD33_USB		RGMII_RXD3
F	NA	NA	VSS		WDG_RSTN	RSTN		VOU656_DATA5	VGA_VS		AVDD33_USB	AVSS_USB		RGMII_RXD2
G		VSS	VSS											
H	NA	NA	NA		NA	NA		DVDD33	DVDD33	DVDD33	VSS	DVDD10_USB	DVSS_USB	AVSS_USB
J		VSS	JTAG_TDO		JTAG_TDI	VSS		VSS						
K	NA	NA	JTAG_TMS					DVDD33						
L		IR_IN	JTAG_TCK		JTAG_TRSTN	VDDREF10_PLL234		AVSS_PLL1						
M	GPIO11_0	GPIO11_1	VSS		VDD10_PLL234	VDD10_PLL1		AVDD33_PLL1			VSS	DVDD10	VSS	DVDD10
N		XOUT	XIN					AVDD33_PLL234			DVDD10	VSS	DVDD10	VSS
P	UART1_RTSN	VSS	VSS		UART1_CTSN	UART1_TXD		AVSS_PLL234			VSS	DVDD10	VSS	DVDD10

Figure 2-6 Pin map part 2 (R1–AH14)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
R		SATA_LED_N1	UART1_RXD		UART0_RXD	UART0_TXD		DVDD33			DVDD10	VSS	DVDD10	VSS
T	SATA_TX1P	SATA_TX1M	SATA_LED_N0					VSS			VSS	DVDD10	VSS	DVDD10
U		VSS	VSS		SATA_REXT	VSS		VDD25_EFUSE			DVDD10	VSS	DVDD10	VSS
V	SATA_RX1M	SATA_RX1P	VSS		SATA_REFCLKP	SATA_REFCLKM		SATA_VP10			VSS	DVDD10	VSS	DVDD10
W		SATA_RX0P	SATA_RX0M					SATA_VP25						
Y	VSS	VSS	VSS		NF_WEN	NF_ALE		VSS						
AA		SATA_TX0P	SATA_TX0M		NF_CLE	NF_REN		DVDD33	DVDD33	DVDD1518	DVDD1518	DDR_REF	DVDD1518	DVDD1518
AB	NF_CSN1	NF_CSN0	NF_RDY1											
AC		NF_RDY0	NF_DQ7		NF_DQ0	DDR_RTT		DDR_DQ7	DDR_DQ6		DDR_DM0	DDR_A12		DDR_A8
AD	NF_DQ6	NF_DQ5	NF_DQ4		SFC_CLK	VSS		DDR_DQ5	DDR_DQ4		DDR_DQ3	DDR_A10		DDR_CKE
AE		NF_DQ3	NF_DQ2											
AF	NF_DQ1	SFC_CS0N	SFC_DOI	DDR_DQ15	DDR_DQ13	DDR_DQS1_N	VSS	DDR_DQ10	DDR_DQS0_N	VSS	DDR_DQ1	DDR_RAS_N	VSS	DDR_CAS_N
AG	SFC_CS1N	SFC_HOLD_IO3	SFC_DIO	DDR_DQ14	DDR_DM1	DDR_DQS1_P	VSS	DDR_DQ9	DDR_DQS0_P	VSS	DDR_DQ0	DDR_CLK0_N	VSS	DDR_WE_N
AH	VSS	SFC_WP_IO2		DDR_DQ12		DDR_DQ11		DDR_DQ8		DDR_DQ2		DDR_CLK0_P		DDR_A0

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Figure 2-7 Pin map part 3 (A15–P28)

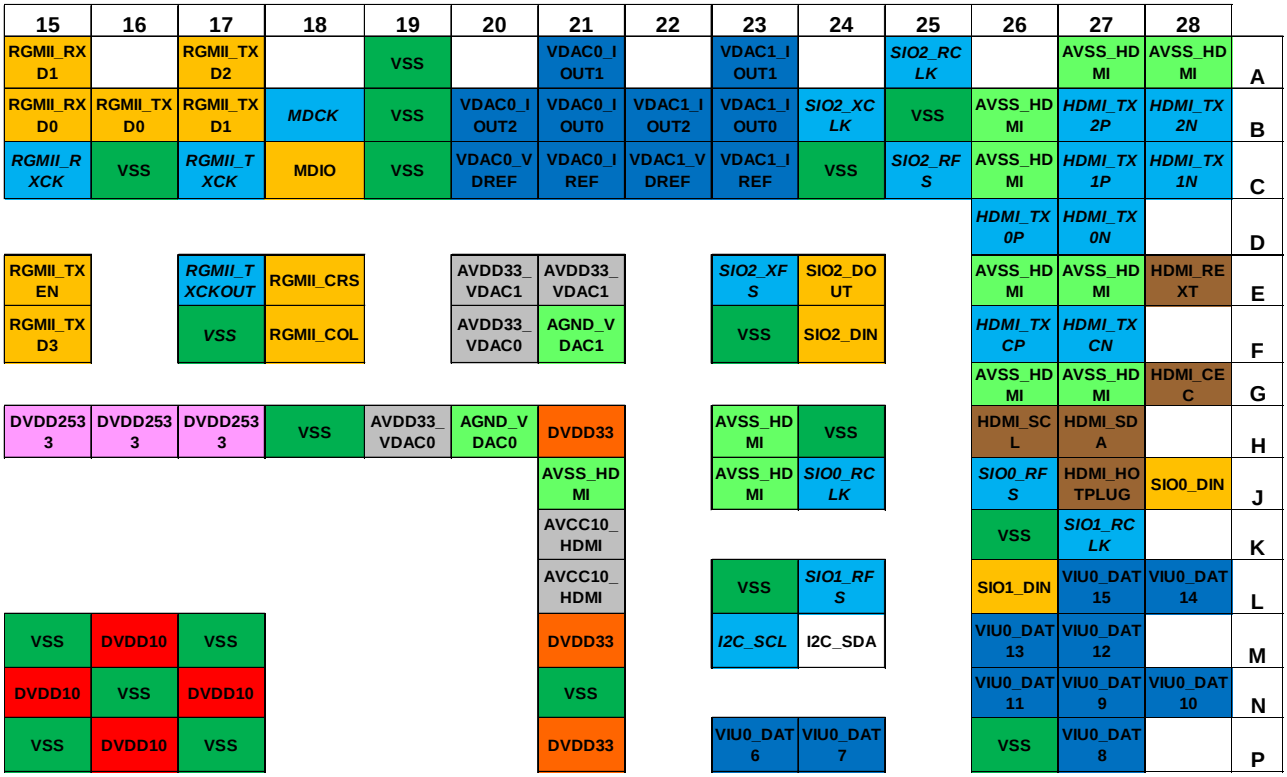
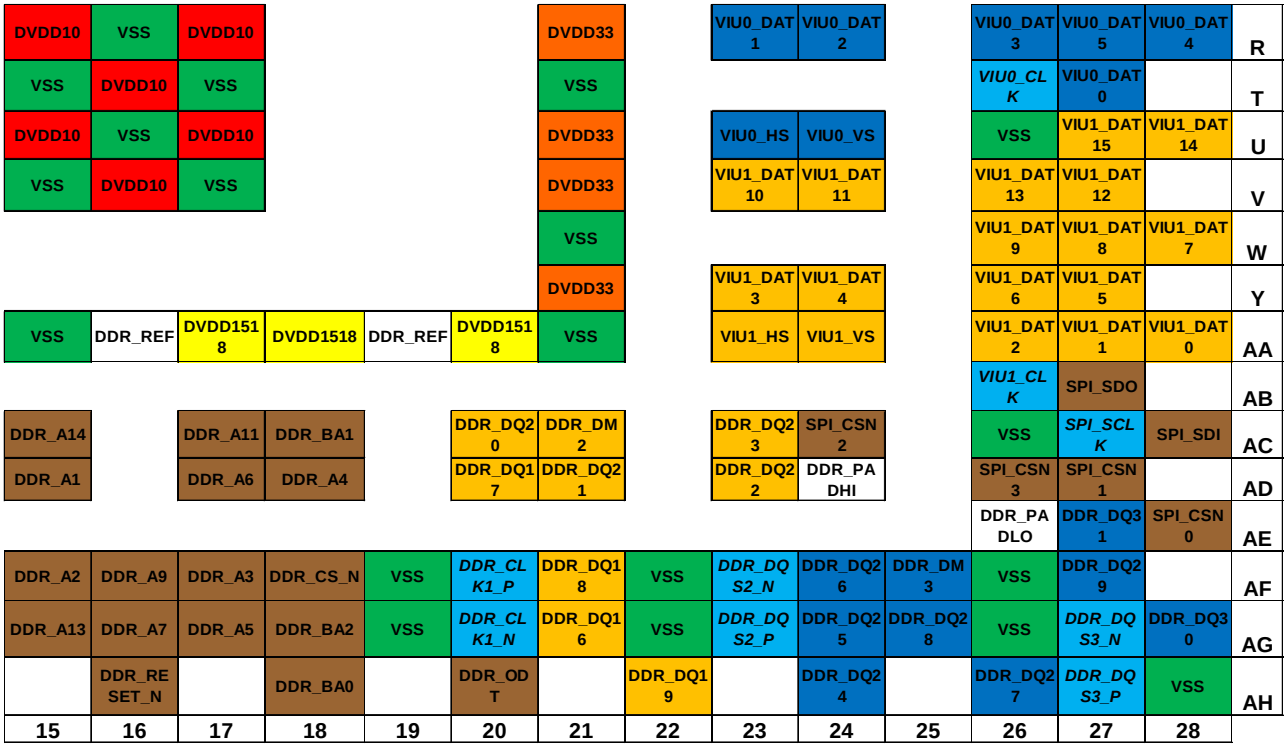


Figure 2-8 Pin map part 4 (R15–AH28)



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Pin Arrangement

Table 2-2 lists the pins of the Hi3521 based on their positions.

Table 2-2 Pin arrangement

Position	Pin Name	Position	Pin Name
A1	VSS	R8	DVDD33
A2	VOU1120_DATA8	R11	DVDD10
A3	VOU1120_DATA10	R12	VSS
A5	VOU1120_DATA14	R13	DVDD10
A7	VOU656_DATA0	R14	VSS
A9	USB0_OVRCUR	R15	DVDD10
A11	USB0_DP	R16	VSS
A13	USB1_DM	R17	DVDD10
A15	RGMII_RXD1	R21	DVDD33
A17	RGMII_TXD2	R23	VIU0_DAT1
A19	VSS	R24	VIU0_DAT2
A21	VDAC0_IOUT1	R26	VIU0_DAT3
A23	VDAC1_IOUT1	R27	VIU0_DAT5
A25	SIO2_RCLK	R28	VIU0_DAT4
A27	AVSS_HDMI	T1	SATA_TX1P
A28	AVSS_HDMI	T2	SATA_TX1M
B1	VOU1120_DATA6	T3	SATA_LED_N0
B2	VOU1120_DATA7	T8	VSS
B3	VOU1120_DATA9	T11	VSS
B4	VOU1120_DATA12	T12	DVDD10
B5	VOU1120_DATA15	T13	VSS
B6	VOU1120_CLK	T14	DVDD10
B7	VOU656_DATA1	T15	VSS
B8	VOU656_DATA3	T16	DVDD10
B9	VOU656_DATA6	T17	VSS
B10	USB1_OVRCUR	T21	VSS
B11	USB0_DM	T26	VIU0_CLK

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Position	Pin Name	Position	Pin Name
B12	AVSS_USB	T27	VIU0_DAT0
B13	USB1_DP	U2	VSS
B14	AVSS_USB	U3	VSS
B15	RGMII_RXD0	U5	SATA_REXT
B16	RGMII_TXD0	U6	VSS
B17	RGMII_TXD1	U8	VDD25_EFUSE
B18	MDCK	U11	DVDD10
B19	VSS	U12	VSS
B20	VDAC0_IOUT2	U13	DVDD10
B21	VDAC0_IOUT0	U14	VSS
B22	VDAC1_IOUT2	U15	DVDD10
B23	VDAC1_IOUT0	U16	VSS
B24	SIO2_XCLK	U17	DVDD10
B25	VSS	U21	DVDD33
B26	AVSS_HDMI	U23	VIU0_HS
B27	HDMI_TX2P	U24	VIU0_VS
B28	HDMI_TX2N	U26	VSS
C2	VOU1120_DATA4	U27	VIU1_DAT15
C3	VOU1120_DATA5	U28	VIU1_DAT14
C4	VOU1120_DATA11	V1	SATA_RX1M
C5	VOU1120_DATA13	V2	SATA_RX1P
C6	VSS	V3	VSS
C7	VOU656_DATA2	V5	SATA_REFCLKP
C8	VOU656_DATA4	V6	SATA_REFCLKM
C9	VOU656_DATA7	V8	SATA_VP10
C10	USB0_PWREN	V11	VSS
C11	AVSS_USB	V12	DVDD10
C12	USB_REXT	V13	VSS
C13	AVSS_USB	V14	DVDD10
C14	RGMII_RXDV	V15	VSS
C15	RGMII_RXCK	V16	DVDD10

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Position	Pin Name	Position	Pin Name
C16	VSS	V17	VSS
C17	RGMII_TXCK	V21	DVDD33
C18	MDIO	V23	VIU1_DAT10
C19	VSS	V24	VIU1_DAT11
C20	VDAC0_VDREF	V26	VIU1_DAT13
C21	VDAC0_IREF	V27	VIU1_DAT12
C22	VDAC1_VDREF	W2	SATA_RX0P
C23	VDAC1_IREF	W3	SATA_RX0M
C24	VSS	W8	SATA_VP25
C25	SIO2_RFS	W21	VSS
C26	AVSS_HDMI	W26	VIU1_DAT9
C27	HDMI_TX1P	W27	VIU1_DAT8
C28	HDMI_TX1N	W28	VIU1_DAT7
D1	VOU1120_DATA2	Y1	VSS
D2	VOU1120_DATA1	Y2	VSS
D3	VOU1120_DATA3	Y3	VSS
D26	HDMI_TX0P	Y5	NF_WEN
D27	HDMI_TX0N	Y6	NF_ALE
E2	LCD_DV	Y8	VSS
E3	VOU1120_DATA0	Y21	DVDD33
E5	TEST_MODE	Y23	VIU1_DAT3
E6	VSS	Y24	VIU1_DAT4
E8	VOU656_CLK	Y26	VIU1_DAT6
E9	VGA_HS	Y27	VIU1_DAT5
E11	USB1_PWREN	AA2	SATA_TX0P
E12	AVDD33_USB	AA3	SATA_TX0M
E14	RGMII_RXD3	AA5	NF_CLE
E15	RGMII_TXEN	AA6	NF_REN
E17	RGMII_TXCKOUT	AA8	DVDD33
E18	RGMII_CRS	AA9	DVDD33
E20	AVDD33_VDAC1	AA10	DVDD1518

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Position	Pin Name	Position	Pin Name
E21	AVDD33_VDAC1	AA11	DVDD1518
E23	SIO2_XFS	AA12	DDR_REF
E24	SIO2_DOUT	AA13	DVDD1518
E26	AVSS_HDMI	AA14	DVDD1518
E27	AVSS_HDMI	AA15	VSS
E28	HDMI_REXT	AA16	DDR_REF
F1	NA	AA17	DVDD1518
F2	NA	AA18	DVDD1518
F3	VSS	AA19	DDR_REF
F5	WDG_RSTN	AA20	DVDD1518
F6	RSTN	AA21	VSS
F8	VOU656_DATA5	AA23	VIU1_HS
F9	VGA_VS	AA24	VIU1_VS
F11	AVDD33_USB	AA26	VIU1_DAT2
F12	AVSS_USB	AA27	VIU1_DAT1
F14	RGMII_RXD2	AA28	VIU1_DAT0
F15	RGMII_TXD3	AB1	NF_CSN1
F17	VSS	AB2	NF_CSN0
F18	RGMII_COL	AB3	NF_RDY1
F20	AVDD33_VDAC0	AB26	VIU1_CLK
F21	AGND_VDAC1	AB27	SPI_SDO
F23	VSS	AC2	NF_RDY0
F24	SIO2_DIN	AC3	NF_DQ7
F26	HDMI_TXCP	AC5	NF_DQ0
F27	HDMI_TXCN	AC6	DDR_RTT
G2	VSS	AC8	DDR_DQ7
G3	VSS	AC9	DDR_DQ6
G26	AVSS_HDMI	AC11	DDR_DM0
G27	AVSS_HDMI	AC12	DDR_A12
G28	HDMI_CEC	AC14	DDR_A8
H1	NA	AC15	DDR_A14

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Position	Pin Name	Position	Pin Name
H2	NA	AC17	DDR_A11
H3	NA	AC18	DDR_BA1
H5	NA	AC20	DDR_DQ20
H6	NA	AC21	DDR_DM2
H8	DVDD33	AC23	DDR_DQ23
H9	DVDD33	AC24	SPI_CSN2
H10	DVDD33	AC26	VSS
H11	VSS	AC27	SPI_SCLK
H12	DVDD10_USB	AC28	SPI_SDI
H13	DVSS_USB	AD1	NF_DQ6
H14	AVSS_USB	AD2	NF_DQ5
H15	DVDD2533	AD3	NF_DQ4
H16	DVDD2533	AD5	SFC_CLK
H17	DVDD2533	AD6	VSS
H18	VSS	AD8	DDR_DQ5
H19	AVDD33_VDAC0	AD9	DDR_DQ4
H20	AGND_VDAC0	AD11	DDR_DQ3
H21	DVDD33	AD12	DDR_A10
H23	AVSS_HDMI	AD14	DDR_CKE
H24	VSS	AD15	DDR_A1
H26	HDMI_SCL	AD17	DDR_A6
H27	HDMI_SDA	AD18	DDR_A4
J2	VSS	AD20	DDR_DQ17
J3	JTAG_TDO	AD21	DDR_DQ21
J5	JTAG_TDI	AD23	DDR_DQ22
J6	VSS	AD24	DDR_PADHI
J8	VSS	AD26	SPI_CSN3
J21	AVSS_HDMI	AD27	SPI_CSN1
J23	AVSS_HDMI	AE2	NF_DQ3
J24	SIO0_RCLK	AE3	NF_DQ2
J26	SIO0_RFS	AE26	DDR_PADLO

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Position	Pin Name	Position	Pin Name
J27	HDMI_HOTPLUG	AE27	DDR_DQ31
J28	SIO0_DIN	AE28	SPI_CSN0
K1	NA	AF1	NF_DQ1
K2	NA	AF2	SFC_CS0N
K3	JTAG_TMS	AF3	SFC_DOI
K8	DVDD33	AF4	DDR_DQ15
K21	AVCC10_HDMI	AF5	DDR_DQ13
K26	VSS	AF6	DDR_DQS1_N
K27	SIO1_RCLK	AF7	VSS
L2	IR_IN	AF8	DDR_DQ10
L3	JTAG_TCK	AF9	DDR_DQS0_N
L5	JTAG_TRSTN	AF10	VSS
L6	VDDREF10_PLL234	AF11	DDR_DQ1
L8	AVSS_PLL1	AF12	DDR_RAS_N
L21	AVCC10_HDMI	AF13	VSS
L23	VSS	AF14	DDR_CAS_N
L24	SIO1_RFS	AF15	DDR_A2
L26	SIO1_DIN	AF16	DDR_A9
L27	VIU0_DAT15	AF17	DDR_A3
L28	VIU0_DAT14	AF18	DDR_CS_N
M1	GPIO11_0	AF19	VSS
M2	GPIO11_1	AF20	DDR_CLK1_P
M3	VSS	AF21	DDR_DQ18
M5	VDD10_PLL234	AF22	VSS
M6	VDD10_PLL1	AF23	DDR_DQS2_N
M8	AVDD33_PLL1	AF24	DDR_DQ26
M11	VSS	AF25	DDR_DM3
M12	DVDD10	AF26	VSS
M13	VSS	AF27	DDR_DQ29
M14	DVDD10	AG1	SFC_CS1N
M15	VSS	AG2	SFC_HOLD_IO3

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Position	Pin Name	Position	Pin Name
M16	DVDD10	AG3	SFC_DIO
M17	VSS	AG4	DDR_DQ14
M21	DVDD33	AG5	DDR_DM1
M23	I2C_SCL	AG6	DDR_DQS1_P
M24	I2C_SDA	AG7	VSS
M26	VIU0_DAT13	AG8	DDR_DQ9
M27	VIU0_DAT12	AG9	DDR_DQS0_P
N2	XOUT	AG10	VSS
N3	XIN	AG11	DDR_DQ0
N8	AVDD33_PLL234	AG12	DDR_CLK0_N
N11	DVDD10	AG13	VSS
N12	VSS	AG14	DDR_WE_N
N13	DVDD10	AG15	DDR_A13
N14	VSS	AG16	DDR_A7
N15	DVDD10	AG17	DDR_A5
N16	VSS	AG18	DDR_BA2
N17	DVDD10	AG19	VSS
N21	VSS	AG20	DDR_CLK1_N
N26	VIU0_DAT11	AG21	DDR_DQ16
N27	VIU0_DAT9	AG22	VSS
N28	VIU0_DAT10	AG23	DDR_DQS2_P
P1	UART1_RTSN	AG24	DDR_DQ25
P2	VSS	AG25	DDR_DQ28
P3	VSS	AG26	VSS
P5	UART1_CTSN	AG27	DDR_DQS3_N
P6	UART1_TXD	AG28	DDR_DQ30
P8	AVSS_PLL234	AH1	VSS
P11	VSS	AH2	SFC_WP_IO2
P12	DVDD10	AH4	DDR_DQ12
P13	VSS	AH6	DDR_DQ11
P14	DVDD10	AH8	DDR_DQ8

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Position	Pin Name	Position	Pin Name
P15	VSS	AH10	DDR_DQ2
P16	DVDD10	AH12	DDR_CLK0_P
P17	VSS	AH14	DDR_A0
P21	DVDD33	AH16	DDR_RESET_N
P23	VIU0_DAT6	AH18	DDR_BA0
P24	VIU0_DAT7	AH20	DDR_ODT
P26	VSS	AH22	DDR_DQ19
P27	VIU0_DAT8	AH24	DDR_DQ24
R2	SATA_LED_N1	AH26	DDR_DQ27
R3	UART1_RXD	AH27	DDR_DQS3_P
R5	UART0_RXD	AH28	VSS
R6	UART0_TXD		

2.2 Pin Descriptions

2.2.1 Pin Types

Table 2-3 describes the input/output (I/O) pin types.

Table 2-3 I/O pin types

I/O Type	Description
I	Input signal
I_{PD}	Input signal, internal pull-down
I_{PU}	Input signal, internal pull-up
I_S	Input signal with Schmitt trigger
I_{SPD}	Input signal with Schmitt trigger, internal pull-down
I_{SPU}	Input signal with Schmitt trigger, internal pull-up
O	Output signal
O_{OD}	Output open drain (OD)
I/O	Bidirectional (input/output) signal
I_{PD}/O	Bidirectional signal, input pull-down

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I/O Type	Description
I_{PU}/O	Bidirectional signal, input pull-up
I_{SPU}/O	Bidirectional signal with Schmitt trigger, input pull-up
I_{PD}/O_{OD}	Bidirectional signal, input pull-down and output OD
I_{PU}/O_{OD}	Bidirectional signal, input pull-up and output OD
I_S/O	Bidirectional signal, input with Schmitt trigger
I_S/O_{OD}	Bidirectional signal, input with Schmitt trigger and output OD
CIN	Crystal oscillator input
COUT	Crystal oscillator output
P	Power supply
G	Ground (GND)

2.2.2 DDR Pins

NOTE

Based on the operating mode of the double data rate (DDR), all DDR I/O pins support SSTL_1.8V_ClassI, SSTL_1.8V_ClassII, or SSTL_1.5V.

DDR Power Pins

Table 2-4 describes DDR power pins.

Table 2-4 DDR power pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
AA10, AA11, AA13, AA14, AA17, AA18, AA20	DVDD1518	P	None	1.8/1.5/1.35	I/O power of DDR2, DDR3, or DDR3L

DDR Pins

Table 2-5 describes DDR pins.

Table 2-5 DDR pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
AH14	DDR_A0	O	None	1.5/1.8/1.35	Address signal 0 of the DDR synchronous dynamic random

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
					access memory (SDRAM)
AD15	DDR_A1	O	None	1.5/1.8/1.35	Address signal 1 of the DDR SDRAM
AF15	DDR_A2	O	None	1.5/1.8/1.35	Address signal 2 of the DDR SDRAM
AF17	DDR_A3	O	None	1.5/1.8/1.35	Address signal 3 of the DDR SDRAM
AD18	DDR_A4	O	None	1.5/1.8/1.35	Address signal 4 of the DDR SDRAM
AG17	DDR_A5	O	None	1.5/1.8/1.35	Address signal 5 of the DDR SDRAM
AD17	DDR_A6	O	None	1.5/1.8/1.35	Address signal 6 of the DDR SDRAM
AG16	DDR_A7	O	None	1.5/1.8/1.35	Address signal 7 of the DDR SDRAM
AC14	DDR_A8	O	None	1.5/1.8/1.35	Address signal 8 of the DDR SDRAM
AF16	DDR_A9	O	None	1.5/1.8/1.35	Address signal 9 of the DDR SDRAM
AD12	DDR_A10	O	None	1.5/1.8/1.35	Address signal 10 of the DDR SDRAM
AC17	DDR_A11	O	None	1.5/1.8/1.35	Address signal 11 of the DDR SDRAM
AC12	DDR_A12	O	None	1.5/1.8/1.35	Address signal 12 of the DDR SDRAM
AG15	DDR_A13	O	None	1.5/1.8/1.35	Address signal 13 of the DDR SDRAM
AC15	DDR_A14	O	None	1.5/1.8/1.35	Address signal 14 of the DDR SDRAM
AH18	DDR_BA0	O	None	1.5/1.8/1.35	Bank address signal 0 of the DDR SDRAM
AC18	DDR_BA1	O	None	1.5/1.8/1.35	Bank address signal 1 of the DDR SDRAM
AG18	DDR_BA2	O	None	1.5/1.8/1.35	Bank address signal 2 of the DDR SDRAM
AF14	DDR_CAS_N	O	None	1.5/1.8/1.35	Column address select of the DDR SDRAM

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
AD14	DDR_CKE	O	None	1.5/1.8/1.35	DDR SDRAM clock enable
AG12	DDR_CLK0_N	O	None	1.5/1.8/1.35	Negative differential clock 0 of the DDR SDRAM
AH12	DDR_CLK0_P	O	None	1.5/1.8/1.35	Positive differential clock 0 of the DDR SDRAM
AG20	DDR_CLK1_N	O	None	1.5/1.8/1.35	Negative differential clock 1 of the DDR SDRAM
AF20	DDR_CLK1_P	O	None	1.5/1.8/1.35	Positive differential clock 1 of the DDR SDRAM
AF18	DDR_CS_N	O	None	1.5/1.8/1.35	DDR SDRAM chip select (CS)
AC11	DDR_DM0	I/O	None	1.5/1.8/1.35	Data mask signal 0 of the DDR SDRAM
AG5	DDR_DM1	I/O	None	1.5/1.8/1.35	Data mask signal 1 of the DDR SDRAM
AC21	DDR_DM2	I/O	None	1.5/1.8/1.35	Data mask signal 2 of the DDR SDRAM
AF25	DDR_DM3	I/O	None	1.5/1.8/1.35	Data mask signal 3 of the DDR SDRAM
AG11	DDR_DQ0	I/O	None	1.5/1.8/1.35	Data line 0 of the DDR SDRAM
AF11	DDR_DQ1	I/O	None	1.5/1.8/1.35	Data line 1 of the DDR SDRAM
AH10	DDR_DQ2	I/O	None	1.5/1.8/1.35	Data line 2 the DDR SDRAM
AD11	DDR_DQ3	I/O	None	1.5/1.8/1.35	Data line 3 the DDR SDRAM
AD9	DDR_DQ4	I/O	None	1.5/1.8/1.35	Data line 4 the DDR SDRAM
AD8	DDR_DQ5	I/O	None	1.5/1.8/1.35	Data line 5 the DDR SDRAM
AC9	DDR_DQ6	I/O	None	1.5/1.8/1.35	Data line 6 the DDR SDRAM
AC8	DDR_DQ7	I/O	None	1.5/1.8/1.35	Data line 7 the DDR SDRAM
AH8	DDR_DQ8	I/O	None	1.5/1.8/1.35	Data line 8 the DDR SDRAM
AG8	DDR_DQ9	I/O	None	1.5/1.8/1.35	Data line 9 the DDR SDRAM
AF8	DDR_DQ10	I/O	None	1.5/1.8/1.35	Data line 10 the DDR SDRAM
AH6	DDR_DQ11	I/O	None	1.5/1.8/1.35	Data line 11 the DDR SDRAM
AH4	DDR_DQ12	I/O	None	1.5/1.8/1.35	Data line 12 the DDR SDRAM
AF5	DDR_DQ13	I/O	None	1.5/1.8/1.35	Data line 13 the DDR SDRAM
AG4	DDR_DQ14	I/O	None	1.5/1.8/1.35	Data line 14 the DDR SDRAM

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
AF4	DDR_DQ15	I/O	None	1.5/1.8/1.35	Data line 15 the DDR SDRAM
AG21	DDR_DQ16	I/O	None	1.5/1.8/1.35	Data line 16 the DDR SDRAM
AD20	DDR_DQ17	I/O	None	1.5/1.8/1.35	Data line 17 the DDR SDRAM
AF21	DDR_DQ18	I/O	None	1.5/1.8/1.35	Data line 18 the DDR SDRAM
AH22	DDR_DQ19	I/O	None	1.5/1.8/1.35	Data line 19 the DDR SDRAM
AC20	DDR_DQ20	I/O	None	1.5/1.8/1.35	Data line 20 the DDR SDRAM
AD21	DDR_DQ21	I/O	None	1.5/1.8/1.35	Data line 21 the DDR SDRAM
AD23	DDR_DQ22	I/O	None	1.5/1.8/1.35	Data line 22 the DDR SDRAM
AC23	DDR_DQ23	I/O	None	1.5/1.8/1.35	Data line 23 the DDR SDRAM
AH24	DDR_DQ24	I/O	None	1.5/1.8/1.35	Data line 24 the DDR SDRAM
AG24	DDR_DQ25	I/O	None	1.5/1.8/1.35	Data line 25 the DDR SDRAM
AF24	DDR_DQ26	I/O	None	1.5/1.8/1.35	Data line 26 the DDR SDRAM
AH26	DDR_DQ27	I/O	None	1.5/1.8/1.35	Data line 27 the DDR SDRAM
AG25	DDR_DQ28	I/O	None	1.5/1.8/1.35	Data line 28 the DDR SDRAM
AF27	DDR_DQ29	I/O	None	1.5/1.8/1.35	Data line 29 the DDR SDRAM
AG28	DDR_DQ30	I/O	None	1.5/1.8/1.35	Data line 30 the DDR SDRAM
AE27	DDR_DQ31	I/O	None	1.5/1.8/1.35	Data line 31 the DDR SDRAM
AF9	DDR_DQS0_N	I/O	None	1.5/1.8/1.35	Negative data strobe (DQS) signal 0 of the DDR, corresponding to DQ[7:0]
AG9	DDR_DQS0_P	I/O	None	1.5/1.8/1.35	Positive DQS signal 0 of the DDR, corresponding to DQ[7:0]
AF6	DDR_DQS1_N	I/O	None	1.5/1.8/1.35	Negative DQS signal 1 of the DDR, corresponding to DQ[15:8]
AG6	DDR_DQS1_P	I/O	None	1.5/1.8/1.35	Positive DQS signal 1 of the DDR, corresponding to DQ[15:8]
AF23	DDR_DQS2_N	I/O	None	1.5/1.8/1.35	Negative DQS signal 2 of the DDR, corresponding to DQ[23:16]
AG23	DDR_DQS2_P	I/O	None	1.5/1.8/1.35	Positive DQS signal 2 of the DDR, corresponding to DQ[23:16]
AG27	DDR_DQS3_N	I/O	None	1.5/1.8/1.35	Negative DQS signal 3 of the DDR, corresponding to DQ[31:24]
AH27	DDR_DQS3_P	I/O	None	1.5/1.8/1.35	Positive DQS signal 3 of the DDR,

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
					corresponding to DQ[31:24]
AH20	DDR_ODT	None	None	1.5/1.8/1.35	Connect to an external matched reference resistor
AD24	DDR_PADHI	None	None	1.5/1.8/1.35	Connect to an external pull-down resistor
AE26	DDR_PADLO	None	None	1.5/1.8/1.35	Connect to an external pull-up resistor
AF12	DDR_RAS_N	None	None	1.5/1.8/1.35	Row address select of the DDR SDRAM
AH16	DDR_RESET_N	P	None	1.5/1.8/1.35	Reset signal of the DDR3 SDRAM
AC6	DDR_RTT	None	None	1.5/1.8/1.35	Connect to an external pull-down resistor
AG14	DDR_WE_N	O	None	1.5/1.8/1.35	DDR SDRAM write enable
AA12, AA16, AA19	DDR_REF	P	None	0.5 x DVDD1518	DDR reference voltage

2.2.3 GPIO Pins

Table 2-6 describes general-purpose input/output (GPIO) pins.

Table 2-6 GPIO pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
M1	GPIO11_0	I_{PU}/O	4	3.3	Function 0: GPIO11_0 GPIO Function 1: UART3_RXD Universal asynchronous receiver transmitter 3 (UART3) data receive
M2	GPIO11_1	I_{PU}/O	4	3.3	Function 0: GPIO11_1 GPIO Function 1: UART3_TXD UART3 data transmit

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2.2.4 HDMI Pins

Table 2-7 describes high-definition multimedia interface (HDMI) pins.

Table 2-7 HDMI pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
K21, L21	AVCC10_HDMI	P	None	1.0	HDMI analog power
A27, A28, B26, C26, E26, E27, G26, G27, H23, J21, J23	AVSS_HDMI	G	None	None	HDMI analog GND
E28	HDMI_REXT	None	None	None	Connect to an external resistor. For details, see the *Hi3521 Hardware Design User Guide*.
G28	HDMI_CEC	I_{PU}/O	4	3.3	Function 0: GPIO11_5 GPIO Function 1: HDMI_CEC Channel control signal of the HDMI
J27	HDMI_HOTPLUG	I_{PD}/O	4	3.3	Function 0: GPIO11_4 GPIO Function 1: HDMI_HOTPLUG Hot plug signal of the HDMI
H26	HDMI_SCL	I_{SPU}/O	8	3.3	Function 0: GPIO11_7 GPIO Function 1: HDMI_SCL Dedicated inter-integrated circuit (I^2C) bus clock for the HDMI, OD output
H27	HDMI_SDA	I_{SPU}/O	4	3.3	Function 0: GPIO11_6 GPIO Function 1: HDMI_SDA Dedicated I^2C bus data/address for

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
					the HDMI, OD output
D27	HDMI_TX0N	O	None	0.7	Serial differential signal of channel 0
D26	HDMI_TX0P				
C28	HDMI_TX1N	O	None	0.7	Serial differential signal of channel 1
C27	HDMI_TX1P				
B28	HDMI_TX2N	O	None	0.7	Serial differential signal of channel 2
B27	HDMI_TX2P				
F27	HDMI_TXCN	O	None	0.7	Differential pixel clock
F26	HDMI_TXCP				

2.2.5 I2C Pins

Table 2-8 describes I^2C pins.

Table 2-8 I^2C pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
M23	I2C_SCL	I_{SPU}/O	8	3.3	Function 0: GPIO13_3 GPIO Function 1: I2C_SCL I^2C bus clock, OD output
M24	I2C_SDA	I_{SPU}/O	4	3.3	Function 0: GPIO13_2 GPIO Function 1: I2C_SDA I^2C bus data/address, OD output

2.2.6 IR Pin

Table 2-9 describes the infrared (IR) pin.

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Table 2-9 IR pin

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
L2	IR_IN	I_{SPU}/O	4	3.3	Function 0: IR_IN IR input Function 1: GPIO9_4 GPIO

2.2.7 JTAG Pins

Table 2-10 describes Joint Test Action Group (JTAG) pins.

Table 2-10 JTAG pins

Name	Type	Drive Current (mA)	Voltage (V)	Description	
L3	JTAG_TCK	I_{SPD}	None	3.3	JTAG clock input
J5	JTAG_TDI	I_{SPU}	None	3.3	JTAG data input
J3	JTAG_TDO	O	4	3.3	JTAG data output
K3	JTAG_TMS	I_{SPU}/O	4	3.3	JTAG mode select input or data output for software trace. The modes are controlled by using the CPU.
L5	JTAG_TRSTN	I_{SPD}	None	3.3	JTAG reset input

2.2.8 GMAC Pins

DVDD2533 Pins

Table 2-11 describes DVDD2533 pins.

Table 2-11 DVDD2533 pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
H15, H16, H17	DVDD2533	P	None	3.3/2.5	I/O voltage of the Ethernet port

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MDIO Pins

Table 2-12 describes management data input/output (MDIO) pins.

Table 2-12 MDIO pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
B18	MDCK	I_{SPD}/O	Configurable	3.3/2.5	Function 0: MDCK MDIO clock output Function 1: JTAG_SEL0 JTAG function select. The definitions of {JTAG_SEL1, JTAG_SEL0} are as follows: 00: A9 01: reserved 10: serial advanced technology attachment (SATA) 11: reserved
C18	MDIO	I/O	Configurable	3.3/2.5	MDIO

GMAC Pins

Table 2-13 describes gigabit media access control (GMAC) pins.

Table 2-13 GMAC pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
F18	RGMII_COL	I/O	Configurable	2.5/3.3	Function 0: GPIO13_5 GPIO Function 1: RGMII_COL Collision indicator signal of the reduced gigabit media independent interface (RGMII) Function 2: RGMII_TXER Transmit error signal of the media independent interface (MII)
E18	RGMII_CRS	I/O	Configurable	2.5/3.3	Function 0: GPIO13_4 GPIO Function 1: RGMII_CRS Carrier sense signal of the

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
					RGMII Function 2: RGMII_RXER Receive error signal of the MII
C15	RGMII_RXCK	I	None	2.5/3.3	Receive clock of the RGMII (active on both edges) or MII
B15	RGMII_RXD0	I	None	2.5/3.3	Receive data of the RGMII or MII
A15	RGMII_RXD1	I	None	2.5/3.3	Receive data of the RGMII or MII
F14	RGMII_RXD2	I	None	2.5/3.3	Receive data of the RGMII or MII
E14	RGMII_RXD3	I	None	2.5/3.3	Receive data of the RGMII or MII
C14	RGMII_RXDV	I	None	2.5/3.3	Receive enable of the RGMII or MII
C17	RGMII_TXCK	I/O	Configurable	2.5/3.3	Function 0: RGMII_TXCK Transmit clock of the MII Function 1: GPIO8_7 GPIO
E17	RGMII_TXCKOUT	O	Configurable	2.5/3.3	Gigabit transmit clock of the RGMII, active on both edges
B16	RGMII_TXD0	O	Configurable	2.5/3.3	Function 0: PLL_TEST_OUT0 Phase-locked loop (PLL) test clock output Function 1: RGMII_TXD0 Transmit data of the RGMII or MII Function 2: PLL_TEST_OUT1 PLL test clock output Function 3: PLL_TEST_OUT2 PLL test clock output Function 4: PLL_TEST_OUT3 PLL test clock output
B17	RGMII_TXD1	O	Configurable	2.5/3.3	Transmit data of the RGMII or MII
A17	RGMII_TXD2	O	Configurable	2.5/3.3	Transmit data of the RGMII or MII

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
F15	RGMII_TXD3	O	Configurable	2.5/3.3	Transmit data of the RGMII or MII
E15	RGMII_TXEN	O	Configurable	2.5/3.3	Transmit data enable of the RGMII or MII

2.2.9 NANDC Pins

Table 2-14 describes NAND flash controller (NANDC) pins.

Table 2-14 NANDC pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
Y6	NF_ALE	I_{SPD}/O	8	3.3	Function 0: NF_ALE Address latch signal of the NAND flash Function 1: BOOT_SEL1 Boot mode select. For details, see the description of BOOT_SEL0.
AA5	NF_CLE	I_{SPD}/O	8	3.3	Function 0: NF_CLE Command latch signal of the NAND flash Function 1: BOOT_SEL0 Boot mode select. BOOT_SEL0 works with BOOT_SEL1 for selecting the boot mode. The definitions of {BOOT_SEL1, BOOT_SEL0} are as follows: 00: storage space of the serial peripheral interface (SPI) flash 01: reserved 10: storage space of the NAND flash 11: reserved
AB2	NF_CSN0	O	4	3.3	NAND flash CS0, active low. This pin is used to mount the NAND flash for booting the system.
AB1	NF_CSN1	O	4	3.3	NAND flash CS1, active low. This pin is used to mount the NAND flash for booting the system.
AC5	NF_DQ0	I_{PD}/O	8	3.3	Function 0: NF_DQ0

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
					Data bus of the NAND flash Function 1: GPIO9_5 GPIO
AF1	NF_DQ1	I_{PD}/O	8	3.3	Function 0: NF_DQ1 Data bus of the NAND flash Function 1: GPIO9_6 GPIO
AE3	NF_DQ2	I_{PD}/O	8	3.3	Function 0: NF_DQ2 Data bus of the NAND flash Function 1: GPIO9_7 GPIO
AE2	NF_DQ3	I_{PD}/O	8	3.3	Function 0: NF_DQ3 Data bus of the NAND flash Function 1: GPIO10_0 GPIO
AD3	NF_DQ4	I_{PD}/O	8	3.3	Function 0: NF_DQ4 Data bus of the NAND flash Function 1: GPIO10_1 GPIO
AD2	NF_DQ5	I_{PD}/O	8	3.3	Function 0: NF_DQ5 Data bus of the NAND flash Function 1: GPIO10_2 GPIO
AD1	NF_DQ6	I_{PD}/O	8	3.3	Function 0: NF_DQ6 Data bus of the NAND flash Function 1: GPIO10_3 GPIO
AC3	NF_DQ7	I_{PD}/O	8	3.3	Function 0: NF_DQ7 Data bus of the NAND flash Function 1: GPIO10_4 GPIO
AC2	NF_RDY0	I_{SPU}/O	4	3.3	Function 0: NF_RDY0 Status indicator signal of the NAND flash. 0: busy 1: idle

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
					Function 1: GPIO10_5 GPIO
AB3	NF_RDY1	I_{SPU}/O	4	3.3	Function 0: NF_RDY1 Status indicator signal of the NAND flash. 0: busy 1: idle Function 1: GPIO10_6 GPIO
AA6	NF_REN	I_{SPD}/O	8	3.3	Function 0: NF_REN Read enable signal of the NAND flash, active low Function 1: JTAG_SEL1 JTAG function select. The definitions of {JTAG_SEL1, JTAG_SEL0} are as follows: 00: A9 01: reserved 10: SATA 11: reserved
Y5	NF_WEN	I_{SPD}/O	8	3.3	Function 0: NF_WEN Write enable signal of the NAND flash, active low. Function 1: BOOTROM_SEL BOOTROM boot. When this signal is set to 1, the BOOTROM boot mode is selected. In this case, if the communication over the serial port times out, the boot program is jumped to another storage space based on the values of BOOT_SEL1 and BOOT_SEL0.

2.2.10 SYS Pins

Table 2-15 describes system (SYS) pins.

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Table 2-15 SYS pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
F6	RSTN	I_{SPU}	None	3.3	Reset input during system power-on, active low
E5	TEST_MODE	I_{SPD}	None	3.3	Functional mode and test mode select. 0: functional mode 1: test mode
F5	WDG_RSTN	O_{OD}	4	3.3	Watchdog reset, active low and OD output

2.2.11 SATA Pins

Table 2-16 describes SATA pins.

Table 2-16 SATA pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
T3	SATA_LED_N0	I/O	4	3.3	Function 0: GPIO11_2 GPIO Function 1: SATA_LED_N0 LED indicator of the SATA0 port, active low
R2	SATA_LED_N1	I/O	4	3.3	Function 0: GPIO11_3 GPIO Function 1: SATA_LED_N1 Light emitting diode (LED) indicator of the SATA1 port, active low
V6	SATA_REFCLKM	I	None	0.7	Differential clock input
V5	SATA_REFCLKP	I	None	0.7	Differential clock input
U5	SATA_REXT	I	None	0.7	External resistor with the impedance 191 Ω ±1%
W3	SATA_RX0M	I	None	0.7	Differential signal received by channel 0
W2	SATA_RX0P	I	None	0.7	Differential signal received by channel 0

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
V1	SATA_RX1M	I	None	0.7	Differential signal received by channel 1
V2	SATA_RX1P	I	None	0.7	Differential signal received by channel 1
AA3	SATA_TX0M	O	None	0.7	Differential signal transmitted by channel 0
AA2	SATA_TX0P	O	None	0.7	Differential signal transmitted by channel 0
T2	SATA_TX1M	O	None	0.7	Differential signal transmitted by channel 1
T1	SATA_TX1P	O	None	0.7	Differential signal transmitted by channel 1
V8	SATA_VP10	P	None	1.0	SATA 1.0 V power
W8	SATA_VP25	P	None	2.5	SATA 2.5 V power

2.2.12 SFC Pins

Table 2-17 describes SPI flash controller (SFC) pins.

Table 2-17 SFC pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
AD5	SFC_CLK	O	12	3.3	Clock signal transmitted to the SPI flash. The high level or low level can be configured when the clock is not switched.
AF2	SFC_CS0N	O	4	3.3	SFC CS 0, active low
AG1	SFC_CS1N	O	4	3.3	SFC CS 1, active low. This pin is used to mount the SPI flash for booting the system.
AG3	SFC_DIO	I_{PD}/O	8	3.3	Function 0: SFC_DIO Data output signal in standard SPI mode Data I/O signal in dual SPI mode Data I/O signal in quad SPI mode Function 1: GPIO13_6 GPIO

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
AF3	SFC_DOI	I_{PD}/O	8	3.3	Function 0: SFC_DOI Data input signal in standard SPI mode Data I/O signal in dual SPI mode Data I/O signal in quad SPI mode Function 1: GPIO13_7 GPIO
AG2	SFC_HOLD_IO3	I_{PD}/O	8	3.3	Function 0: SFC_HOLD_IO3 Hold function in standard SPI mode, active low Hold function in dual SPI mode, active low Data I/O signal in quad SPI mode Function 1: GPIO14_4 GPIO
AH2	SFC_WP_IO2	I_{PD}/O	8	3.3	Function 0: SFC_WP_IO2 Write protect function in standard SPI mode, active low Write protect function in dual SPI mode, active low Data I/O signal in quad SPI mode Function 1: GPIO10_7 GPIO

2.2.13 SIO Pins

SIO0 Pins

Table 2-18 describes sonic input/output (SIO) pins.

Table 2-18 SIO0 pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
J28	SIO0_DIN	I_{PU}/O	4	3.3	Function 0: GPIO7_2 GPIO Function 1: SIO0_DIN Data input of the inter-IC sound (I^2S) or pulse code modulation (PCM)

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
					interface
J24	SIO0_RCLK	I_{PD}/O	8	3.3	Function 0: GPIO7_0 GPIO Function 1: SIO0_RCLK Bit stream clock of the I^2S or PCM interface
J26	SIO0_RFS	I_{PD}/O	8	3.3	Function 0: GPIO7_1 GPIO Function 1: SIO0_RFS I^2S receive audio channel select signal (connected to the ADC interface) or PCM frame sync signal

SIO1 Pins

Table 2-19 describes SIO1 pins.

Table 2-19 SIO1 pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
L26	SIO1_DIN	I_{PU}/O	4	3.3	Function 0: GPIO7_5 GPIO Function 1: SIO1_DIN Data input of the I^2S or PCM interface
K27	SIO1_RCLK	I_{PD}/O	8	3.3	Function 0: GPIO7_3 GPIO Function 1: SIO1_RCLK Bit stream clock of the I^2S or PCM interface
L24	SIO1_RFS	I_{PD}/O	8	3.3	Function 0: GPIO7_4 GPIO Function 1: SIO1_RFS I^2S receive audio channel select signal (connected to the ADC interface) or PCM frame sync signal

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SIO2 Pins

Table 2-20 describes SIO2 pins.

Table 2-20 SIO2 pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
F24	SIO2_DIN	I_{PU}/O	4	3.3	Function 0: GPIO8_2 GPIO Function 1: SIO2_DIN Data input of the I^2S or PCM interface
E24	SIO2_DOUT	I_{PU}/O	4	3.3	Function 0: SIO2_DOUT Data output of the I^2S or PCM interface Function 1: NF_BOOT_PIN1 NAND flash type configuration, active only during power-on. For details, see the description of NF_BOOT_PIN0.
A25	SIO2_RCLK	I_{PD}/O	8	3.3	Function 0: GPIO8_0 GPIO Function 1: SIO2_RCLK Bit stream clock of the I^2S or PCM interface
C25	SIO2_RFS	I_{PD}/O	8	3.3	Function 0: GPIO8_1 GPIO Function 1: SIO2_RFS I^2S receive audio channel select signal (connected to the ADC interface) or PCM frame sync signal
B24	SIO2_XCLK	I_{PD}/O	8	3.3	Function 0: GPIO7_6 GPIO Function 1: SIO2_XCLK Bit stream clock of the I^2S or PCM interface
E23	SIO2_XFS	I_{PD}/O	8	3.3	Function 0: GPIO7_7 GPIO Function 1: SIO2_XFS I^2S transmit audio channel select signal (connected to the DAC interface) or PCM frame sync signal

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2.2.14 SPI Pins

Table 2-21 describes SPI pins.

Table 2-21 SPI pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
AE28	SPI_CSN0	I_{PU}/O	4	3.3	Function 0: GPIO8_6 GPIO Function 1: SPI_CSN0 SPI CS 0 output
AD27	SPI_CSN1	I_{SPD}/O	4	3.3	Function 0: SPI_CSN1 SPI CS 1 output Function 1: NF_BOOT_PIN2 NAND flash type configuration, active only during power-on. For details, see the description of NF_BOOT_PIN0.
AC24	SPI_CSN2	I_{SPD}/O	4	3.3	Function 0: SPI_CSN2 SPI CS 0 output Function 1: NF_BOOT_PIN3 NAND flash type configuration, active only during power-on. For details, see the description of NF_BOOT_PIN0.
AD26	SPI_CSN3	I_{SPD}/O	4	3.3	Function 0: SPI_CSN3 SPI CS 1 output Function 1: NF_BOOT_PIN4 NAND flash type configuration, active only during power-on. For details, see the description of NF_BOOT_PIN0. Function 2: CLK_TEST_OUT0 Main test clock output Function 3: CLK_TEST_OUT1 Main test clock output Function 4: CLK_TEST_OUT2 Main test clock output Function 5: CLK_TEST_OUT3 Main test clock output
AC27	SPI_SCLK	I_{PD}/O	12	3.3	Function 0: GPIO8_3 GPIO Function 1: SPI_SCLK SPI clock

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
AC28	SPI_SDI	I_{PD}/O	4	3.3	Function 0: GPIO8_5 GPIO Function 1: SPI_SDI SPI data input
AB27	SPI_SDO	I_{PD}/O	8	3.3	Function 0: GPIO8_4 GPIO Function 1: SPI_SDO SPI data output

2.2.15 UART Pins

UART0 Pins

Table 2-22 describes UART0 pins.

Table 2-22 UART0 pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
R5	UART0_RXD	I_{PU}	None	3.3	UART0 data receive
R6	UART0_TXD	O	4	3.3	UART0 data transmit

UART1 Pins

Table 2-23 describes UART1 pins.

Table 2-23 UART1 pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
P5	UART1_CTSN	I_{PU}/O	4	3.3	Function 0: GPIO9_2 GPIO Function 1: UART1_CTSN Modem state input: clear-to-send, active low
P1	UART1_RTSN	I_{PU}/O	4	3.3	Function 0: GPIO9_0

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
					GPIO Function 1: UART1_RTSN Modem state output: request-to-send, active low. The reset value is 0.
R3	UART1_RXD	I_{PU}/O	4	3.3	Function 0: GPIO9_1 GPIO Function 1: UART1_RXD UART1 data receive
P6	UART1_TXD	I_{PU}/O	4	3.3	Function 0: GPIO9_3 GPIO Function 1: UART1_TXD UART1 data transmit

2.2.16 USB Pins

Table 2-24 describes universal serial bus (USB) pins.

Table 2-24 USB pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
E12, F11	AVDD33_USB	P	None	3.3	USB analog power
B12, B14, C11, C13, F12, H14	AVSS_USB	G	None	None	USB analog GND
H12	DVDD10_USB	P	None	1.0	USB digital power
H13	DVSS_USB	G		None	USB digital GND
C12	USB_REXT	I/O	None	3.3	Connect to an external 43.2 Ω ±1% resistor and then to GND
B11	USB0_DM	I/O	None	0.4/3.3	USB port 0 D- signal. In high-speed mode, the maximum voltage of this port is 800 mV or 400 mV. In full-speed or low-speed mode, the voltage of

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
					this port is 3.3 V.
A11	USB0_DP	I/O	None	0.4/3.3	USB port 0 D+ signal. In high-speed mode, the maximum voltage of this port is 800 mV or 400 mV. In full-speed or low-speed mode, the voltage of this port is 3.3 V.
A9	USB0_OVRCUR	I_{SPD}/O	4	3.3	Function 0: GPIO14_0 GPIO Function 1: USB0_OVRCUR Overcurrent indicator signal of USB port 0, configurable level, and active high by default
C10	USB0_PWREN	I_{PU}/O	4	3.3	Function 0: GPIO14_1 GPIO Function 1: USB0_PWREN Power control output of USB port 0, configurable level, and active high by default
A13	USB1_DM	I/O	None	0.4/3.3	USB port 1 D- signal. In high-speed mode, the maximum voltage of this port is 800 mV or 400 mV. In full-speed or low-speed mode, the voltage of this port is 3.3 V.
B13	USB1_DP	I/O	None	0.4/3.3	USB port 1 D+ signal. In high-speed mode, the maximum voltage of this port is 800 mV or 400 mV. In full-speed or low-speed mode, the voltage of this port is 3.3 V.
B10	USB1_OVRCUR	I_{SPD}/O	4	3.3	Function 0: GPIO14_2 GPIO Function 1: USB1_OVRCUR Overcurrent indicator signal of USB port 1, configurable level, and active high by default
E11	USB1_PWREN	I_{PU}/O	4	3.3	Function 0: GPIO14_3 GPIO Function 1: USB1_PWREN Power control output of USB port 1, configurable level, and active

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
					high by default

2.2.17 VDAC Pins

VDAC0 Pins

Table 2-25 describes video digital-to-analog converter 0 (VDAC0) pins.

Table 2-25 VDAC0 pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
F20, H19	AVDD33_VDAC0	P	None	3.3	VDAC0 analog power
H20	AGND_VDAC0	G	None	None	VDAC0 analog GND
B21	VDAC0_IOUT0	O	None	3.3	Composite video broadcast signal 0 (CVBS0) channel output
A21	VDAC0_IOUT1	O	None	3.3	CVBS1 channel output
B20	VDAC0_IOUT2	None	None	3.3	Connect to an external 75 Ω resistor and then to GND
C21	VDAC0_IREF	I/O	None	3.3	Reference current. When an external resistor is connected, the current is output; when an external power supply is connected, the current is input.
C20	VDAC0_VDREF	I/O	None	3.3	External decoupling reference voltage, for connecting to a 10 nF and a 1 nF capacitors and then to the analog GND.

VDAC1 Pins

Table 2-26 describes VDAC1 pins.

Table 2-26 VDAC1 pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
E20, E21	AVDD33_VDAC1	P	None	3.3	VDAC1 analog power

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
F21	AGND_VDAC1	G	None	None	VDAC1 analog GND
B23	VDAC1_IOUT0	O	None	3.3	B channel output of the video graphics array (VGA)
A23	VDAC1_IOUT1	O	None	3.3	G channel output of the VGA
B22	VDAC1_IOUT2	O	None	3.3	R channel output of the VGA
C23	VDAC1_IREF	I/O	None	3.3	Reference current. When an external resistor is connected, the current is output; when an external power supply is connected, the current is input.
C22	VDAC1_VDREF	I/O	None	3.3	External decoupling reference voltage, for connecting to a 10 nF and a 1 nF capacitors and then to the analog GND.

2.2.18 VIU Pins

VIU0 Pins

Table 2-27 describes video input unit 0 (VIU0) pins.

Table 2-27 VIU0 pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
T26	VIU0_CLK	I_{PD}/O	4	3.3	Function 0: VIU0_CLK VIU0 clock Function 1: GPIO12_0 GPIO
T27	VIU0_DAT0	I_{PD}/O	4	3.3	Function 0: VIU0_DAT0 VIU0 data input Function 1: GPIO1_7 GPIO
R23	VIU0_DAT1	I_{PD}/O	4	3.3	Function 0: VIU0_DAT1 VIU0 data input Function 1: GPIO1_6 GPIO

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
R24	VIU0_DAT2	I_{PD}/O	4	3.3	Function 0: VIU0_DAT2 VIU0 data input Function 1: GPIO1_5 GPIO
R26	VIU0_DAT3	I_{PD}/O	4	3.3	Function 0: VIU0_DAT3 VIU0 data input Function 1: GPIO1_4 GPIO
R28	VIU0_DAT4	I_{PD}/O	4	3.3	Function 0: VIU0_DAT4 VIU0 data input Function 1: GPIO1_3 GPIO
R27	VIU0_DAT5	I_{PD}/O	4	3.3	Function 0: VIU0_DAT5 VIU0 data input Function 1: GPIO1_2 GPIO
P23	VIU0_DAT6	I_{PD}/O	4	3.3	Function 0: VIU0_DAT6 VIU0 data input Function 1: GPIO1_1 GPIO
P24	VIU0_DAT7	I_{PD}/O	4	3.3	Function 0: VIU0_DAT7 VIU0 data input Function 1: GPIO1_0 GPIO
P27	VIU0_DAT8	I_{PD}/O	4	3.3	Function 0: VIU0_DAT8 VIU0 data input Function 1: GPIO0_7 GPIO
N27	VIU0_DAT9	I_{PD}/O	4	3.3	Function 0: VIU0_DAT9 VIU0 data input Function 1: GPIO0_6 GPIO
N28	VIU0_DAT10	I_{PD}/O	4	3.3	Function 0: VIU0_DAT10 VIU0 data input Function 1: GPIO0_5 GPIO

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
N26	VIU0_DAT11	I_{PD}/O	4	3.3	Function 0: VIU0_DAT11 VIU0 data input Function 1: GPIO0_4 GPIO
M27	VIU0_DAT12	I_{PD}/O	4	3.3	Function 0: VIU0_DAT12 VIU0 data input Function 1: GPIO0_3 GPIO
M26	VIU0_DAT13	I_{PD}/O	4	3.3	Function 0: VIU0_DAT13 VIU0 data input Function 1: GPIO0_2 GPIO
L28	VIU0_DAT14	I_{PD}/O	4	3.3	Function 0: VIU0_DAT14 VIU0 data input Function 1: GPIO0_1 GPIO
L27	VIU0_DAT15	I_{PD}/O	4	3.3	Function 0: VIU0_DAT15 VIU0 data input Function 1: GPIO0_0 GPIO
U23	VIU0_HS	I_{PU}/O	4	3.3	Function 0: VIU0_HS VIU0 horizontal sync, active high Function 1: GPIO12_3 GPIO Function 2: UART2_RXD UART2 data receive
U24	VIU0_VS	I_{PD}/O	4	3.3	Function 0: VIU0_VS VIU0 vertical sync, active high Function 1: GPIO12_2 GPIO Function 2: VIU0_CLKA VIU0 clock

VIU1 Pins

Table 2-28 describes VIU1 pins.

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Table 2-28 VIU1 pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
AB26	VIU1_CLK	I_{PD}/O	4	3.3	Function 0: VIU1_CLK VIU1 clock Function 1: GPIO12_1 GPIO
AA28	VIU1_DAT0	I_{PD}/O	4	3.3	Function 0: VIU1_DAT0 VIU1 data input Function 1: GPIO3_7 GPIO
AA27	VIU1_DAT1	I_{PD}/O	4	3.3	Function 0: VIU1_DAT1 VIU1 data input Function 1: GPIO3_6 GPIO
AA26	VIU1_DAT2	I_{PD}/O	4	3.3	Function 0: VIU1_DAT2 VIU1 data input Function 1: GPIO3_5 GPIO
Y23	VIU1_DAT3	I_{PD}/O	4	3.3	Function 0: VIU1_DAT3 VIU1 data input Function 1: GPIO3_4 GPIO
Y24	VIU1_DAT4	I_{PD}/O	4	3.3	Function 0: VIU1_DAT4 VIU1 data input Function 1: GPIO3_3 GPIO
Y27	VIU1_DAT5	I_{PD}/O	4	3.3	Function 0: VIU1_DAT5 VIU1 data input Function 1: GPIO3_2 GPIO
Y26	VIU1_DAT6	I_{PD}/O	4	3.3	Function 0: VIU1_DAT6 VIU1 data input Function 1: GPIO3_1 GPIO
W28	VIU1_DAT7	I_{PD}/O	4	3.3	Function 0: VIU1_DAT7 VIU1 data input Function 1: GPIO3_0

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
					GPIO
W27	VIU1_DAT8	I_{PD}/O	4	3.3	Function 0: VIU1_DAT8 VIU1 data input Function 1: GPIO2_7 GPIO
W26	VIU1_DAT9	I_{PD}/O	4	3.3	Function 0: VIU1_DAT9 VIU1 data input Function 1: GPIO2_6 GPIO
V23	VIU1_DAT10	I_{PD}/O	4	3.3	Function 0: VIU1_DAT10 VIU1 data input Function 1: GPIO2_5 GPIO
V24	VIU1_DAT11	I_{PD}/O	4	3.3	Function 0: VIU1_DAT11 VIU1 data input Function 1: GPIO2_4 GPIO
V27	VIU1_DAT12	I_{PD}/O	4	3.3	Function 0: VIU1_DAT12 VIU1 data input Function 1: GPIO2_3 GPIO
V26	VIU1_DAT13	I_{PD}/O	4	3.3	Function 0: VIU1_DAT13 VIU1 data input Function 1: GPIO2_2 GPIO
U28	VIU1_DAT14	I_{PD}/O	4	3.3	Function 0: VIU1_DAT14 VIU1 data input Function 1: GPIO2_1 GPIO
U27	VIU1_DAT15	I_{PD}/O	4	3.3	Function 0: VIU1_DAT15 VIU1 data input Function 1: GPIO2_0 GPIO
AA23	VIU1_HS	I_{PU}/O	4	3.3	Function 0: VIU1_HS VIU1 horizontal sync, active high Function 1: GPIO12_5

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
					GPIO Function 2: UART2_TXD UART2 data transmit
AA24	VIU1_VS	I_{PD}/O	4	3.3	Function 0: VIU1_VS VIU1 vertical sync, active high Function 1: GPIO12_4 GPIO Function 2: VIU1_CLKA VIU1 clock

2.2.19 VOU Pins

Table 2-29 describes video output unit (VOU) pins.

Table 2-29 VOU pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
E2	LCD_DV	I_{SPU}/O	8	3.3	Function 0: LCD_DV Data validity output of the liquid crystal display (LCD) interface, active high Function 1: NF_BOOT_PIN0 NAND flash type configuration, active only during power-on. NF_BOOT_PIN0, NF_BOOT_PIN1, NF_BOOT_PIN2, NF_BOOT_PIN3, and NF_BOOT_PIN4 work together for setting the PAGE_SEIZE, ECC_TYPE, BLOCK_SIZE, and ADDR_NUM parameters of the connected NAND flash. For details, see "Mapping Between Pin Values and NAND Flash Types" in section 4.2.3.3.
E9	VGA_HS	I/O	8	3.3	Function 0: GPIO13_0 GPIO Function 1: VOU1120_HS Horizontal sync output of the BT.1120 interface Function 2: VGA_HS VGA horizontal sync output

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
F9	VGA_VS	I/O	8	3.3	Function 0: GPIO13_1 GPIO Function 1: VOU1120_VS Vertical sync output of the BT.1120 interface Function 2: VGA_VS VGA vertical sync output
B6	VOU1120_CLK	I/O	Configurable	3.3	Function 0: GPIO12_6 GPIO Function 1: VOU1120_CLK Clock output of the BT.1120 interface Function 2: LCD_CLK Clock output of the LCD interface
E3	VOU1120_DATA0	I_{PD}/O	8	3.3	Function 0: GPIO5_7 GPIO Function 1: VOU1120_DATA0 Data output of the BT.1120 interface Function 2: LCD_DATA_B7 B component output of the LCD interface
D2	VOU1120_DATA1	I_{PD}/O	8	3.3	Function 0: GPIO5_6 GPIO Function 1: VOU1120_DATA1 Data output of the BT.1120 interface Function 2: LCD_DATA_B6 B component output of the LCD interface
D1	VOU1120_DATA2	I_{PD}/O	8	3.3	Function 0: GPIO5_5 GPIO Function 1: VOU1120_DATA2 Data output of the BT.1120 interface Function 2: LCD_DATA_B5 B component output of the LCD interface
D3	VOU1120_DATA3	I_{PD}/O	8	3.3	Function 0: GPIO5_4 GPIO Function 1: VOU1120_DATA3 Data output of the BT.1120 interface Function 2: LCD_DATA_B4 B component output of the LCD interface

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
C2	VOU1120_DATA4	I_{PD}/O	8	3.3	Function 0: GPIO5_3 GPIO Function 1: VOU1120_DATA4 Data output of the BT.1120 interface Function 2: LCD_DATA_B3 B component output of the LCD interface
C3	VOU1120_DATA5	I_{PD}/O	8	3.3	Function 0: GPIO5_2 GPIO Function 1: VOU1120_DATA5 Data output of the BT.1120 interface Function 2: LCD_DATA_B2 B component output of the LCD interface
B1	VOU1120_DATA6	I_{PD}/O	8	3.3	Function 0: GPIO5_1 GPIO Function 1: VOU1120_DATA6 Data output of the BT.1120 interface Function 2: LCD_DATA_B1 B component output of the LCD interface
B2	VOU1120_DATA7	I_{PD}/O	8	3.3	Function 0: GPIO5_0 GPIO Function 1: VOU1120_DATA7 Data output of the BT.1120 interface Function 2: LCD_DATA_B0 B component output of the LCD interface
A2	VOU1120_DATA8	I_{PD}/O	8	3.3	Function 0: GPIO4_7 GPIO Function 1: VOU1120_DATA8 Data output of the BT.1120 interface Function 2: LCD_DATA_G7 G component output of the LCD interface
B3	VOU1120_DATA9	I_{PD}/O	8	3.3	Function 0: GPIO4_6 GPIO Function 1: VOU1120_DATA9 Data output of the BT.1120 interface Function 2: LCD_DATA_G6 G component output of the LCD interface

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
A3	VOU1120_DATA10	I_{PD}/O	8	3.3	Function 0: GPIO4_5 GPIO Function 1: VOU1120_DATA10 Data output of the BT.1120 interface Function 2: LCD_DATA_G5 G component output of the LCD interface
C4	VOU1120_DATA11	I_{PD}/O	8	3.3	Function 0: GPIO4_4 GPIO Function 1: VOU1120_DATA11 Data output of the BT.1120 interface Function 2: LCD_DATA_G4 G component output of the LCD interface
B4	VOU1120_DATA12	I_{PD}/O	8	3.3	Function 0: GPIO4_3 GPIO Function 1: VOU1120_DATA12 Data output of the BT.1120 interface Function 2: LCD_DATA_G3 G component output of the LCD interface
C5	VOU1120_DATA13	I_{PD}/O	8	3.3	Function 0: GPIO4_2 GPIO Function 1: VOU1120_DATA13 Data output of the BT.1120 interface Function 2: LCD_DATA_G2 G component output of the LCD interface
A5	VOU1120_DATA14	I_{PD}/O	8	3.3	Function 0: GPIO4_1 GPIO Function 1: VOU1120_DATA14 Data output of the BT.1120 interface Function 2: LCD_DATA_G1 G component output of the LCD interface
B5	VOU1120_DATA15	I_{PD}/O	8	3.3	Function 0: GPIO4_0 GPIO Function 1: VOU1120_DATA15 Data output of the BT.1120 interface Function 2: LCD_DATA_G0 G component output of the LCD interface

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
E8	VOU656_CLK	I_{PD}/O	12	3.3	Function 0: GPIO12_7 GPIO Function 1: VOU656_CLK Clock output of the BT.656 interface Function 3: SDIO_CCLK_OUT Working clock output of the SDIO card
A7	VOU656_DATA0	I_{PU}/O	8	3.3	Function 0: GPIO6_7 GPIO Function 1: VOU656_DATA0 Data output of the BT.656 interface Function 2: LCD_DATA_R7 R component output of the LCD interface Function 3: SDIO_CDATA0 Data bus of the SDIO card
B7	VOU656_DATA1	I_{PU}/O	8	3.3	Function 0: GPIO6_6 GPIO Function 1: VOU656_DATA1 Data output of the BT.656 interface Function 2: LCD_DATA_R6 R component output of the LCD interface Function 3: SDIO_CDATA1 Data bus of the SDIO card
C7	VOU656_DATA2	I_{PU}/O	8	3.3	Function 0: GPIO6_5 GPIO Function 1: VOU656_DATA2 Data output of the BT.656 interface Function 2: LCD_DATA_R5 R component output of the LCD interface Function 3: SDIO_CDATA2 Data bus of the SDIO card
B8	VOU656_DATA3	I_{PU}/O	8	3.3	Function 0: GPIO6_4 GPIO Function 1: VOU656_DATA3 Data output of the BT.656 interface Function 2: LCD_DATA_R4 R component output of the LCD interface Function 3: SDIO_CDATA3

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
					Data bus of the SDIO card
C8	VOU656_DATA4	I_{PU}/O	8	3.3	Function 0: GPIO6_3 GPIO Function 1: VOU656_DATA4 Data output of the BT.656 interface Function 2: LCD_DATA_R3 R component output of the LCD interface Function 3: SDIO_CCMD SDIO card command
F8	VOU656_DATA5	I_{PU}/O	8	3.3	Function 0: GPIO6_2 GPIO Function 1: VOU656_DATA5 Data output of the BT.656 interface Function 2: LCD_DATA_R2 R component output of the LCD interface Function 3: SDIO_CWPR Write protection signal input of the SDIO card
B9	VOU656_DATA6	I_{PU}/O	8	3.3	Function 0: GPIO6_1 GPIO Function 1: VOU656_DATA6 Data output of the BT.656 interface Function 2: LCD_DATA_R1 R component output of the LCD interface Function 3: SDIO_CARD_DETECT SDIO card detection input, active low
C9	VOU656_DATA7	I_{PD}/O	8	3.3	Function 0: GPIO6_0 GPIO Function 1: VOU656_DATA7 Data output of the BT.656 interface Function 2: LCD_DATA_R0 R component output of the LCD interface Function 3: SDIO_CARD_POWER_EN Power enable control output of the SDIO card. The value 1 indicates power-on.

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2.2.20 OSC Pins

Table 2-30 describes oscillator (OSC) pins.

Table 2-30 OSC pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
N3	XIN	CIN	None	3.3	Crystal input
N2	XOUT	COUT	None	3.3	Crystal output

2.2.21 eFUSE Pin

Table 2-31 describes the eFUSE pin.

Table 2-31 eFUSE pin

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
U8	VDD25_EFUSE	P	None	2.5	2.5 V eFUSE power **Note: Never supply power to this pin. For details about hardware design, see the *Hi3521/Hi3520A Hardware Design User Guide***

2.2.22 PLL Pins

Table 2-32 describes PLL pins.

Table 2-32 PLL pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
M8	AVDD33_PLL1	P	None	3.3	PLL1 analog power
N8	AVDD33_PLL234	P	None	3.3	Analog power of PLL2, PLL3, or PLL4
L8	AVSS_PLL1	G	None	None	PLL1 analog GND
P8	AVSS_PLL234	G	None	None	Analog GND of PLL2, PLL3, or PLL4
M6	VDD10_PLL1	P	None	1.0	PLL1 digital power
M5	VDD10_PLL234	P	None	1.0	Digital power of PLL2, PLL3, or PLL4

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L6	VDDREF10_PLL234	P	None	1.0	Digital reference power of PLL2, PLL3, or PLL4

2.2.23 Power Pins and GND Pins

DVDD10 Power Pins

Table 2-33 describes DVDD10 pins.

Table 2-33 DVDD10 pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
M12, M14, M16, N11, N13, N15, N17, P12, P14, P16, R11, R13, R15, R17, T12, T14, T16, U11, U13, U15, U17, V12, V14, V16	DVDD10	P	None	1.0	Core voltage

DVDD33 Power Pins

Table 2-34 describes DVDD33 pins.

Table 2-34 DVDD33 pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
H8, H9, H10, H21, K8, M21, P21, R8, R21, U21, V21, Y21, AA8, AA9	DVDD33	P	None	3.3	Digital I/O voltage

VSS Pins

Table 2-35 describes VSS pins.

Table 2-35 VSS pins

Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
A1, A19, B19, B25, C6, C16, C19, C24, E6, F3, F17, F23, G2, G3, H11, H18, H24, J2, J6, J8, K26, L23, M3, M11, M13, M15, M17,	VSS	G	None	None	Digital GND

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Position	Name	Type	Drive Current (mA)	Voltage (V)	Description
N12, N14, N16, N21, P2, P3, P11, P13, P15, P17, P26, R12, R14, R16, T8, T11, T13, T15, T17, T21, U2, U3, U6, U12, U14, U16, U26, V3, V11, V13, V15, V17, W21, Y1, Y2, Y3, Y8, AA15, AA21, AC26, AD6, AF7, AF10, AF13, AF19, AF22, AF26, AG7, AG10, AG13, AG19, AG22, AG26, AH1, AH28					

2.3 I/O Config Registers

2.3.1 Summary of Multiplexing Control Registers

Table 2-36 describes multiplexing control registers.

Table 2-36 Summary of multiplexing control registers (base address:0x200F_0000)

Offset Address	Register	Description	Page
0x000	muxctrl_reg0	Multiplexing control register for the VIU0_CLK pin	2-56
0x004	muxctrl_reg1	Multiplexing control register for the VIU0_VS pin	2-57
0x008	muxctrl_reg2	Multiplexing control register for the VIU0_HS pin	2-57
0x00C	muxctrl_reg3	Multiplexing control register for the VIU0_DAT15 pin	2-58
0x010	muxctrl_reg4	Multiplexing control register for the VIU0_DAT14 pin	2-58
0x014	muxctrl_reg5	Multiplexing control register for the VIU0_DAT13 pin	2-42
0x018	muxctrl_reg6	Multiplexing control register for the VIU0_DAT12 pin	2-59
0x01C	muxctrl_reg7	Multiplexing control register for the VIU0_DAT11 pin	2-60
0x020	muxctrl_reg8	Multiplexing control register for the VIU0_DAT10 pin	2-60
0x024	muxctrl_reg9	Multiplexing control register for the VIU0_DAT9 pin	2-61

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Offset Address	Register	Description	Page
0x028	muxctrl_reg10	Multiplexing control register for the VIU0_DAT8 pin	2-61
0x02C	muxctrl_reg11	Multiplexing control register for the VIU0_DAT7 pin	2-62
0x030	muxctrl_reg12	Multiplexing control register for the VIU0_DAT6 pin	2-62
0x034	muxctrl_reg13	Multiplexing control register for the VIU0_DAT5 pin	2-63
0x038	muxctrl_reg14	Multiplexing control register for the VIU0_DAT4 pin	2-63
0x03C	muxctrl_reg15	Multiplexing control register for the VIU0_DAT3 pin	2-64
0x040	muxctrl_reg16	Multiplexing control register for the VIU0_DAT2 pin	2-64
0x044	muxctrl_reg17	Multiplexing control register for the VIU0_DAT1 pin	2-65
0x048	muxctrl_reg18	Multiplexing control register for the VIU0_DAT0 pin	2-65
0x04C	muxctrl_reg19	Multiplexing control register for the VIU1_CLK pin	2-66
0x050	muxctrl_reg20	Multiplexing control register for the VIU1_VS pin	2-66
0x054	muxctrl_reg21	Multiplexing control register for the VIU1_HS pin	2-48
0x058	muxctrl_reg22	Multiplexing control register for the VIU1_DAT15 pin	2-67
0x05C	muxctrl_reg23	Multiplexing control register for the VIU1_DAT14 pin	2-68
0x060	muxctrl_reg24	Multiplexing control register for the VIU1_DAT13 pin	2-68
0x064	muxctrl_reg25	Multiplexing control register for the VIU1_DAT12 pin	2-69
0x068	muxctrl_reg26	Multiplexing control register for the VIU1_DAT11 pin	2-69
0x06C	muxctrl_reg27	Multiplexing control register for the VIU1_DAT10 pin	2-70
0x070	muxctrl_reg28	Multiplexing control register for the VIU1_DAT9 pin	2-70

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Offset Address	Register	Description	Page
0x074	muxctrl_reg29	Multiplexing control register for the VIU1_DAT8 pin	2-48
0x078	muxctrl_reg30	Multiplexing control register for the VIU1_DAT7 pin	2-71
0x07C	muxctrl_reg31	Multiplexing control register for the VIU1_DAT6 pin	2-72
0x080	muxctrl_reg32	Multiplexing control register for the VIU1_DAT5 pin	2-72
0x084	muxctrl_reg33	Multiplexing control register for the VIU1_DAT4 pin	2-73
0x088	muxctrl_reg34	Multiplexing control register for the VIU1_DAT3 pin	2-73
0x08C	muxctrl_reg35	Multiplexing control register for the VIU1_DAT2 pin	2-74
0x090	muxctrl_reg36	Multiplexing control register for the VIU1_DAT1 pin	2-48
0x094	muxctrl_reg37	Multiplexing control register for the VIU1_DAT0 pin	2-75
0x098	muxctrl_reg38	Multiplexing control register for the VOU1120_CLK pin	2-75
0x09C	muxctrl_reg39	Multiplexing control register for the VOU1120_DATA15 pin	2-76
0x0A0	muxctrl_reg40	Multiplexing control register for the VOU1120_DATA14 pin	2-76
0x0A4	muxctrl_reg41	Multiplexing control register for the VOU1120_DATA13 pin	2-77
0x0A8	muxctrl_reg42	Multiplexing control register for the VOU1120_DATA12 pin	2-77
0x0AC	muxctrl_reg43	Multiplexing control register for the VOU1120_DATA11 pin	2-78
0x0B0	muxctrl_reg44	Multiplexing control register for the VOU1120_DATA10 pin	2-49
0x0B4	muxctrl_reg45	Multiplexing control register for the VOU1120_DATA9 pin	2-79
0x0B8	muxctrl_reg46	Multiplexing control register for the VOU1120_DATA8 pin	2-79
0x0BC	muxctrl_reg47	Multiplexing control register for the VOU1120_DATA7 pin	2-80

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Offset Address	Register	Description	Page
0x0C0	muxctrl_reg48	Multiplexing control register for the VOU1120_DATA6 pin	2-80
0x0C4	muxctrl_reg49	Multiplexing control register for the VOU1120_DATA5 pin	2-81
0x0C8	muxctrl_reg50	Multiplexing control register for the VOU1120_DATA4 pin	2-81
0x0CC	muxctrl_reg51	Multiplexing control register for the VOU1120_DATA3 pin	2-82
0x0D0	muxctrl_reg52	Multiplexing control register for the VOU1120_DATA2 pin	2-49
0x0D4	muxctrl_reg53	Multiplexing control register for the VOU1120_DATA1 pin	2-83
0x0D8	muxctrl_reg54	Multiplexing control register for the VOU1120_DATA0 pin	2-83
0x0DC	muxctrl_reg55	Multiplexing control register for the VGA_HS pin	2-84
0x0E0	muxctrl_reg56	Multiplexing control register for the VGA_VS pin	2-84
0x0E4	muxctrl_reg57	Multiplexing control register for the VOU656_CLK pin	2-85
0x0E8	muxctrl_reg58	Multiplexing control register for the VOU656_DATA7 pin	2-85
0x0EC	muxctrl_reg59	Multiplexing control register for the VOU656_DATA6 pin	2-86
0x0F0	muxctrl_reg60	Multiplexing control register for the VOU656_DATA5 pin	2-86
0x0F4	muxctrl_reg61	Multiplexing control register for the VOU656_DATA4 pin	2-87
0x0F8	muxctrl_reg62	Multiplexing control register for the VOU656_DATA3 pin	2-49
0x0FC	muxctrl_reg63	Multiplexing control register for the VOU656_DATA2 pin	2-88
0x100	muxctrl_reg64	Multiplexing control register for the VOU656_DATA1 pin	2-88
0x104	muxctrl_reg65	Multiplexing control register for the VOU656_DATA0 pin	2-89
0x108	muxctrl_reg66	Multiplexing control register for the SIO0_RCLK pin	2-89

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Offset Address	Register	Description	Page
0x10C	muxctrl_reg67	Multiplexing control register for the SIO0_RFS pin	2-90
0x110	muxctrl_reg68	Multiplexing control register for the SIO0_DIN pin	2-90
0x114	muxctrl_reg69	Multiplexing control register for the SIO1_RCLK pin	2-152
0x118	muxctrl_reg70	Multiplexing control register for the SIO1_RFS pin	2-91
0x11C	muxctrl_reg71	Multiplexing control register for the SIO1_DIN pin	2-92
0x120	muxctrl_reg72	Multiplexing control register for the SIO2_XCLK pin	2-92
0x124	muxctrl_reg73	Multiplexing control register for the SIO2_XFS pin	2-93
0x128	muxctrl_reg74	Multiplexing control register for the SIO2_RCLK pin	2-93
0x12C	muxctrl_reg75	Multiplexing control register for the SIO2_RFS pin	2-94
0x130	muxctrl_reg76	Multiplexing control register for the SIO2_DIN pin	2-94
0x134	muxctrl_reg77	Multiplexing control register for the SPI_SCLK pin	2-95
0x138	muxctrl_reg78	Multiplexing control register for the SPI_SDO pin	2-95
0x13C	muxctrl_reg79	Multiplexing control register for the SPI_SDI pin	2-96
0x140	muxctrl_reg80	Multiplexing control register for the SPI_CSN0 pin	2-96
0x144	muxctrl_reg81	Multiplexing control register for the SPI_CSN3 pin	2-97
0x148	muxctrl_reg82	Multiplexing control register for the I2C_SDA pin	2-97
0x14C	muxctrl_reg83	Multiplexing control register for the I2C_SCL pin	2-98
0x150	muxctrl_reg84	Multiplexing control register for the UART1_RTSN pin	2-98
0x154	muxctrl_reg85	Multiplexing control register for the UART1_RXD pin	2-99

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Offset Address	Register	Description	Page
0x158	muxctrl_reg86	Multiplexing control register for the UART1_CTSN pin	2-99
0x15C	muxctrl_reg87	Multiplexing control register for the UART1_TXD pin	2-100
0x160	muxctrl_reg88	Multiplexing control register for the RGMII_TXD0 pin	2-100
0x164	muxctrl_reg89	Multiplexing control register for the RGMII_TXCK pin	2-101
0x168	muxctrl_reg90	Multiplexing control register for the RGMII_CRS pin	2-101
0x16C	muxctrl_reg91	Multiplexing control register for the RGMII_COL pin	2-102
0x170	muxctrl_reg92	Multiplexing control register for the IR_IN pin	2-102
0x174	muxctrl_reg93	Multiplexing control register for the NF_DQ0 pin	2-103
0x178	muxctrl_reg94	Multiplexing control register for the NF_DQ1 pin	2-103
0x17C	muxctrl_reg95	Multiplexing control register for the NF_DQ2 pin	2-104
0x180	muxctrl_reg96	Multiplexing control register for the NF_DQ3 pin	2-104
0x184	muxctrl_reg97	Multiplexing control register for the NF_DQ4 pin	2-105
0x188	muxctrl_reg98	Multiplexing control register for the NF_DQ5 pin	2-105
0x18C	muxctrl_reg99	Multiplexing control register for the NF_DQ6 pin	2-106
0x190	muxctrl_reg100	Multiplexing control register for the NF_DQ7 pin	2-106
0x194	muxctrl_reg101	Multiplexing control register for the NF_RDY0 pin	2-107
0x198	muxctrl_reg102	Multiplexing control register for the NF_RDY1 pin	2-107
0x19C	muxctrl_reg103	Multiplexing control register for the SFC_DIO pin	2-108
0x1A0	muxctrl_reg104	Multiplexing control register for the SFC_WP_IO2 pin	2-108

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Offset Address	Register	Description	Page
0x1A4	muxctrl_reg105	Multiplexing control register for the SFC_DOI pin	2-109
0x1A8	muxctrl_reg106	Multiplexing control register for the SFC_HOLD_IO3 pin	2-109
0x1AC	muxctrl_reg107	Multiplexing control register for the USB0_OVRCUR pin	2-110
0x1B0	muxctrl_reg108	Multiplexing control register for the USB0_PWREN pin	2-110
0x1B4	muxctrl_reg109	Multiplexing control register for the USB1_OVRCUR pin	2-111
0x1B8	muxctrl_reg110	Multiplexing control register for the USB1_PWREN pin	2-111
0x1BC	muxctrl_reg111	Multiplexing control register for the GPIO11_0 pin	2-112
0x1C0	muxctrl_reg112	Multiplexing control register for the GPIO11_1 pin	2-112
0x1C4	muxctrl_reg113	Multiplexing control register for the SATA_LED_N0 pin	2-113
0x1C8	muxctrl_reg114	Multiplexing control register for the SATA_LED_N1 pin	2-113
0x1CC	muxctrl_reg115	Multiplexing control register for the HDMI_HOTPLUG pin	2-114
0x1D0	muxctrl_reg116	Multiplexing control register for the HDMI_CEC pin	2-114
0x1D4	muxctrl_reg117	Multiplexing control register for the HDMI_SDA pin	2-115
0x1D8	muxctrl_reg118	Multiplexing control register for the HDMI_SCL pin	2-115

2.3.2 Descriptions of Multiplexing Control Registers

muxctrl_reg0

muxctrl_reg0 is the multiplexing control register for the VIU0_CLK pin.

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Offset Address	Register Name	Total Reset Value
0x000	muxctrl_reg0	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg0	Multiplexing control for the VIU0_CLK pin. 0: VIU0_CLK 1: GPIO12_0

muxctrl_reg1

muxctrl_reg1 is the multiplexing control register for the VIU0_VS pin.

Offset Address	Register Name	Total Reset Value
0x004	muxctrl_reg1	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg1
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg1	Multiplexing control for the VIU0_VS pin. 00: VIU0_VS 01: GPIO12_2 10: VIU0_CLKA Other values: reserved

muxctrl_reg2

muxctrl_reg2 is the multiplexing control register for the VIU0_HS pin.

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Offset Address	Register Name	Total Reset Value
0x008	muxctrl_reg2	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg2	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg2	Multiplexing control for the VIU0_HS pin. 00: VIU0_HS 01: GPIO12_3 10: UART2_RXD Other values: reserved

muxctrl_reg3

muxctrl_reg3 is the multiplexing control register for the VIU0_DAT15 pin.

Offset Address	Register Name	Total Reset Value
0x00C	muxctrl_reg3	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg3
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg3	Multiplexing control for the VIU0_DAT15 pin. 0: VIU0_DAT15 1: GPIO0_0

muxctrl_reg4

muxctrl_reg4 is the multiplexing control register for the VIU0_DAT14 pin.

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Offset Address	Register Name	Total Reset Value
0x010	muxctrl_reg4	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg4
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg4	Multiplexing control for the VIU0_DAT14 pin. 0: VIU0_DAT14 1: GPIO0_1

muxctrl_reg5

muxctrl_reg5 is the multiplexing control register for the VIU0_DAT13 pin.

Offset Address	Register Name	Total Reset Value
0x014	muxctrl_reg5	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg5
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg5	Multiplexing control for the VIU0_DAT13 pin. 0: VIU0_DAT13 1: GPIO0_2

muxctrl_reg6

muxctrl_reg6 is the multiplexing control register for the VIU0_DAT12 pin.

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Offset Address	Register Name	Total Reset Value
0x018	muxctrl_reg6	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg6
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg6	Multiplexing control for the VIU0_DAT12 pin. 0: VIU0_DAT12 1: GPIO0_3

muxctrl_reg7

muxctrl_reg7 is the multiplexing control register for the VIU0_DAT11 pin.

Offset Address	Register Name	Total Reset Value
0x01C	muxctrl_reg7	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg7
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg7	Multiplexing control for the VIU0_DAT11 pin. 0: VIU0_DAT11 1: GPIO0_4

muxctrl_reg8

muxctrl_reg8 is the multiplexing control register for the VIU0_DAT10 pin.

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Offset Address	Register Name	Total Reset Value
0x020	muxctrl_reg8	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg8
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg8	Multiplexing control for the VIU0_DAT10 pin. 0: VIU0_DAT10 1: GPIO0_5

muxctrl_reg9

muxctrl_reg9 is the multiplexing control register for the VIU0_DAT9 pin.

Offset Address	Register Name	Total Reset Value
0x024	muxctrl_reg9	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg9
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg9	Multiplexing control for the VIU0_DAT9 pin. 0: VIU0_DAT9 1: GPIO0_6

muxctrl_reg10

muxctrl_reg10 is the multiplexing control register for the VIU0_DAT8 pin.

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Offset Address	Register Name	Total Reset Value
0x028	muxctrl_reg10	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg10
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg10	Multiplexing control for the VIU0_DAT8 pin. 0: VIU0_DAT8 1: GPIO0_7

muxctrl_reg11

muxctrl_reg11 is the multiplexing control register for the VIU0_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x02C	muxctrl_reg11	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg11
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg11	Multiplexing control for the VIU0_DAT7 pin. 0: VIU0_DAT7 1: GPIO1_0

muxctrl_reg12

muxctrl_reg12 is the multiplexing control register for the VIU0_DAT6 pin.

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Offset Address	Register Name	Total Reset Value
0x030	muxctrl_reg12	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg12
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg12	Multiplexing control for the VIU0_DAT6 pin. 0: VIU0_DAT6 1: GPIO1_1

muxctrl_reg13

muxctrl_reg13 is the multiplexing control register for the VIU0_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x034	muxctrl_reg13	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg13
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg13	Multiplexing control for the VIU0_DAT5 pin. 0: VIU0_DAT5 1: GPIO1_2

muxctrl_reg14

muxctrl_reg14 is the multiplexing control register for the VIU0_DAT4 pin.

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Offset Address	Register Name	Total Reset Value
0x038	muxctrl_reg14	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg14
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg14	Multiplexing control for the VIU0_DAT4 pin. 0: VIU0_DAT4 1: GPIO1_3

muxctrl_reg15

muxctrl_reg15 is the multiplexing control register for the VIU0_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x03C	muxctrl_reg15	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg15
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg15	Multiplexing control for the VIU0_DAT3 pin. 0: VIU0_DAT3 1: GPIO1_4

muxctrl_reg16

muxctrl_reg16 is the multiplexing control register for the VIU0_DAT2 pin.

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Offset Address	Register Name	Total Reset Value
0x040	muxctrl_reg16	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg16	Multiplexing control for the VIU0_DAT2 pin. 0: VIU0_DAT2 1: GPIO1_5

muxctrl_reg17

muxctrl_reg17 is the multiplexing control register for the VIU0_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x044	muxctrl_reg17	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg17
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg17	Multiplexing control for the VIU0_DAT1 pin. 0: VIU0_DAT1 1: GPIO1_6

muxctrl_reg18

muxctrl_reg18 is the multiplexing control register for the VIU0_DAT0 pin.

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Offset Address	Register Name	Total Reset Value
0x048	muxctrl_reg18	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg18
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg18	Multiplexing control for the VIU0_DAT0 pin. 0: VIU0_DAT0 1: GPIO1_7

muxctrl_reg19

muxctrl_reg19 is the multiplexing control register for the VIU1_CLK pin.

Offset Address	Register Name	Total Reset Value
0x04C	muxctrl_reg19	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg19
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg19	Multiplexing control for the VIU1_CLK pin. 0: VIU1_CLK 1: GPIO12_1

muxctrl_reg20

muxctrl_reg20 is the multiplexing control register for the VIU1_VS pin.

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Offset Address	Register Name	Total Reset Value
0x050	muxctrl_reg20	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg20	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg20	Multiplexing control for the VIU1_VS pin. 00: VIU1_VS 01: GPIO12_4 10: VIU1_CLKA Other values: reserved

muxctrl_reg21

muxctrl_reg21 is the multiplexing control register for the VIU1_HS pin.

Offset Address	Register Name	Total Reset Value
0x054	muxctrl_reg21	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg21	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg21	Multiplexing control for the VIU1_HS pin. 00: VIU1_HS 01: GPIO12_5 10: UART2_TXD Other values: reserved

muxctrl_reg22

muxctrl_reg22 is the multiplexing control register for the VIU1_DAT15 pin.

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Offset Address	Register Name	Total Reset Value
0x058	muxctrl_reg22	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg22
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg22	Multiplexing control for the VIU1_DAT15 pin. 0: VIU1_DAT15 1: GPIO2_0

muxctrl_reg23

muxctrl_reg23 is the multiplexing control register for the VIU1_DAT14 pin.

Offset Address	Register Name	Total Reset Value
0x05C	muxctrl_reg23	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg23
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg23	Multiplexing control for the VIU1_DAT14 pin. 0: VIU1_DAT14 1: GPIO2_1

muxctrl_reg24

muxctrl_reg24 is the multiplexing control register for the VIU1_DAT13 pin.

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Offset Address	Register Name	Total Reset Value
0x060	muxctrl_reg24	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg24
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg24	Multiplexing control for the VIU1_DAT13 pin. 0: VIU1_DAT13 1: GPIO2_2

muxctrl_reg25

muxctrl_reg25 is the multiplexing control register for the VIU1_DAT12 pin.

Offset Address	Register Name	Total Reset Value
0x064	muxctrl_reg25	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg25
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg25	Multiplexing control for the VIU1_DAT12 pin. 0: VIU1_DAT12 1: GPIO2_3

muxctrl_reg26

muxctrl_reg26 is the multiplexing control register for the VIU1_DAT11 pin.

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Offset Address	Register Name	Total Reset Value
0x068	muxctrl_reg26	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg26
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg26	Multiplexing control for the VIU1_DAT11 pin. 0: VIU1_DAT11 1: GPIO2_4

muxctrl_reg27

muxctrl_reg27 is the multiplexing control register for the VIU1_DAT10 pin.

Offset Address	Register Name	Total Reset Value
0x06C	muxctrl_reg27	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg27
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg27	Multiplexing control for the VIU1_DAT10 pin. 0: VIU1_DAT10 1: GPIO2_5

muxctrl_reg28

muxctrl_reg28 is the multiplexing control register for the VIU1_DAT9 pin.

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Offset Address	Register Name	Total Reset Value
0x070	muxctrl_reg28	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg28
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg28	Multiplexing control for the VIU1_DAT9 pin. 0: VIU1_DAT9 1: GPIO2_6

muxctrl_reg29

muxctrl_reg29 is the multiplexing control register for the VIU1_DAT8 pin.

Offset Address	Register Name	Total Reset Value
0x074	muxctrl_reg29	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg29
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg29	Multiplexing control for the VIU1_DAT8 pin. 0: VIU1_DAT8 1: GPIO2_7

muxctrl_reg30

muxctrl_reg30 is the multiplexing control register for the VIU1_DAT7 pin.

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Offset Address	Register Name	Total Reset Value
0x078	muxctrl_reg30	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg30
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg30	Multiplexing control for the VIU1_DAT7 pin. 0: VIU1_DAT7 1: GPIO3_0

muxctrl_reg31

muxctrl_reg31 is the multiplexing control register for the VIU1_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x07C	muxctrl_reg31	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg31
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg31	Multiplexing control for the VIU1_DAT6 pin. 0: VIU1_DAT6 1: GPIO3_1

muxctrl_reg32

muxctrl_reg32 is the multiplexing control register for the VIU1_DAT5 pin.

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Offset Address	Register Name	Total Reset Value
0x080	muxctrl_reg32	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg32
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg32	Multiplexing control for the VIU1_DAT5 pin. 0: VIU1_DAT5 1: GPIO3_2

muxctrl_reg33

muxctrl_reg33 is the multiplexing control register for the VIU1_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x084	muxctrl_reg33	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg33
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg33	Multiplexing control for the VIU1_DAT4 pin. 0: VIU1_DAT4 1: GPIO3_3

muxctrl_reg34

muxctrl_reg34 is the multiplexing control register for the VIU1_DAT3 pin.

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Offset Address	Register Name	Total Reset Value
0x088	muxctrl_reg34	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg34
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg34	Multiplexing control for the VIU1_DAT3 pin. 0: VIU1_DAT3 1: GPIO3_4

muxctrl_reg35

muxctrl_reg35 is the multiplexing control register for the VIU1_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x08C	muxctrl_reg35	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg35
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg35	Multiplexing control for the VIU1_DAT2 pin. 0: VIU1_DAT2 1: GPIO3_5

muxctrl_reg36

muxctrl_reg36 is the multiplexing control register for the VIU1_DAT1 pin.

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Offset Address	Register Name	Total Reset Value
0x090	muxctrl_reg36	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg36
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg36	Multiplexing control for the VIU1_DAT1 pin. 0: VIU1_DAT1 1: GPIO3_6

muxctrl_reg37

muxctrl_reg37 is the multiplexing control register for the VIU1_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x094	muxctrl_reg37	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg37
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg37	Multiplexing control for the VIU1_DAT0 pin. 0: VIU1_DAT0 1: GPIO3_7

muxctrl_reg38

muxctrl_reg38 is the multiplexing control register for the VOU1120_CLK pin.

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Offset Address	Register Name	Total Reset Value
0x098	muxctrl_reg38	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg38
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg38	Multiplexing control for the VOU1120_CLK pin. 00: GPIO12_6 01: VOU1120_CLK 10: LCD_CLK Other values: reserved

muxctrl_reg39

muxctrl_reg39 is the multiplexing control register for the VOU1120_DATA15 pin.

Offset Address	Register Name	Total Reset Value
0x09C	muxctrl_reg39	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg39
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg39	Multiplexing control for the VOU1120_DATA15 pin. 00: GPIO4_0 01: VOU1120_DATA15 10: LCD_DATA_G0 Other values: reserved

muxctrl_reg40

muxctrl_reg40 is the multiplexing control register for the VOU1120_DATA14 pin.

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Offset Address	Register Name	Total Reset Value
0x0A0	muxctrl_reg40	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg40
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg40	Multiplexing control for the VOU1120_DATA14 pin. 00: GPIO4_1 01: VOU1120_DATA14 10: LCD_DATA_G1 Other values: reserved

muxctrl_reg41

muxctrl_reg41 is the multiplexing control register for the VOU1120_DATA13 pin.

Offset Address	Register Name	Total Reset Value
0x0A4	muxctrl_reg41	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg41
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg41	Multiplexing control for the VOU1120_DATA13 pin. 00: GPIO4_2 01: VOU1120_DATA13 10: LCD_DATA_G2 Other values: reserved

muxctrl_reg42

muxctrl_reg42 is the multiplexing control register for the VOU1120_DATA12 pin.

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Offset Address	Register Name	Total Reset Value
0x0A8	muxctrl_reg42	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg42	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg42	Multiplexing control for the VOU1120_DATA12 pin. 00: GPIO4_3 01: VOU1120_DATA12 10: LCD_DATA_G3 Other values: reserved

muxctrl_reg43

muxctrl_reg43 is the multiplexing control register for the VOU1120_DATA11 pin.

Offset Address	Register Name	Total Reset Value
0x0AC	muxctrl_reg43	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg43	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg43	Multiplexing control for the VOU1120_DATA11 pin. 00: GPIO4_4 01: VOU1120_DATA11 10: LCD_DATA_G4 Other values: reserved

muxctrl_reg44

muxctrl_reg44 is the multiplexing control register for the VOU1120_DATA10 pin.

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Offset Address	Register Name	Total Reset Value
0x0B0	muxctrl_reg44	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg44
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg44	Multiplexing control for the VOU1120_DATA10 pin. 00: GPIO4_5 01: VOU1120_DATA10 10: LCD_DATA_G5 Other values: reserved

muxctrl_reg45

muxctrl_reg45 is the multiplexing control register for the VOU1120_DATA9 pin.

Offset Address	Register Name	Total Reset Value
0x0B4	muxctrl_reg45	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg45
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg45	Multiplexing control for the VOU1120_DATA9 pin. 00: GPIO4_6 01: VOU1120_DATA9 10: LCD_DATA_G6 Other values: reserved

muxctrl_reg46

muxctrl_reg46 is the multiplexing control register for the VOU1120_DATA8 pin.

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Offset Address	Register Name	Total Reset Value
0x0B8	muxctrl_reg46	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg46	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg46	Multiplexing control for the VOU1120_DATA8 pin. 00: GPIO4_7 01: VOU1120_DATA8 10: LCD_DATA_G7 Other values: reserved

muxctrl_reg47

muxctrl_reg47 is the multiplexing control register for the VOU1120_DATA7 pin.

Offset Address	Register Name	Total Reset Value
0x0BC	muxctrl_reg47	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg47	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg47	Multiplexing control for the VOU1120_DATA7 pin. 00: GPIO5_0 01: VOU1120_DATA7 10: LCD_DATA_B0 Other values: reserved

muxctrl_reg48

muxctrl_reg48 is the multiplexing control register for the VOU1120_DATA6 pin.

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Offset Address	Register Name	Total Reset Value
0x0C0	muxctrl_reg48	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg48
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg48	Multiplexing control for the VOU1120_DATA6 pin. 00: GPIO5_1 01: VOU1120_DATA6 10: LCD_DATA_B1 Other values: reserved

muxctrl_reg49

muxctrl_reg4 is the multiplexing control register for the VOU1120_DATA5 pin.

Offset Address	Register Name	Total Reset Value
0x0C4	muxctrl_reg49	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg49
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg49	Multiplexing control for the VOU1120_DATA5 pin. 00: GPIO5_2 01: VOU1120_DATA5 10: LCD_DATA_B2 Other values: reserved

muxctrl_reg50

muxctrl_reg50 is the multiplexing control register for the VOU1120_DATA4 pin.

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Offset Address	Register Name	Total Reset Value
0x0C8	muxctrl_reg50	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg50
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg50	Multiplexing control for the VOU1120_DATA4 pin. 00: GPIO5_3 01: VOU1120_DATA4 10: LCD_DATA_B3 Other values: reserved

muxctrl_reg51

muxctrl_reg51 is the multiplexing control register for the VOU1120_DATA3 pin.

Offset Address	Register Name	Total Reset Value
0x0CC	muxctrl_reg51	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg51
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg51	Multiplexing control for the VOU1120_DATA3 pin. 00: GPIO5_4 01: VOU1120_DATA3 10: LCD_DATA_B4 Other values: reserved

muxctrl_reg52

muxctrl_reg52 is the multiplexing control register for the VOU1120_DATA2 pin.

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Offset Address	Register Name	Total Reset Value
0x0D0	muxctrl_reg52	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg52
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg52	Multiplexing control for the VOU1120_DATA2 pin. 00: GPIO5_5 01: VOU1120_DATA2 10: LCD_DATA_B5 Other values: reserved

muxctrl_reg53

muxctrl_reg53 is the multiplexing control register for the VOU1120_DATA1 pin.

Offset Address	Register Name	Total Reset Value
0x0D4	muxctrl_reg53	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg53
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg53	Multiplexing control for the VOU1120_DATA1 pin. 00: GPIO5_6 01: VOU1120_DATA1 10: LCD_DATA_B6 Other values: reserved

muxctrl_reg54

muxctrl_reg54 is the multiplexing control register for the VOU1120_DATA0 pin.

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Offset Address	Register Name	Total Reset Value
0x0D8	muxctrl_reg54	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg54
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg54	Multiplexing control for the VOU1120_DATA0 pin. 00: GPIO5_7 01: VOU1120_DATA0 10: LCD_DATA_B7 Other values: reserved

muxctrl_reg55

muxctrl_reg55 is the multiplexing control register for the VGA_HS pin.

Offset Address	Register Name	Total Reset Value
0x0DC	muxctrl_reg55	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg55
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg55	Multiplexing control for the VGA_HS pin. 00: GPIO13_0 01: VOU1120_HS 10: VGA_HS Other values: reserved

muxctrl_reg56

muxctrl_reg56 is the multiplexing control register for the VGA_VS pin.

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Offset Address	Register Name	Total Reset Value
0x0E0	muxctrl_reg56	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg56
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg56	Multiplexing control for the VGA_VS pin. 00: GPIO13_1 01: VOU1120_VS 10: VGA_VS Other values: reserved

muxctrl_reg57

muxctrl_reg57 is the multiplexing control register for the VOU656_CLK pin.

Offset Address	Register Name	Total Reset Value
0x0E4	muxctrl_reg57	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg57
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg57	Multiplexing control for the VOU656_CLK pin. 00: GPIO12_7 01: VOU656_CLK 11: SDIO_CCLK_OUT Other values: reserved

muxctrl_reg58

muxctrl_reg58 is the multiplexing control register for the VOU656_DATA7 pin.

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Offset Address	Register Name	Total Reset Value
0x0E8	muxctrl_reg58	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg58
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg58	Multiplexing control for the VOU656_DATA7 pin. 00: GPIO6_0 01: VOU656_DATA7 10: LCD_DATA_R0 11: SDIO_CARD_POWER_EN

muxctrl_reg59

muxctrl_reg59 is the multiplexing control register for the VOU656_DATA6 pin.

Offset Address	Register Name	Total Reset Value
0x0EC	muxctrl_reg59	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg59
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg59	Multiplexing control for the VOU656_DATA6 pin. 00: GPIO6_1 01: VOU656_DATA6 10: LCD_DATA_R1 11: SDIO_CARD_DETECT

muxctrl_reg60

muxctrl_reg60 is the multiplexing control register for the VOU656_DATA5 pin.

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Offset Address	Register Name	Total Reset Value
0x0F0	muxctrl_reg60	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg60
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg60	Multiplexing control for the VOU656_DATA5 pin. 00: GPIO6_2 01: VOU656_DATA5 10: LCD_DATA_R2 11: SDIO_CWPR

muxctrl_reg61

muxctrl_reg61 is the multiplexing control register for the VOU656_DATA4 pin.

Offset Address	Register Name	Total Reset Value
0x0F4	muxctrl_reg61	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg61
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg61	Multiplexing control for the VOU656_DATA4 pin. 00: GPIO6_3 01: VOU656_DATA4 10: LCD_DATA_R3 11: SDIO_CCMD

muxctrl_reg62

muxctrl_reg62 is the multiplexing control register for the VOU656_DATA3 pin.

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Offset Address	Register Name	Total Reset Value
0x0F8	muxctrl_reg62	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg62
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg62	Multiplexing control for the VOU656_DATA3 pin. 00: GPIO6_4 01: VOU656_DATA3 10: LCD_DATA_R4 11: SDIO_CDATA3

muxctrl_reg63

muxctrl_reg63 is the multiplexing control register for the VOU656_DATA2 pin.

Offset Address	Register Name	Total Reset Value
0x0FC	muxctrl_reg63	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg63
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg63	Multiplexing control for the VOU656_DATA2 pin. 00: GPIO6_5 01: VOU656_DATA2 10: LCD_DATA_R5 11: SDIO_CDATA2

muxctrl_reg64

muxctrl_reg64 is the multiplexing control register for the VOU656_DATA1 pin.

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Offset Address	Register Name	Total Reset Value
0x100	muxctrl_reg64	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg64
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg64	Multiplexing control for the VOU656_DATA1 pin. 00: GPIO6_6 01: VOU656_DATA1 10: LCD_DATA_R6 11: SDIO_CDATA1

muxctrl_reg65

muxctrl_reg65 is the multiplexing control register for the VOU656_DATA0 pin.

Offset Address	Register Name	Total Reset Value
0x104	muxctrl_reg65	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg65
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg65	Multiplexing control for the VOU656_DATA0 pin. 00: GPIO6_7 01: VOU656_DATA0 10: LCD_DATA_R7 11: SDIO_CDATA0

muxctrl_reg66

muxctrl_reg66 is the multiplexing control register for the SIO0_RCLK pin.

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Offset Address	Register Name	Total Reset Value
0x108	muxctrl_reg66	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg66
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg66	Multiplexing control for the SIO0_RCLK pin. 0: GPIO7_0 1: SIO0_RCLK

muxctrl_reg67

muxctrl_reg67 is the multiplexing control register for the SIO0_RFS pin.

Offset Address	Register Name	Total Reset Value
0x10C	muxctrl_reg67	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg67
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg67	Multiplexing control for the SIO0_RFS pin. 0: GPIO7_1 1: SIO0_RFS

muxctrl_reg68

muxctrl_reg68 is the multiplexing control register for the SIO0_DIN pin.

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Offset Address	Register Name	Total Reset Value
0x110	muxctrl_reg68	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg68
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg68	Multiplexing control for the SIO0_DIN pin. 0: GPIO7_2 1: SIO0_DIN

muxctrl_reg69

muxctrl_reg69 is the multiplexing control register for the SIO1_RCLK pin.

Offset Address	Register Name	Total Reset Value
0x114	muxctrl_reg69	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg69
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg69	Multiplexing control for the SIO1_RCLK pin. 0: GPIO7_3 1: SIO1_RCLK

muxctrl_reg70

muxctrl_reg70 is the multiplexing control register for the SIO1_RFS pin.

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Offset Address	Register Name	Total Reset Value
0x118	muxctrl_reg70	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg70
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg70	Multiplexing control for the SIO1_RFS pin. 0: GPIO7_4 1: SIO1_RFS

muxctrl_reg71

muxctrl_reg71 is the multiplexing control register for the SIO1_DIN pin.

Offset Address	Register Name	Total Reset Value
0x11C	muxctrl_reg71	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg71
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg71	Multiplexing control for the SIO1_DIN pin. 0: GPIO7_5 1: SIO1_DIN

muxctrl_reg72

muxctrl_reg72 is the multiplexing control register for the SIO2_XCLK pin.

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Offset Address	Register Name	Total Reset Value
0x120	muxctrl_reg72	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg72
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg72	Multiplexing control for the SIO2_XCLK pin. 0: GPIO7_6 1: SIO2_XCLK

muxctrl_reg73

muxctrl_reg73 is the multiplexing control register for the SIO2_XFS pin.

Offset Address	Register Name	Total Reset Value
0x124	muxctrl_reg73	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg73
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg73	Multiplexing control for the SIO2_XFS pin. 0: GPIO7_7 1: SIO2_XFS

muxctrl_reg74

muxctrl_reg74 is the multiplexing control register for the SIO2_RCLK pin.

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Offset Address	Register Name	Total Reset Value
0x128	muxctrl_reg74	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg74
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg74	Multiplexing control for the SIO2_RCLK pin. 0: GPIO8_0 1: SIO2_RCLK

muxctrl_reg75

muxctrl_reg75 is the multiplexing control register for the SIO2_RFS pin.

Offset Address	Register Name	Total Reset Value
0x12C	muxctrl_reg75	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg75
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg75	Multiplexing control for the SIO2_RFS pin. 0: GPIO8_1 1: SIO2_RFS

muxctrl_reg76

muxctrl_reg76 is the multiplexing control register for the SIO2_DIN pin.

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Offset Address	Register Name	Total Reset Value
0x130	muxctrl_reg76	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg76
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg76	Multiplexing control for the SIO2_DIN pin. 0: GPIO8_2 1: SIO2_DIN

muxctrl_reg77

muxctrl_reg77 is the multiplexing control register for the SPI_SCLK pin.

Offset Address	Register Name	Total Reset Value
0x134	muxctrl_reg77	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg77
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg77	Multiplexing control for the SPI_SCLK pin. 0: GPIO8_3 1: SPI_SCLK

muxctrl_reg78

muxctrl_reg78 is the multiplexing control register for the SPI_SDO pin.

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Offset Address	Register Name	Total Reset Value
0x138	muxctrl_reg78	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg78
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg78	Multiplexing control for the SPI_SDO pin. 0: GPIO8_4 1: SPI_SDO

muxctrl_reg79

muxctrl_reg79 is the multiplexing control register for the SPI_SDI pin.

Offset Address	Register Name	Total Reset Value
0x13C	muxctrl_reg79	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg79
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg79	Multiplexing control for the SPI_SDI pin. 0: GPIO8_5 1: SPI_SDI

muxctrl_reg80

muxctrl_reg80 is the multiplexing control register for the SPI_CSN0 pin.

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Offset Address	Register Name	Total Reset Value
0x140	muxctrl_reg80	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg80
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg80	Multiplexing control for the SPI_CSN0 pin. 0: GPIO8_6 1: SPI_CSN0

muxctrl_reg81

muxctrl_reg81 is the multiplexing control register for the SPI_CSN3 pin.

Offset Address	Register Name	Total Reset Value
0x144	muxctrl_reg81	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg81	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[2:0]	RW	muxctrl_reg81	Multiplexing control for the SPI_CSN3 pin. 000: SPI_CSN3 001: NF_BOOT_PIN4 010: CLK_TEST_OUT0 011: CLK_TEST_OUT1 100: CLK_TEST_OUT2 101: CLK_TEST_OUT3 Other values: reserved

muxctrl_reg82

muxctrl_reg82 is the multiplexing control register for the I2C_SDA pin.

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Offset Address	Register Name	Total Reset Value
0x148	muxctrl_reg82	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg82
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg82	Multiplexing control for the I2C_SDA pin. 0: GPIO13_2 1: I2C_SDA

muxctrl_reg83

muxctrl_reg83 is the multiplexing control register for the I2C_SCL pin.

Offset Address	Register Name	Total Reset Value
0x14C	muxctrl_reg83	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg83
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg83	Multiplexing control for the I2C_SCL pin. 0: GPIO13_3 1: I2C_SCL

muxctrl_reg84

muxctrl_reg84 is the multiplexing control register for the UART1_RTSN pin.

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Offset Address	Register Name	Total Reset Value
0x150	muxctrl_reg84	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg84
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg84	Multiplexing control for the UART1_RTSN pin. 0: GPIO9_0 1: UART1_RTSN

muxctrl_reg85

muxctrl_reg85 is the multiplexing control register for the UART1_RXD pin.

Offset Address	Register Name	Total Reset Value
0x154	muxctrl_reg85	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg85
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg85	Multiplexing control for the UART1_RXD pin. 0: GPIO9_1 1: UART1_RXD

muxctrl_reg86

muxctrl_reg86 is the multiplexing control register for the UART1_CTSN pin.

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Offset Address	Register Name	Total Reset Value
0x158	muxctrl_reg86	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg86
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg86	Multiplexing control for the UART1_CTSN pin. 0: GPIO9_2 1: UART1_CTSN

muxctrl_reg87

muxctrl_reg87 is the multiplexing control register for the UART1_TXD pin.

Offset Address	Register Name	Total Reset Value
0x15C	muxctrl_reg87	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg87
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg87	Multiplexing control for the UART1_TXD pin. 0: GPIO9_3 1: UART1_TXD

muxctrl_reg88

muxctrl_reg88 is the multiplexing control register for the RGMII_TXD0 pin.

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Offset Address	Register Name	Total Reset Value
0x160	muxctrl_reg88	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg88	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[2:0]	RW	muxctrl_reg88	Multiplexing control for the RGMII_TXD0 pin. 000: PLL_TEST_OUT0 001: RGMII_TXD0 010: PLL_TEST_OUT1 011: PLL_TEST_OUT2 100: PLL_TEST_OUT3 Other values: reserved

muxctrl_reg89

muxctrl_reg89 is the multiplexing control register for the RGMII_TXCK pin.

Offset Address	Register Name	Total Reset Value
0x164	muxctrl_reg89	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg89
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg89	Multiplexing control for the RGMII_TXCK pin. 0: RGMII_TXCK 1: GPIO8_7

muxctrl_reg90

muxctrl_reg90 is the multiplexing control register for the RGMII_CRS pin.

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Offset Address	Register Name	Total Reset Value
0x168	muxctrl_reg90	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg90
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg90	Multiplexing control for the RGMII_CRS pin. 00: GPIO13_4 01: RGMII_CRS 10: RGMII_RXER Other values: reserved

muxctrl_reg91

muxctrl_reg91 is the multiplexing control register for the RGMII_COL pin.

Offset Address	Register Name	Total Reset Value
0x16C	muxctrl_reg91	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg91
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg91	Multiplexing control for the RGMII_COL pin. 00: GPIO13_5 01: RGMII_COL 10: RGMII_TXER Other values: reserved

muxctrl_reg92

muxctrl_reg92 is the multiplexing control register for the IR_IN pin.

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Offset Address	Register Name	Total Reset Value
0x170	muxctrl_reg92	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg92
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg92	Multiplexing control for the IR_IN pin. 0: IR_IN 1: GPIO9_4

muxctrl_reg93

muxctrl_reg93 is the multiplexing control register for the NF_DQ0 pin.

Offset Address	Register Name	Total Reset Value
0x174	muxctrl_reg93	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg93
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg93	Multiplexing control for the NF_DQ0 pin. 0: NF_DQ0 1: GPIO9_5

muxctrl_reg94

muxctrl_reg94 is the multiplexing control register for the NF_DQ1 pin.

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Offset Address	Register Name	Total Reset Value
0x178	muxctrl_reg94	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg94
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg94	Multiplexing control for the NF_DQ1 pin. 0: NF_DQ1 1: GPIO9_6

muxctrl_reg95

muxctrl_reg95 is the multiplexing control register for the NF_DQ2 pin.

Offset Address	Register Name	Total Reset Value
0x17C	muxctrl_reg95	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg95
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg95	Multiplexing control for the NF_DQ2 pin. 0: NF_DQ2 1: GPIO9_7

muxctrl_reg96

muxctrl_reg96 is the multiplexing control register for the NF_DQ3 pin.

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Offset Address	Register Name	Total Reset Value
0x180	muxctrl_reg96	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg96
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg96	Multiplexing control for the NF_DQ3 pin. 0: NF_DQ3 1: GPIO10_0

muxctrl_reg97

muxctrl_reg97 is the multiplexing control register for the NF_DQ4 pin.

Offset Address	Register Name	Total Reset Value
0x184	muxctrl_reg97	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg97
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg97	Multiplexing control for the NF_DQ4 pin. 0: NF_DQ4 1: GPIO10_1

muxctrl_reg98

muxctrl_reg98 is the multiplexing control register for the NF_DQ5 pin.

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Offset Address	Register Name	Total Reset Value
0x188	muxctrl_reg98	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg98
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg98	Multiplexing control for the NF_DQ5 pin. 0: NF_DQ5 1: GPIO10_2

muxctrl_reg99

muxctrl_reg99 is the multiplexing control register for the NF_DQ6 pin.

Offset Address	Register Name	Total Reset Value
0x18C	muxctrl_reg99	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg99
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg99	Multiplexing control for the NF_DQ6 pin. 0: NF_DQ6 1: GPIO10_3

muxctrl_reg100

muxctrl_reg100 is the multiplexing control register for the NF_DQ7 pin.

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Offset Address	Register Name	Total Reset Value
0x190	muxctrl_reg100	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg100
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg100	Multiplexing control for the NF_DQ7 pin. 0: NF_DQ7 1: GPIO10_4

muxctrl_reg101

muxctrl_reg101 is the multiplexing control register for the NF_RDY0 pin.

Offset Address	Register Name	Total Reset Value
0x194	muxctrl_reg101	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg101
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg101	Multiplexing control for the NF_RDY0 pin. 0: NF_RDY0 1: GPIO10_5

muxctrl_reg102

muxctrl_reg102 is the multiplexing control register for the NF_RDY1 pin.

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Offset Address	Register Name	Total Reset Value
0x198	muxctrl_reg102	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg102
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg102	Multiplexing control for the NF_RDY1 pin. 0: NF_RDY1 1: GPIO10_6

muxctrl_reg103

muxctrl_reg103 is the multiplexing control register for the SFC_DIO pin.

Offset Address	Register Name	Total Reset Value
0x19C	muxctrl_reg103	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg103
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg103	Multiplexing control for the SFC_DIO pin. 0: SFC_DIO 1: GPIO13_6

muxctrl_reg104

muxctrl_reg104 is the multiplexing control register for the SFC_WP_IO2 pin.

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Offset Address	Register Name	Total Reset Value
0x1A0	muxctrl_reg104	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg104
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg104	Multiplexing control for the SFC_WP_IO2 pin. 0: SFC_WP_IO2 1: GPIO10_7

muxctrl_reg105

muxctrl_reg105 is the multiplexing control register for the SFC_DOI pin.

Offset Address	Register Name	Total Reset Value
0x1A4	muxctrl_reg105	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg105
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg105	Multiplexing control for the SFC_DOI pin. 0: SFC_DOI 1: GPIO13_7

muxctrl_reg106

muxctrl_reg106 is the multiplexing control register for the SFC_HOLD_IO3 pin.

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Offset Address	Register Name	Total Reset Value
0x1A8	muxctrl_reg106	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg106
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg106	Multiplexing control for the SFC_HOLD_IO3 pin. 0: SFC_HOLD_IO3 1: GPIO14_4

muxctrl_reg107

muxctrl_reg107 is the multiplexing control register for the USB0_OVRCUR pin.

Offset Address	Register Name	Total Reset Value
0x1AC	muxctrl_reg107	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg107
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg107	Multiplexing control for the USB0_OVRCUR pin. 0: GPIO14_0 1: USB0_OVRCUR

muxctrl_reg108

muxctrl_reg108 is the multiplexing control register for the USB0_PWREN pin.

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Offset Address	Register Name	Total Reset Value
0x1B0	muxctrl_reg108	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg108
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg108	Multiplexing control for the USB0_PWREN pin. 0: GPIO14_1 1: USB0_PWREN

muxctrl_reg109

muxctrl_reg109 is the multiplexing control register for the USB1_OVRCUR pin.

Offset Address	Register Name	Total Reset Value
0x1B4	muxctrl_reg109	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg109
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg109	Multiplexing control for the USB1_OVRCUR pin. 0: GPIO14_2 1: USB1_OVRCUR

muxctrl_reg110

muxctrl_reg110 is the multiplexing control register for the USB1_PWREN pin.

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Offset Address	Register Name	Total Reset Value
0x1B8	muxctrl_reg110	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg110
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg110	Multiplexing control for the USB1_PWREN pin. 0: GPIO14_3 1: USB1_PWREN

muxctrl_reg111

muxctrl_reg111 is the multiplexing control register for the GPIO11_0 pin.

Offset Address	Register Name	Total Reset Value
0x1BC	muxctrl_reg111	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg111
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg111	Multiplexing control for the GPIO11_0 pin. 0: GPIO11_0 1: UART3_RXD

muxctrl_reg112

muxctrl_reg112 is the multiplexing control register for the GPIO11_1 pin.

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Offset Address	Register Name	Total Reset Value
0x1C0	muxctrl_reg112	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg112
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg112	Multiplexing control for the GPIO11_1 pin. 0: GPIO11_1 1: UART3_TXD

muxctrl_reg113

muxctrl_reg113 is the multiplexing control register for the SATA_LED_N0 pin.

Offset Address	Register Name	Total Reset Value
0x1C4	muxctrl_reg113	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg113
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg113	Multiplexing control for the SATA_LED_N0 pin. 0: GPIO11_2 1: SATA_LED_N0

muxctrl_reg114

muxctrl_reg114 is the multiplexing control register for the SATA_LED_N1 pin.

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Offset Address	Register Name	Total Reset Value
0x1C8	muxctrl_reg114	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg114
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg114	Multiplexing control for the SATA_LED_N1 pin. 0: GPIO11_3 1: SATA_LED_N1

muxctrl_reg115

muxctrl_reg115 is the multiplexing control register for the HDMI_HOTPLUG pin.

Offset Address	Register Name	Total Reset Value
0x1CC	muxctrl_reg115	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg115
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg115	Multiplexing control for the HDMI_HOTPLUG pin. 0: GPIO11_4 1: HDMI_HOTPLUG

muxctrl_reg116

muxctrl_reg116 is the multiplexing control register for the HDMI_CEC pin.

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Offset Address	Register Name	Total Reset Value
0x1D0	muxctrl_reg116	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg116
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg116	Multiplexing control for the HDMI_CEC pin. 0: GPIO11_5 1: HDMI_CEC

muxctrl_reg117

muxctrl_reg117 is the multiplexing control register for the HDMI_SDA pin.

Offset Address	Register Name	Total Reset Value
0x1D4	muxctrl_reg117	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg117
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg117	Multiplexing control for the HDMI_SDA pin. 0: GPIO11_6 1: HDMI_SDA

muxctrl_reg118

muxctrl_reg118 is the multiplexing control register for the HDMI_SCL pin.

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Offset Address	Register Name	Total Reset Value
0x1D8	muxctrl_reg118	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg118
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg118	Multiplexing control for the HDMI_SCL pin. 0: GPIO11_7 1: HDMI_SCL

2.4 Software Multiplexed Pins

VIU0

Table 2-37 lists the software multiplexed pins of VIU0.

Table 2-37 Software multiplexed pins of VIU0

Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	Multiplexing Signal 2
T26	VIU0_CLK	muxctrl_reg0	VIU0_CLK	GPIO12_0	None
U24	VIU0_VS	muxctrl_reg1	VIU0_VS	GPIO12_2	VIU0_CLKA
U23	VIU0_HS	muxctrl_reg2	VIU0_HS	GPIO12_3	UART2_RXD
L27	VIU0_DAT15	muxctrl_reg3	VIU0_DAT15	GPIO0_0	None
L28	VIU0_DAT14	muxctrl_reg4	VIU0_DAT14	GPIO0_1	None
M26	VIU0_DAT13	muxctrl_reg5	VIU0_DAT13	GPIO0_2	None
M27	VIU0_DAT12	muxctrl_reg6	VIU0_DAT12	GPIO0_3	None
N26	VIU0_DAT11	muxctrl_reg7	VIU0_DAT11	GPIO0_4	None
N28	VIU0_DAT10	muxctrl_reg8	VIU0_DAT10	GPIO0_5	None
N27	VIU0_DAT9	muxctrl_reg9	VIU0_DAT9	GPIO0_6	None

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Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	Multiplexing Signal 2
P27	VIU0_DAT8	muxctrl_reg10	VIU0_DAT8	GPIO0_7	None
P24	VIU0_DAT7	muxctrl_reg11	VIU0_DAT7	GPIO1_0	None
P23	VIU0_DAT6	muxctrl_reg12	VIU0_DAT6	GPIO1_1	None
R27	VIU0_DAT5	muxctrl_reg13	VIU0_DAT5	GPIO1_2	None
R28	VIU0_DAT4	muxctrl_reg14	VIU0_DAT4	GPIO1_3	None
R26	VIU0_DAT3	muxctrl_reg15	VIU0_DAT3	GPIO1_4	None
R24	VIU0_DAT2	muxctrl_reg16	VIU0_DAT2	GPIO1_5	None
R23	VIU0_DAT1	muxctrl_reg17	VIU0_DAT1	GPIO1_6	None
T27	VIU0_DAT0	muxctrl_reg18	VIU0_DAT0	GPIO1_7	None

Table 2-38 describes the software multiplexed pins of VIU0.

Table 2-38 Description of the software multiplexed pins of VIU0

Signal	Direction	Description
GPIO0_0	I/O	GPIO
GPIO0_1	I/O	GPIO
GPIO0_2	I/O	GPIO
GPIO0_3	I/O	GPIO
GPIO0_4	I/O	GPIO
GPIO0_5	I/O	GPIO
GPIO0_6	I/O	GPIO
GPIO0_7	I/O	GPIO
GPIO1_0	I/O	GPIO
GPIO1_1	I/O	GPIO
GPIO1_2	I/O	GPIO
GPIO1_3	I/O	GPIO
GPIO1_4	I/O	GPIO
GPIO1_5	I/O	GPIO

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Signal	Direction	Description
GPIO1_6	I/O	GPIO
GPIO1_7	I/O	GPIO
GPIO12_0	I/O	GPIO
GPIO12_2	I/O	GPIO
GPIO12_3	I/O	GPIO
UART2_RXD	I	UART2 data receive
VIU0_CLK	I	VIU0 clock
VIU0_CLKA	I	VIU0 clock
VIU0_DAT0	I	VIU0 data input
VIU0_DAT1	I	VIU0 data input
VIU0_DAT10	I	VIU0 data input
VIU0_DAT11	I	VIU0 data input
VIU0_DAT12	I	VIU0 data input
VIU0_DAT13	I	VIU0 data input
VIU0_DAT14	I	VIU0 data input
VIU0_DAT15	I	VIU0 data input
VIU0_DAT2	I	VIU0 data input
VIU0_DAT3	I	VIU0 data input
VIU0_DAT4	I	VIU0 data input
VIU0_DAT5	I	VIU0 data input
VIU0_DAT6	I	VIU0 data input
VIU0_DAT7	I	VIU0 data input
VIU0_DAT8	I	VIU0 data input
VIU0_DAT9	I	VIU0 data input
VIU0_HS	I	VIU0 horizontal sync, active high
VIU0_VS	I	VIU0 vertical sync, active high

VIU1

Table 2-39 lists the software multiplexed pins of VIU1.

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Table 2-39 Software multiplexed pins of VIU1

Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	Multiplexing Signal 2
AB26	VIU1_CLK	muxctrl_reg19	VIU1_CLK	GPIO12_1	None
AA24	VIU1_VS	muxctrl_reg20	VIU1_VS	GPIO12_4	VIU1_CLKA
AA23	VIU1_HS	muxctrl_reg21	VIU1_HS	GPIO12_5	UART2_TXD
U27	VIU1_DAT15	muxctrl_reg22	VIU1_DAT15	GPIO2_0	None
U28	VIU1_DAT14	muxctrl_reg23	VIU1_DAT14	GPIO2_1	None
V26	VIU1_DAT13	muxctrl_reg24	VIU1_DAT13	GPIO2_2	None
V27	VIU1_DAT12	muxctrl_reg25	VIU1_DAT12	GPIO2_3	None
V24	VIU1_DAT11	muxctrl_reg26	VIU1_DAT11	GPIO2_4	None
V23	VIU1_DAT10	muxctrl_reg27	VIU1_DAT10	GPIO2_5	None
W26	VIU1_DAT9	muxctrl_reg28	VIU1_DAT9	GPIO2_6	None
W27	VIU1_DAT8	muxctrl_reg29	VIU1_DAT8	GPIO2_7	None
W28	VIU1_DAT7	muxctrl_reg30	VIU1_DAT7	GPIO3_0	None
Y26	VIU1_DAT6	muxctrl_reg31	VIU1_DAT6	GPIO3_1	None
Y27	VIU1_DAT5	muxctrl_reg32	VIU1_DAT5	GPIO3_2	None
Y24	VIU1_DAT4	muxctrl_reg33	VIU1_DAT4	GPIO3_3	None
Y23	VIU1_DAT3	muxctrl_reg34	VIU1_DAT3	GPIO3_4	None
AA26	VIU1_DAT2	muxctrl_reg35	VIU1_DAT2	GPIO3_5	None
AA27	VIU1_DAT1	muxctrl_reg36	VIU1_DAT1	GPIO3_6	None
AA28	VIU1_DAT0	muxctrl_reg37	VIU1_DAT0	GPIO3_7	None

Table 2-40 describes the software multiplexed pins of VIU1.

Table 2-40 Description of the software multiplexed pins of VIU1

Signal	Direction	Description
GPIO12_1	I/O	GPIO

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Signal	Direction	Description
GPIO12_4	I/O	GPIO
GPIO12_5	I/O	GPIO
GPIO2_0	I/O	GPIO
GPIO2_1	I/O	GPIO
GPIO2_2	I/O	GPIO
GPIO2_3	I/O	GPIO
GPIO2_4	I/O	GPIO
GPIO2_5	I/O	GPIO
GPIO2_6	I/O	GPIO
GPIO2_7	I/O	GPIO
GPIO3_0	I/O	GPIO
GPIO3_1	I/O	GPIO
GPIO3_2	I/O	GPIO
GPIO3_3	I/O	GPIO
GPIO3_4	I/O	GPIO
GPIO3_5	I/O	GPIO
GPIO3_6	I/O	GPIO
GPIO3_7	I/O	GPIO
UART2_TXD	O	UART2 data transmit
VIU1_CLK	I	VIU1 clock
VIU1_CLKA	I	VIU1 clock
VIU1_DAT0	I	VIU1 data input
VIU1_DAT1	I	VIU1 data input
VIU1_DAT10	I	VIU1 data input
VIU1_DAT11	I	VIU1 data input
VIU1_DAT12	I	VIU1 data input
VIU1_DAT13	I	VIU1 data input
VIU1_DAT14	I	VIU1 data input
VIU1_DAT15	I	VIU1 data input
VIU1_DAT2	I	VIU1 data input
VIU1_DAT3	I	VIU1 data input

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Signal	Direction	Description
VIU1_DAT4	I	VIU1 data input
VIU1_DAT5	I	VIU1 data input
VIU1_DAT6	I	VIU1 data input
VIU1_DAT7	I	VIU1 data input
VIU1_DAT8	I	VIU1 data input
VIU1_DAT9	I	VIU1 data input
VIU1_HS	I	VIU1 horizontal sync, active high
VIU1_VS	I	VIU1 vertical sync, active high

VOU

Table 2-41 lists the software multiplexed pins of the VOU.

Table 2-41 Software multiplexed pins of the VOU

Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	Multiplexing Signal 2	Multiplexing Signal 3
B6	VOU1120_CLK	muxctrl_reg38	GPIO12_6	VOU1120_CLK	LCD_CLK	None
B5	VOU1120_DATA15	muxctrl_reg39	GPIO4_0	VOU1120_DATA15	LCD_DATA_G0	None
A5	VOU1120_DATA14	muxctrl_reg40	GPIO4_1	VOU1120_DATA14	LCD_DATA_G1	None
C5	VOU1120_DATA13	muxctrl_reg41	GPIO4_2	VOU1120_DATA13	LCD_DATA_G2	None
B4	VOU1120_DATA12	muxctrl_reg42	GPIO4_3	VOU1120_DATA12	LCD_DATA_G3	None
C4	VOU1120_DATA11	muxctrl_reg43	GPIO4_4	VOU1120_DATA11	LCD_DATA_G4	None
A3	VOU1120_DATA10	muxctrl_reg44	GPIO4_5	VOU1120_DATA10	LCD_DATA_G5	None
B3	VOU1120_DATA9	muxctrl_reg45	GPIO4_6	VOU1120_DATA9	LCD_DATA_G6	None
A2	VOU1120_DATA8	muxctrl_reg46	GPIO4_7	VOU1120_DATA8	LCD_DATA_G7	None
B2	VOU1120_DATA7	muxctrl_reg47	GPIO5_0	VOU1120_DATA7	LCD_DATA_B0	None

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Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	Multiplexing Signal 2	Multiplexing Signal 3
B1	VOU1120_DATA6	muxctrl_reg48	GPIO5_1	VOU1120_DATA6	LCD_DATA_B1	None
C3	VOU1120_DATA5	muxctrl_reg49	GPIO5_2	VOU1120_DATA5	LCD_DATA_B2	None
C2	VOU1120_DATA4	muxctrl_reg50	GPIO5_3	VOU1120_DATA4	LCD_DATA_B3	None
D3	VOU1120_DATA3	muxctrl_reg51	GPIO5_4	VOU1120_DATA3	LCD_DATA_B4	None
D1	VOU1120_DATA2	muxctrl_reg52	GPIO5_5	VOU1120_DATA2	LCD_DATA_B5	None
D2	VOU1120_DATA1	muxctrl_reg53	GPIO5_6	VOU1120_DATA1	LCD_DATA_B6	None
E3	VOU1120_DATA0	muxctrl_reg54	GPIO5_7	VOU1120_DATA0	LCD_DATA_B7	None
E9	VGA_HS	muxctrl_reg55	GPIO13_0	VOU1120_HS	VGA_HS	None
F9	VGA_VS	muxctrl_reg56	GPIO13_1	VOU1120_VS	VGA_VS	None
E8	VOU656_CLK	muxctrl_reg57	GPIO12_7	VOU656_CLK	SDIO_CCLK_OUT	None
C9	VOU656_DATA7	muxctrl_reg58	GPIO6_0	VOU656_DATA7	LCD_DATA_R0	SDIO_CARD_POWER_EN
B9	VOU656_DATA6	muxctrl_reg59	GPIO6_1	VOU656_DATA6	LCD_DATA_R1	SDIO_CARD_DETECT
F8	VOU656_DATA5	muxctrl_reg60	GPIO6_2	VOU656_DATA5	LCD_DATA_R2	SDIO_CWPR
C8	VOU656_DATA4	muxctrl_reg61	GPIO6_3	VOU656_DATA4	LCD_DATA_R3	SDIO_CCMD
B8	VOU656_DATA3	muxctrl_reg62	GPIO6_4	VOU656_DATA3	LCD_DATA_R4	SDIO_CDATA3
C7	VOU656_DATA2	muxctrl_reg63	GPIO6_5	VOU656_DATA2	LCD_DATA_R5	SDIO_CDATA2
B7	VOU656_DATA1	muxctrl_reg64	GPIO6_6	VOU656_DATA1	LCD_DATA_R6	SDIO_CDATA1
A7	VOU656_DATA0	muxctrl_reg65	GPIO6_7	VOU656_DATA0	LCD_DATA_R7	SDIO_CDATA0

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Table 2-42 describes the software multiplexed pins of the VOU.

Table 2-42 Description of the software multiplexed pins of the VOU

Signal	Direction	Description
GPIO12_6	I/O	GPIO
GPIO12_7	I/O	GPIO
GPIO13_0	I/O	GPIO
GPIO13_1	I/O	GPIO
GPIO4_0	I/O	GPIO
GPIO4_1	I/O	GPIO
GPIO4_2	I/O	GPIO
GPIO4_3	I/O	GPIO
GPIO4_4	I/O	GPIO
GPIO4_5	I/O	GPIO
GPIO4_6	I/O	GPIO
GPIO4_7	I/O	GPIO
GPIO5_0	I/O	GPIO
GPIO5_1	I/O	GPIO
GPIO5_2	I/O	GPIO
GPIO5_3	I/O	GPIO
GPIO5_4	I/O	GPIO
GPIO5_5	I/O	GPIO
GPIO5_6	I/O	GPIO
GPIO5_7	I/O	GPIO
GPIO6_0	I/O	GPIO
GPIO6_1	I/O	GPIO
GPIO6_2	I/O	GPIO
GPIO6_3	I/O	GPIO
GPIO6_4	I/O	GPIO
GPIO6_5	I/O	GPIO
GPIO6_6	I/O	GPIO
GPIO6_7	I/O	GPIO

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Signal	Direction	Description
LCD_CLK	O	Clock output of the LCD interface
LCD_DATA_B0	O	B component output of the LCD interface
LCD_DATA_B1	O	B component output of the LCD interface
LCD_DATA_B2	O	B component output of the LCD interface
LCD_DATA_B3	O	B component output of the LCD interface
LCD_DATA_B4	O	B component output of the LCD interface
LCD_DATA_B5	O	B component output of the LCD interface
LCD_DATA_B6	O	B component output of the LCD interface
LCD_DATA_B7	O	B component output of the LCD interface
LCD_DATA_G0	O	G component output of the LCD interface
LCD_DATA_G1	O	G component output of the LCD interface
LCD_DATA_G2	O	G component output of the LCD interface
LCD_DATA_G3	O	G component output of the LCD interface
LCD_DATA_G4	O	G component output of the LCD interface
LCD_DATA_G5	O	G component output of the LCD interface
LCD_DATA_G6	O	G component output of the LCD interface
LCD_DATA_G7	O	G component output of the LCD interface
LCD_DATA_R0	O	R component output of the LCD interface
LCD_DATA_R1	O	R component output of the LCD interface
LCD_DATA_R2	O	R component output of the LCD interface
LCD_DATA_R3	O	R component output of the LCD interface
LCD_DATA_R4	O	R component output of the LCD interface
LCD_DATA_R5	O	R component output of the LCD interface
LCD_DATA_R6	O	R component output of the LCD interface
LCD_DATA_R7	O	R component output of the LCD interface
SDIO_CARD_DETECT	I	SDIO card detection input, active low
SDIO_CARD_POWER_EN	O	Power enable control output of the SDIO card. The value 1 indicates power-on.
SDIO_CCLK_OUT	O	Working clock output of the SDIO card
SDIO_CCMD	I/O	SDIO card command
SDIO_CDATA0	I/O	Data bus of the SDIO card

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Signal	Direction	Description
SDIO_CDATA1	I/O	Data bus of the SDIO card
SDIO_CDATA2	I/O	Data bus of the SDIO card
SDIO_CDATA3	I/O	Data bus of the SDIO card
SDIO_CWPR	I	Write protection signal output of the SDIO card
VGA_HS	O	VGA horizontal sync output
VGA_VS	O	VGA vertical sync output
VOU1120_CLK	O	Clock output of the BT.1120 interface
VOU1120_DATA0	O	Data output of the BT.1120 interface
VOU1120_DATA1	O	Data output of the BT.1120 interface
VOU1120_DATA10	O	Data output of the BT.1120 interface
VOU1120_DATA11	O	Data output of the BT.1120 interface
VOU1120_DATA12	O	Data output of the BT.1120 interface
VOU1120_DATA13	O	Data output of the BT.1120 interface
VOU1120_DATA14	O	Data output of the BT.1120 interface
VOU1120_DATA15	O	Data output of the BT.1120 interface
VOU1120_DATA2	O	Data output of the BT.1120 interface
VOU1120_DATA3	O	Data output of the BT.1120 interface
VOU1120_DATA4	O	Data output of the BT.1120 interface
VOU1120_DATA5	O	Data output of the BT.1120 interface
VOU1120_DATA6	O	Data output of the BT.1120 interface
VOU1120_DATA7	O	Data output of the BT.1120 interface
VOU1120_DATA8	O	Data output of the BT.1120 interface
VOU1120_DATA9	O	Data output of the BT.1120 interface
VOU1120_HS	O	Horizontal sync output of the BT.1120 interface
VOU1120_VS	O	Vertical sync output of the BT.1120 interface
VOU656_CLK	O	Clock output of the BT.656 interface
VOU656_DATA0	O	Data output of the BT.656 interface
VOU656_DATA1	O	Data output of the BT.656 interface
VOU656_DATA2	O	Data output of the BT.656 interface
VOU656_DATA3	O	Data output of the BT.656 interface

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Signal	Direction	Description
VOU656_DATA4	O	Data output of the BT.656 interface
VOU656_DATA5	O	Data output of the BT.656 interface
VOU656_DATA6	O	Data output of the BT.656 interface
VOU656_DATA7	O	Data output of the BT.656 interface

SIO0

Table 2-43 lists the software multiplexed pins of SIO0.

Table 2-43 Software multiplexed pins of SIO0

Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
J24	SIO0_RCLK	muxctrl_reg66	GPIO7_0	SIO0_RCLK
J26	SIO0_RFS	muxctrl_reg67	GPIO7_1	SIO0_RFS
J28	SIO0_DIN	muxctrl_reg68	GPIO7_2	SIO0_DIN

Table 2-44 describes the software multiplexed pins of SIO0.

Table 2-44 Description of the software multiplexed pins of SIO0

Signal	Direction	Description
GPIO7_0	I/O	GPIO
GPIO7_1	I/O	GPIO
GPIO7_2	I/O	GPIO
SIO0_DIN	I	Data input of the I^2S or PCM interface
SIO0_RCLK	I/O	Bit stream clock of the I^2S or PCM interface
SIO0_RFS	I/O	I^2S receive audio channel select signal (connected to the ADC interface) or PCM frame sync signal

SIO1

Table 2-45 lists the software multiplexed pins of SIO1.

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Table 2-45 Software multiplexed pins of SIO1

Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
K27	SIO1_RCLK	muxctrl_reg69	GPIO7_3	SIO1_RCLK
L24	SIO1_RFS	muxctrl_reg70	GPIO7_4	SIO1_RFS
L26	SIO1_DIN	muxctrl_reg71	GPIO7_5	SIO1_DIN

Table 2-46 describes the software multiplexed pins of SIO1.

Table 2-46 Description of the software multiplexed pins of SIO1

Signal	Direction	Description
GPIO7_3	I/O	GPIO
GPIO7_4	I/O	GPIO
GPIO7_5	I/O	GPIO
SIO1_DIN	I	Data input of the I^2S or PCM interface
SIO1_RCLK	I/O	Bit stream clock of the I^2S or PCM interface
SIO1_RFS	I/O	I^2S receive audio channel select signal (connected to the ADC interface) or PCM frame sync signal

SIO2

Table 2-47 lists the software multiplexed pins of SIO2.

Table 2-47 Software multiplexed pins of SIO2

Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
B24	SIO2_XCLK	muxctrl_reg72	GPIO7_6	SIO2_XCLK
E23	SIO2_XFS	muxctrl_reg73	GPIO7_7	SIO2_XFS
A25	SIO2_RCLK	muxctrl_reg74	GPIO8_0	SIO2_RCLK
C25	SIO2_RFS	muxctrl_reg75	GPIO8_1	SIO2_RFS
F24	SIO2_DIN	muxctrl_reg76	GPIO8_2	SIO2_DIN

Table 2-48 describes the software multiplexed pins of SIO2.

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Table 2-48 Description of the software multiplexed pins of SIO2

Signal	Direction	Description
GPIO7_6	I/O	GPIO
GPIO7_7	I/O	GPIO
GPIO8_0	I/O	GPIO
GPIO8_1	I/O	GPIO
GPIO8_2	I/O	GPIO
SIO2_DIN	I	Data input of the I^2S or PCM interface
SIO2_RCLK	I/O	Bit stream clock of the I^2S or PCM interface
SIO2_RFS	I/O	I^2S receive audio channel select signal (connected to the ADC interface) or PCM frame sync signal
SIO2_XCLK	I/O	Bit stream clock of the I^2S or PCM interface
SIO2_XFS	I/O	I^2S transmit audio channel select signal (connected to the DAC interface) or PCM frame sync signal

SPI

Table 2-49 lists the software multiplexed pins of the SPI.

Table 2-49 Software multiplexed pins of the SPI

Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	Multiplexing Signal 2	Multiplexing Signal 3	Multiplexing Signal 4	Multiplexing Signal 5
AC27	SPI_SCLK	muxctrl_reg77	GPIO8_3	SPI_SCLK	None	None	None	None
AB27	SPI_SDO	muxctrl_reg78	GPIO8_4	SPI_SDO	None	None	None	None
AC28	SPI_SDI	muxctrl_reg79	GPIO8_5	SPI_SDI	None	None	None	None
AE28	SPI_CSN0	muxctrl_reg80	GPIO8_6	SPI_CSN0	None	None	None	None
AD26	SPI_CSN3	muxctrl_reg81	SPI_CSN3	NF_BOOT_PIN4	CLK_TEST_OUT0	CLK_TEST_OUT1	CLK_TEST_OUT2	CLK_TEST_OUT3

Table 2-50 describes the software multiplexed pins of the SPI.

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Table 2-50 Description of the software multiplexed pins of the SPI

Signal	Direction	Description
CLK_TEST_OUT0	O	Main test clock output
CLK_TEST_OUT1	O	Main test clock output
CLK_TEST_OUT2	O	Main test clock output
CLK_TEST_OUT3	O	Main test clock output
GPIO8_3	I/O	GPIO
GPIO8_4	I/O	GPIO
GPIO8_5	I/O	GPIO
GPIO8_6	I/O	GPIO
NF_BOOT_PIN4	I	NAND flash type configuration, active only during power-on. For details, see the description of NF_BOOT_PIN0.
SPI_CSN0	I/O	SPI CS 0 output
SPI_CSN3	O	SPI CS 1 output
SPI_SCLK	I/O	SPI clock
SPI_SDI	I	SPI data input
SPI_SDO	O	SPI data output

I2C

Table 2-51 lists the software multiplexed pins of the I^2C interface.

Table 2-51 Software multiplexed pins of the I^2C interface

Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
M24	I2C_SDA	muxctrl_reg82	GPIO13_2	I2C_SDA
M23	I2C_SCL	muxctrl_reg83	GPIO13_3	I2C_SCL

Table 2-52 describes the software multiplexed pins of the I^2C interface.

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Table 2-52 Description of the software multiplexed pins of the I^2C interface

Signal	Direction	Description
GPIO13_2	I/O	GPIO
GPIO13_3	I/O	GPIO
I2C_SCL	I/O	I^2C bus clock, OD output
I2C_SDA	I/O	I^2C bus data/address, OD output

UART1

Table 2-53 lists the software multiplexed pins of UART1.

Table 2-53 Software multiplexed pins of UART1

Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
P1	UART1_RTSN	muxctrl_reg84	GPIO9_0	UART1_RTSN
R3	UART1_RXD	muxctrl_reg85	GPIO9_1	UART1_RXD
P5	UART1_CTSN	muxctrl_reg86	GPIO9_2	UART1_CTSN
P6	UART1_TXD	muxctrl_reg87	GPIO9_3	UART1_TXD

Table 2-54 describes the software multiplexed pins of UART1.

Table 2-54 Description of the software multiplexed pins of UART1

Signal	Direction	Description
GPIO9_0	I/O	GPIO
GPIO9_1	I/O	GPIO
GPIO9_2	I/O	GPIO
GPIO9_3	I/O	GPIO
UART1_CTSN	I	Modem state input: clear-to-send, active low
UART1_RTSN	O	Modem state output: request-to-send, active low. The reset value is 0.
UART1_RXD	I	UART1 data receive
UART1_TXD	O	UART1 data transmit

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GMAC

Table 2-55 lists the software multiplexed pins of the GMAC interface.

Table 2-55 Software multiplexed pins of the GMAC interface

Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	Multiplexing Signal 2	Multiplexing Signal 3	Multiplexing Signal 4
B16	RGMII_TXD0	muxctrl_reg88	PLL_TEST_OUT0	RGMII_TXD0	PLL_TEST_OUT1	PLL_TEST_OUT2	PLL_TEST_OUT3
C17	RGMII_TXCK	muxctrl_reg89	RGMII_TXCK	GPIO8_7	None	None	None
E18	RGMII_CRS	muxctrl_reg90	GPIO13_4	RGMII_CRS	RGMII_RXER	None	None
F18	RGMII_COL	muxctrl_reg91	GPIO13_5	RGMII_COL	RGMII_TXER	None	None

Table 2-56 describes the software multiplexed pins of the GMAC interface.

Table 2-56 Description of the software multiplexed pins of the GMAC interface

Signal	Direction	Description
GPIO13_4	I/O	GPIO
GPIO13_5	I/O	GPIO
GPIO8_7	I/O	GPIO
PLL_TEST_OUT0	O	PLL test clock output
PLL_TEST_OUT1	O	PLL test clock output
PLL_TEST_OUT2	O	PLL test clock output
PLL_TEST_OUT3	O	PLL test clock output
RGMII_COL	I	Collision indicator signal of the RGMII
RGMII_CRS	I	Carrier sense signal of the RGMII
RGMII_RXER	I	Receive error signal of the RGMII
RGMII_TXCK	I	Transmit clock of the RGMII (active on both edges) or MII
RGMII_TXD0	O	Transmit data of the RGMII or MII
RGMII_TXER	O	Transmit error signal of the RGMII

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IR

Table 2-57 lists the software multiplexed pin of the IR.

Table 2-57 Software multiplexed pin of the IR

Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
L2	IR_IN	muxctrl_reg92	IR_IN	GPIO9_4

Table 2-58 describes the software multiplexed pins of the IR.

Table 2-58 Description of the software multiplexed pin of the IR

Signal	Direction	Description
GPIO9_4	I/O	GPIO
IR_IN	I	IR input

NFC

Table 2-59 lists the software multiplexed pins of the NFC.

Table 2-59 Software multiplexed pins of the NFC

Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
AC5	NF_DQ0	muxctrl_reg93	NF_DQ0	GPIO9_5
AF1	NF_DQ1	muxctrl_reg94	NF_DQ1	GPIO9_6
AE3	NF_DQ2	muxctrl_reg95	NF_DQ2	GPIO9_7
AE2	NF_DQ3	muxctrl_reg96	NF_DQ3	GPIO10_0
AD3	NF_DQ4	muxctrl_reg97	NF_DQ4	GPIO10_1
AD2	NF_DQ5	muxctrl_reg98	NF_DQ5	GPIO10_2
AD1	NF_DQ6	muxctrl_reg99	NF_DQ6	GPIO10_3
AC3	NF_DQ7	muxctrl_reg100	NF_DQ7	GPIO10_4
AC2	NF_RDY0	muxctrl_reg101	NF_RDY0	GPIO10_5
AB3	NF_RDY1	muxctrl_reg102	NF_RDY1	GPIO10_6

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Table 2-60 describes the software multiplexed pins of the NFC.

Table 2-60 Description of the software multiplexed pins of the NFC

Signal	Direction	Description
GPIO10_0	I/O	GPIO
GPIO10_1	I/O	GPIO
GPIO10_2	I/O	GPIO
GPIO10_3	I/O	GPIO
GPIO10_4	I/O	GPIO
GPIO10_5	I/O	GPIO
GPIO10_6	I/O	GPIO
GPIO9_5	I/O	GPIO
GPIO9_6	I/O	GPIO
GPIO9_7	I/O	GPIO
NF_DQ0	I/O	Data bus of the NAND flash
NF_DQ1	I/O	Data bus of the NAND flash
NF_DQ2	I/O	Data bus of the NAND flash
NF_DQ3	I/O	Data bus of the NAND flash
NF_DQ4	I/O	Data bus of the NAND flash
NF_DQ5	I/O	Data bus of the NAND flash
NF_DQ6	I/O	Data bus of the NAND flash
NF_DQ7	I/O	Data bus of the NAND flash
NF_RDY0	I	Status indicator signal of the NAND flash. 1: idle 0: busy
NF_RDY1	I	Status indicator signal of the NAND flash. 1: idle 0: busy

SFC

Table 2-61 lists the software multiplexed pins of the SFC.

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Table 2-61 Software multiplexed pins of the SFC

Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
AG3	SFC_DIO	muxctrl_reg103	SFC_DIO	GPIO13_6
AH2	SFC_WP_IO2	muxctrl_reg104	SFC_WP_IO2	GPIO10_7
AF3	SFC_DOI	muxctrl_reg105	SFC_DOI	GPIO13_7
AG2	SFC_HOLD_IO3	muxctrl_reg106	SFC_HOLD_IO3	GPIO14_4

Table 2-62 describes the software multiplexed pins of the SFC.

Table 2-62 Description of the software multiplexed pins of the SFC

Signal	Direction	Description
GPIO10_7	I/O	GPIO
GPIO13_6	I/O	GPIO
GPIO13_7	I/O	GPIO
GPIO14_4	I/O	GPIO
SFC_DIO	I/O	Data output signal in standard SPI mode Data I/O signal in dual SPI mode Data I/O signal in quad SPI mode
SFC_DOI	I/O	Data input signal in standard SPI mode Data I/O signal in dual SPI mode Data I/O signal in quad SPI mode
SFC_HOLD_IO3	I/O	Hold function in standard SPI mode, active low Hold function in dual SPI mode, active low Data I/O signal in quad SPI mode
SFC_WP_IO2	I/O	Write protect function in standard SPI mode, active low Write protect function in dual SPI mode, active low Data I/O signal in quad SPI mode

USB

Table 2-63 lists the software multiplexed pins of the USB port.

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Table 2-63 Software multiplexed pins of the USB port

Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
A9	USB0_OVRCUR	muxctrl_reg107	GPIO14_0	USB0_OVRCUR
C10	USB0_PWREN	muxctrl_reg108	GPIO14_1	USB0_PWREN
B10	USB1_OVRCUR	muxctrl_reg109	GPIO14_2	USB1_OVRCUR
E11	USB1_PWREN	muxctrl_reg110	GPIO14_3	USB1_PWREN

Table 2-64 describes the software multiplexed pins of the USB port.

Table 2-64 Description of the software multiplexed pins of the USB port

Signal	Direction	Description
GPIO14_0	I/O	GPIO
GPIO14_1	I/O	GPIO
GPIO14_2	I/O	GPIO
GPIO14_3	I/O	GPIO
USB0_OVRCUR	I	Overcurrent indicator signal of USB port 0, configurable level, and active high by default
USB0_PWREN	O	Power control output of USB port 0, configurable level, and active low by default
USB1_OVRCUR	I	Overcurrent indicator signal of USB port 1, configurable level, and active high by default
USB1_PWREN	O	Power control output of USB port 1, configurable level, and active low by default

GPIO

Table 2-65 lists the software multiplexed pins of the GPIO interface.

Table 2-65 Software multiplexed pins of the GPIO interface

Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
M1	GPIO11_0	muxctrl_reg111	GPIO11_0	UART3_RXD
M2	GPIO11_1	muxctrl_reg112	GPIO11_1	UART3_TXD

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Table 2-66 describes the software multiplexed pins of the GPIO interface.

Table 2-66 Description of the software multiplexed pins of the GPIO interface

Signal	Direction	Description
GPIO11_0	I/O	GPIO
GPIO11_1	I/O	GPIO
UART3_RXD	I	UART3 data receive
UART3_TXD	O	UART3 data transmit

SATA

Table 2-67 lists the software multiplexed pins of the SATA interface.

Table 2-67 Software multiplexed pins of the SATA interface

Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
T3	SATA_LED_N0	muxctrl_reg113	GPIO11_2	SATA_LED_N0
R2	SATA_LED_N1	muxctrl_reg114	GPIO11_3	SATA_LED_N1

Table 2-68 describes the software multiplexed pins of the SATA interface.

Table 2-68 Description of the software multiplexed pins of the SATA interface

Signal	Direction	Description
GPIO11_2	I/O	GPIO
GPIO11_3	I/O	GPIO
SATA_LED_N0	O	LED indicator of the SATA0 port, active low
SATA_LED_N1	O	LED indicator of the SATA1 port, active low

HDMI

Table 2-69 lists the software multiplexed pins of the HDMI.

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Table 2-69 Software multiplexed pins of the HDMI

Pin	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
J27	HDMI_HOTPLUG	muxctrl_reg115	GPIO11_4	HDMI_HOTPLUG
G28	HDMI_CEC	muxctrl_reg116	GPIO11_5	HDMI_CEC
H27	HDMI_SDA	muxctrl_reg117	GPIO11_6	HDMI_SDA
H26	HDMI_SCL	muxctrl_reg118	GPIO11_7	HDMI_SCL

Table 2-70 describes the software multiplexed pins of the HDMI.

Table 2-70 Description of the software multiplexed pins of the HDMI

Signal	Direction	Description
GPIO11_4	I/O	GPIO
GPIO11_5	I/O	GPIO
GPIO11_6	I/O	GPIO
GPIO11_7	I/O	GPIO
HDMI_CEC	I/O	Channel control signal of the HDMI
HDMI_HOTPLUG	I	Hot plug signal of the HDMI
HDMI_SCL	I/O	Dedicated I^2C bus clock for the HDMI, OD output
HDMI_SDA	I/O	Dedicated I^2C bus data/address for the HDMI, OD output

2.5 Hardware Multiplexed Pins

VOU

Table 2-71 lists the hardware multiplexed pin of the VOU.

Table 2-71 Hardware multiplexed pin of the VOU

Pin	Pad Signal	Multiplexing Signal 1 (power_on == 1'b1)
E2	LCD_DV	NF_BOOT_PIN0

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Table 2-72 describes the hardware multiplexed pin of the VOU.

Table 2-72 Description of the hardware multiplexed pin of the VOU

Signal	Direction	Description
NF_BOOT_PIN0	I	NAND flash type configuration, active only during power-on. NF_BOOT_PIN0, NF_BOOT_PIN1, NF_BOOT_PIN2, NF_BOOT_PIN3, and NF_BOOT_PIN4 work together for setting the PAGE_SEIZE, ECC_TYPE, BLOCK_SIZE, and ADDR_NUM parameters of the connected NAND flash. For details, see "Mapping Between Pin Values and NAND Flash Types" in section 4.2.3.3.

SIO2

Table 2-73 lists the hardware multiplexed pin of SIO2.

Table 2-73 Hardware multiplexed pin of SIO2

Pin	Pad Signal	Multiplexing Signal 1 (power_on == 1'b1)
E24	SIO2_DOUT	NF_BOOT_PIN1

Table 2-74 describes the hardware multiplexed pin of SIO2.

Table 2-74 Description of the hardware multiplexed pin of SIO2

Signal	Direction	Description
NF_BOOT_PIN1	I	NAND flash type configuration, active only during power-on. For details, see the description of NF_BOOT_PIN0.

SPI

Table 2-75 lists the hardware multiplexed pins of the SPI.

Table 2-75 Hardware multiplexed pins of the SPI

Pin	Pad Signal	Multiplexing Signal 1 (power_on == 1'b1)
AD27	SPI_CSN1	NF_BOOT_PIN2

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Pin	Pad Signal	Multiplexing Signal 1 (power_on == 1'b1)
AC24	SPI_CSN2	NF_BOOT_PIN3
AD26	SPI_CSN3	NF_BOOT_PIN4

Table 2-76 describes the hardware multiplexed pins of the SPI.

Table 2-76 Description of the hardware multiplexed pins of the SPI

Signal	Direction	Description
NF_BOOT_PIN2	I	NAND flash type configuration, active only during power-on. For details, see the description of NF_BOOT_PIN0.
NF_BOOT_PIN3	I	NAND flash type configuration, active only during power-on. For details, see the description of NF_BOOT_PIN0.
NF_BOOT_PIN4	I	NAND flash type configuration, active only during power-on. For details, see the description of NF_BOOT_PIN0.

MDIO

Table 2-77 lists the hardware multiplexed pin of the MDIO interface.

Table 2-77 Hardware multiplexed pin of the MDIO interface

Pin	Pad Signal	Multiplexing Signal 1 (power_on == 1'b1)
B18	MDCK	JTAG_SEL0

Table 2-78 describes the hardware multiplexed pin of the MDIO interface.

Table 2-78 Description of the hardware multiplexed pin of the MDIO interface

Signal	Direction	Description
JTAG_SEL0	I	JTAG function select. The definitions of {JTAG_SEL1, JTAG_SEL0} are as follows: 00: A9 01: reserved 10: SATA 11: reserved

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NFC

Table 2-79 lists the hardware multiplexed pins of the NFC.

Table 2-79 Hardware multiplexed pins of the NFC

Pin	Pad Signal	Multiplexing Signal 1 (power_on == 1'b1)
AA6	NF_REN	JTAG_SEL1
AA5	NF_CLE	BOOT_SEL0
Y6	NF_ALE	BOOT_SEL1
Y5	NF_WEN	BOOTROM_SEL

Table 2-80 describes the hardware multiplexed pins of the NFC.

Table 2-80 Description of the hardware multiplexed pins of the NFC

Signal	Direction	Description
JTAG_SEL1	I	JTAG function select. The definitions of {JTAG_SEL1, JTAG_SEL0} are as follows: 00: A9 01: reserved 10: SATA 11: reserved
BOOT_SEL0	I	Boot mode select. BOOT_SEL0 works with BOOT_SEL1 for selecting the boot mode. The definitions of {BOOT_SEL1, BOOT_SEL0} are as follows: 00: storage space of the SPI flash 01: reserved 10: storage space of the NAND flash 11: reserved
BOOT_SEL1	I	Boot mode select. For details, see the description of BOOT_SEL0.
BOOTROM_SEL	I	BOOTROM boot. When this signal is set to 1, the BOOTROM boot mode is selected. In this case, if the communication over the serial port times out, the boot program is jumped to another storage space based on the values of BOOT_SEL1 and BOOT_SEL0.

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2.6 Electrical Specifications

2.6.1 Power Consumption Specifications

Table 2-81 describes the power consumption specifications of Hi3521 andTable 2-82describes the power consumption specifications of Hi3520A.

CAUTION

- The values for power consumption parameters are provided based on typical application scenarios.
- Design board power supplies by following the *Hi3521/Hi3520A Hardware Design User Guide*.

Table 2-81 Power consumption specifications of Hi3521

Power Type	Description	Typ	Max	Unit
Core power	Core power	2500	3900	mA
3.3 V power	Interface power	300	350	mA
2.5 V power	Interface power	30	50	mA
DVDD1518 power	DDR interface power	400	460	mA

Table 2-82 Power consumption specifications of Hi3520A

Power Type	Description	Typ	Max	Unit
Core power	Core power	2000	2900	mA
3.3 V power	Interface power	300	350	mA
2.5 V power	Interface power	30	50	mA
DVDD1518 power	DDR interface power	370	400	mA

2.6.2 Temperature and Thermal Resistance Parameters

Table 2-83 describes the temperature and thermal resistance parameters.

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NOTE

- The thermal resistance is provided in compliance with the JEDEC JESD51-2 standard. The actual system design and environment may be different.
- The chip junction temperature is proportional to the chip power consumption. Ensure that the junction temperature is appropriate to match power supplies.
- Design heat dissipation by following the *Hi3521/Hi3520A Hardware Design User Guide*.

Table 2-83 Temperature and thermal resistance parameters

Parameter	Symbol	Min	Typ	Max	Unit
Recommended ambient temperature	T_A	0	None	70	°C
Limited junction temperature	T_{JMAX}	–20	None	+105	°C
Junction-to-ambient thermal resistance	θ_{JA}	None	17.8	None	°C/W
Junction-to-board thermal resistance	θ_{JB}	None	4.1	None	°C/W
Junction-to-case thermal resistance	θ_{JC}	None	0.37	None	°C/W

2.6.3 Working Conditions

Table 2-84 describes the working conditions.

Table 2-84 Working conditions

Pin	Description	Min	Typ	Max
DVDD10	Core power	0.95 V	1.0 V	1.05 V
DVDD33	I/O power	3.0 V	3.3 V	3.6 V
DVDD1518	DDR2 I/O power	1.7 V	1.8 V	1.9 V
	DDR 3 I/O power	1.425 V	1.5 V	1.575 V
	DDR3L I/O power	1.2825 V	1.35 V	1.4175 V
DDR_REF	DDR2 reference voltage	0.49 x D VDD1518	0.5 x D VDD1518	0.51 x D VDD1518
	DDR3 reference voltage	0.49 x D VDD1518	0.5 x D VDD1518	0.51 x D VDD1518
DVDD10_USB	USB digital power	–7%	1.0 V	+10%
AVDD33_USB	USB analog power	–7%	3.3 V	+10%
VDD10_PLL1	PLL1 digital power	–10%	1.0 V	+10%
AVDD33_PLL1	PLL1 analog power	–10%	3.3 V	+10%

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Pin	Description	Min	Typ	Max
VDDREF10_PLL234	Digital power of PLL2, PLL3, or PLL4	–10%	1.0 V	+10%
VDD10_PLL234	Digital power of PLL2, PLL3, or PLL4	–10%	1.0 V	+10%
AVDD33_PLL234	Analog power of PLL2, PLL3, or PLL4	–10%	3.3 V	+10%
SATA_VP10	SATA 1.0 V power	–10%	1.0 V	+10%
SATA_VP25	SATA 2.5 V power	–10%	2.5 V	+10%
VDD25_EFUSE	eFUSE 2.5 V power	–10%	2.5 V	+10%
AVCC10_HDMI	HDMI 1.0 V analog power	–5%	1.0 V	+5%
DVDD2533	ETH I/O digital power	–10%	3.3/2.5 V	+10%
AVDD33_VDAC0	VDAC0 analog power	–10%	3.3 V	+10%
AVDD33_VDAC1	VDAC1 analog power	–10%	3.3 V	+10%

2.6.4 Sequence of Power-On and Power-Off

To avoid overcurrent for I/O pins during power-on, you are advised to power on DVDD33 and DVDD10 in sequence. There is no requirement on the power-off sequence.

2.6.5 DC/AC Electrical Specifications

Table 2-85 describes the direct current (DC) electrical specifications.

Table 2-85 DC electrical specifications (DVDD33 = 3.3 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DVDD33	Interface voltage	3.0	3.3	3.6	V	None
V_{IH}	Input high voltage	2.0	None	5.5	V	The 5 V input voltage is supported. The maximum input voltage is DVDD33 + 0.3 V. The ETH signals and VOU1120_CLK do not support the 5 V input voltage.
V_{IL}	Input low voltage	–0.3	None	0.8	V	None

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Symbol	Description	Min	Typ	Max	Unit	Remarks
I_L	Input leakage current	None	None	±10	μA	None
I_{OZ}	Tristate output leakage current	None	None	±10	μA	None
V_{OH}	Output high voltage	2.4	None	None	V	None
V_{OL}	Output low voltage	None	None	0.4	V	None
R_{PU}	Internal pull-up resistor	27	38	59	kΩ	None
R_{PD}	Internal pull-down resistor	31	46	80	kΩ	None

Table 2-86 describes the DC electrical specifications in DDR2 SSTL18 mode.

Table 2-86 DC electrical specifications in DDR2 SSTL18 mode (DVDD1518 = 1.8 V)

Symbol	Parameter	Min	Typ	Max	Unit	Remarks
DVDD1518	Interface voltage	1.7	1.8	1.9	V	None
Vref	Reference voltage	833	900	969	mV	(0.49 to 0.51) x DVDD1518
VTT	Termination voltage	Vref – 40	Vref	Vref + 40	mV	None
$V_{IH(DC)}$	Input high voltage	Vref + 0.125	None	DVDD1518 + 0.3	V	None
$V_{IL(DC)}$	Input low voltage	–0.3	None	Vref – 0.125	V	None
I_{OH}	Output high current	8.1	None	None	mA	None
I_{OL}	Output low current	|–8.1|	None	None	mA	None
V_{OH}	Output high voltage	DVDD1518 – 0.28	None	DVDD1518 (1 + 10%)	V	None
V_{OL}	Output low voltage	0	None	0.28	V	I_{OH} = 13.4 mA

Table 2-87 describes the alternating current (AC) electrical specifications in DDR2 mode.

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Table 2-87 AC electrical specifications in DDR2 mode (DVDD1518 = 1.8 V)

Symbol	Description	400–533 Mbit/s		667–800 Mbit/s		Unit	Remarks
		Min	Max	Min	Max		
$V_{IH(AC)}$	AC input high voltage	Vref + 0.25	None	Vref + 0.2	None	V	None
$V_{IL(AC)}$	AC input low voltage	None	Vref – 0.25	None	Vref – 0.2	V	None

Table 2-88 describes the DC electrical specifications in DDR3 mode.

Table 2-88 DC electrical specifications in DDR3 mode (DVDD1518 = 1.5 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DVDD1518	Interface voltage	1.425	1.5	1.575	V	None
Vref	Reference voltage	698	750	803	mV	(0.49 to 0.51) x DVDD1518
VTT	Termination voltage	698	750	803	mV	None
$V_{IH(DC)}$	Input high voltage	Vref + 0.1	None	DVDD1518 + 0.3	V	None
$V_{IL(DC)}$	Input low voltage	–0.3	None	Vref – 0.1	V	None
V_{OH}	Output high voltage	0.8xDVDD1518	None	(1 + 0.1) x DVDD1518	V	None
V_{OL}	Output low voltage	0	None	0.2xDVDD1518	V	None
I_{OH}	Output high current	|8|	None	None	mA	None
I_{OL}	Output low current	|–8|	None	None	mA	None

Table 2-89 describes the AC electrical specifications in DDR3 mode.

Table 2-89 AC electrical specifications in DDR3 mode (DVDD1518 = 1.5 V)

Symbol	Description	Min	Max	Unit	Remarks
$V_{IH(AC)}$	Input high voltage	Vref + 0.175	DVDD1518 + 0.3	V	None
$V_{IL(AC)}$	Input low voltage	None	Vref – 0.175	V	None
V_{OH}	Output high voltage	VTT + 0.1 x DVDD1518	None	V	None

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V_{OL}	Output low voltage	None	VTT – 0.1 x DVDD1518	V	None

2.7 PCB Design Recommendations

For details about the printed circuit board (PCB) design, see the *Hi3521 Hardware Design User Guide*.

2.8 Interface Timings

2.8.1 DDR Interface Timings

2.8.1.1 Write Timings

Write Timings of dqs_out Relative to dq_out

In the write timing of dqs_out relative to dq_out, the major parameters are tDS and tDH. In DDR2-800, the value of tDS is 0.05 ns, and the value of tDH is 0.125 ns.

Figure 2-9 Write timing of dqs_out relative to dq_out for the DDR2

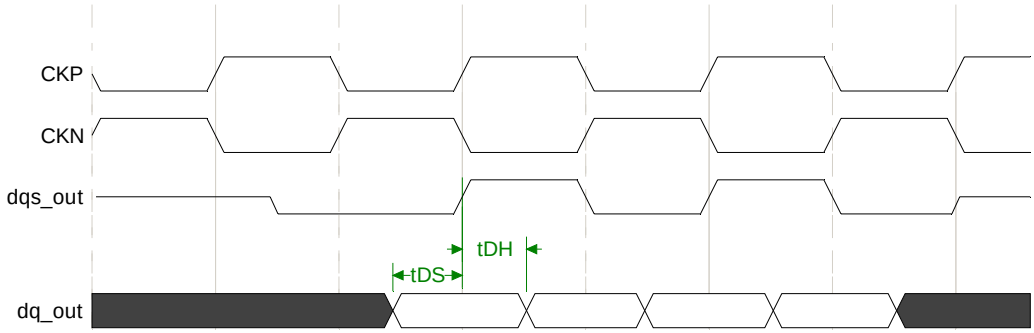
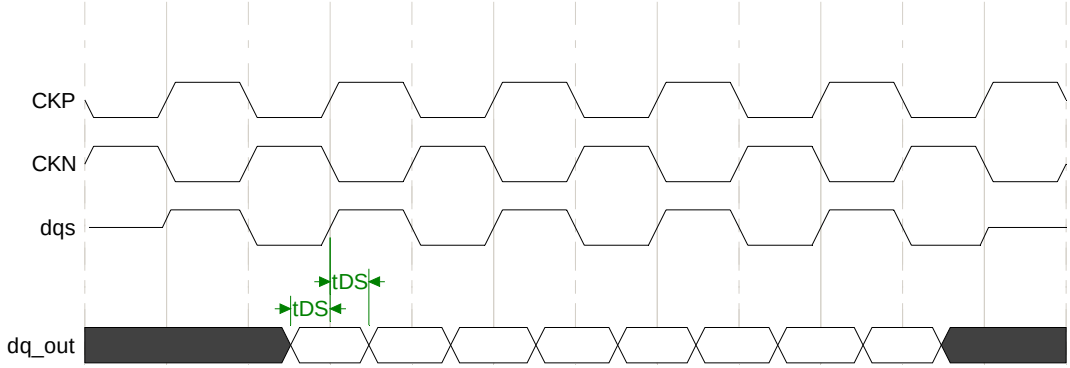


Figure 2-10 Write timing of dqs_out relative to dq_out for the DDR3



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Write Timings of dqs_out Relative to CK

Figure 2-11 shows the write timing of dqs_out relative to CK for the DDR2, and Figure 2-12 shows the write timing of dqs_out relative to CK for the DDR3.

Figure 2-11 Write timing of dqs_out relative to CK for the DDR2

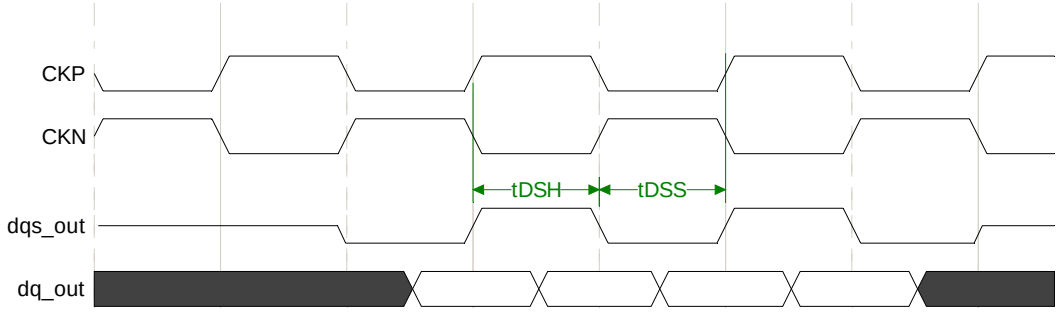
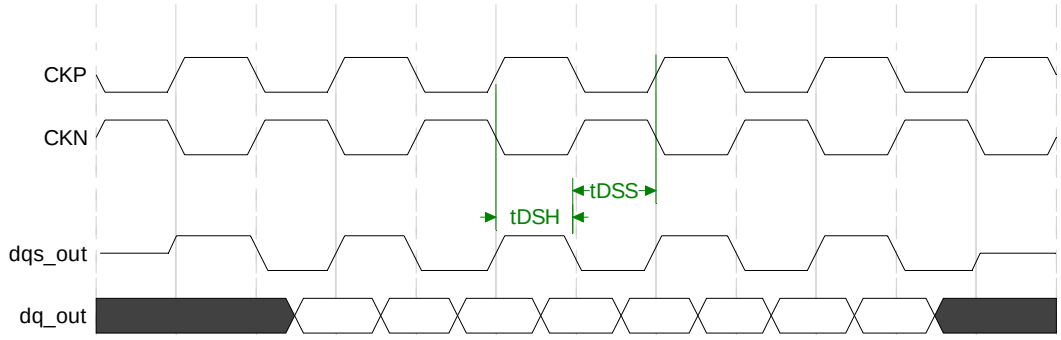


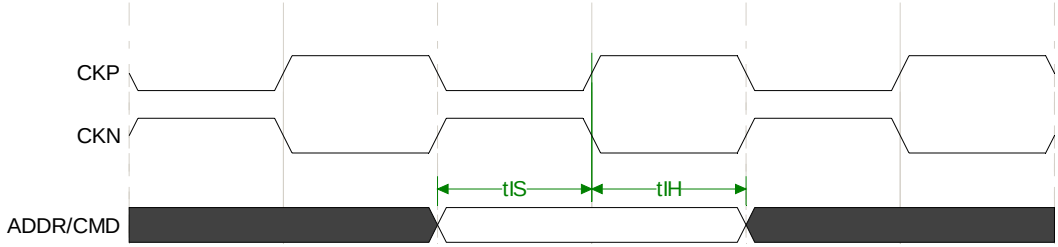
Figure 2-12 Write timing of dqs_out relative to CK for the DDR3



Write Timing of CMD/ADDR Relative to CK

Figure 2-13 shows the write timing of CMD/ADDR relative to CK.

Figure 2-13 Write timing of CMD/ADDR relative to CK



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2.8.1.2 Read Timings

Read Timing of CMD/ADDR Relative to CK

The read timing of CMD/ADDR relative to CK is the same as the "Write Timing of CMD/ADDR Relative to CK".

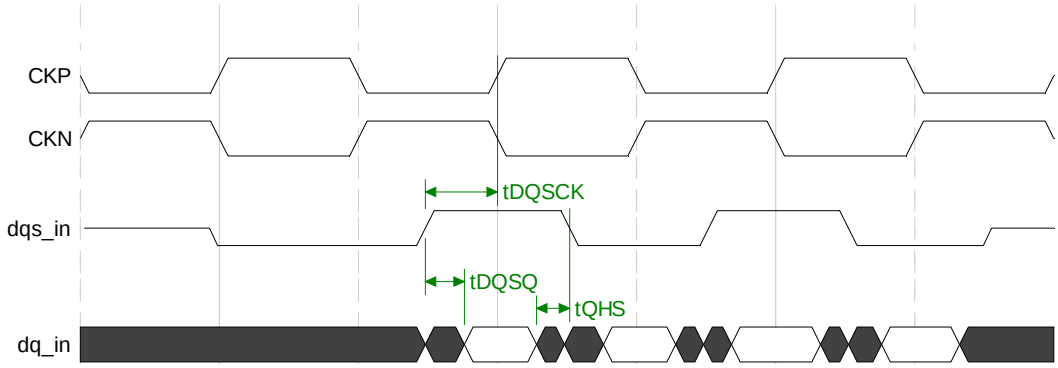
Read Timings of dqs_in Relative to dq_in

The read timings of dqs_in relative to dq_in are classified into the DDRn SDRAM output timing, dqs_in timing on the DDR PHY side, and dq_in timing on the DDR PHY side.

For the DDR SDRAM output timing, the phases of DQS and CK are the same in the ideal condition; however, there is a tDQSCK skew between DQS and CK. The value of tDQSCK is 0.35 ns. tDQSQ is the jitter of the last valid DQ relative to DQS and its value is 0.2 ns; tQHS is the jitter of the first valid DQ relative to DQS and its value is 0.3 ns.

Figure 2-14 shows the output timing of the DDRn SDRAM.

Figure 2-14 Output timing of the DDRn SDRAM



2.8.1.3 Timing Parameters

The timings of the DDR interface comply with the JEDEC standards including JESD79-2E and JESD79-3B standards. All the timings in this document are output on the DDR PHY side.

The Hi3521 is based on the timing parameters of the DDR2-800 and DDR3-1066 SDRAMs.

Table 2-90 and Table 2-91 describe the clock parameters of the DDR2-800 SDRAM.

Table 2-92 and Table 2-93 describe the clock parameters of the DDR3-1066 SDRAM.

Table 2-90 DDR2 clock parameters

Parameter	Typ	Unit
DDR clock frequency	400.00	MHz
PLL jitter	0.200	ns
PLL duty ratio	48.000	%
Clock skew	0.100	ns

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Table 2-91 describes the parameters of the DDR2 SDRAM.

Table 2-91 Parameters for the DDR2-800 SDRAM

Parameter	Symbol	Typ	Unit
Setup time, DQS falling edge to DDR clock	tDSS	0.2	tCK
Hold time, DQS falling edge to DDR clock	tDSH	0.2	tCK
Setup time, DQ/DM to DQS	tDS	0.050	ns
Hold time, DQ/DM to DQS	tDH	0.125	ns
Skew between DQS and DQ	tDQSQ	0.200	ns
Data hold skew	tQHS	0.300	ns
Setup time, ADDR/CMD to DDR clock	tIS	0.175	ns
Hold time, ADDR/CMD to DDR clock	tIH	0.250	ns
Skew of DQS (output) to DDR clock	tDQSCK	0.350	ns

NOTE

For details about some timing parameters, see the following timing diagrams.

Table 2-92 DDR3 clock parameters

Parameter	Typ	Unit
DDR clock frequency	620.00	MHz
PLL jitter	0.200	ns
PLL duty ratio	47.000	%
Clock skew	0.100	ns

Table 2-93 Parameters for the DDR3-1066 SDRAM

Parameter	Symbol	Typ	Unit
Setup time, DQS falling edge to DDR clock	tDSS	0.2	tCK
Hold time, DQS falling edge to DDR clock	tDSH	0.2	tCK
Setup time, DQ/DM to DQS	tDS	0.025	ns
Hold time, DQ/DM to DQS	tDH	0.100	ns
Skew between DQS and DQ	tDQSQ	0.150	ns
Setup time, ADDR/CMD to DDR clock	tIS	0.125	ns

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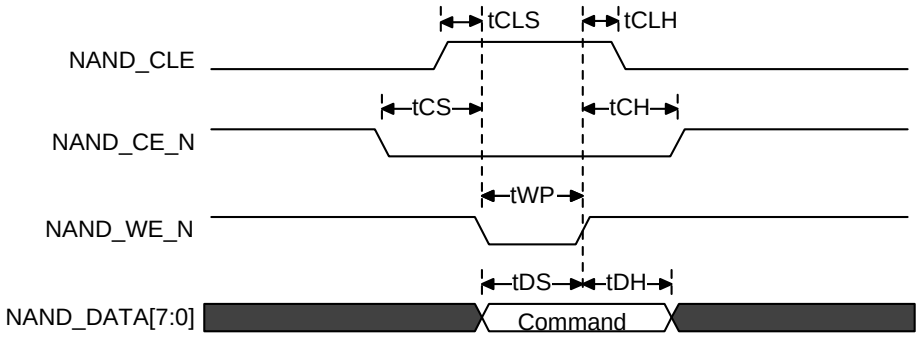
Parameter	Symbol	Typ	Unit
Hold time, ADDR/CMD to DDR clock	tIH	0.200	ns
Skew of DQS (output) to DDR clock	tDQSCK	0.300	ns

2.8.2 NANDC Interface Timings

Command Cycle Timing

Figure 2-15 shows the NANDC command cycle timing.

Figure 2-15 NANDC command cycle timing



NOTE

The level widths of NAND_WE_N and NAND_RE_N can be set by configuring the NF_PULSE_WIDTH register of the NANDC. Some parameters in the timing diagrams of the NANDC interface vary depending on the settings of NF_PULSE_WIDTH. In the following tables, these parameters are marked with "Configurable."

Table 2-94 describes NANDC command cycle timing parameters.

Table 2-94 NANDC command cycle timing parameters

Parameter	Symbol	Mim	Max	Unit	Remarks
Setup time of NAND_CLE	tCLS	0	None	ns	None
Hold time of NAND_CLE	tCLH	10	None	ns	Configurable
Setup time of NAND_CE_N	tCS	0	None	ns	None
Hold time of NAND_CE_N	tCH	10	None	ns	Configurable
Pulse width of NAND_WE_N	tWP	15	None	ns	Configurable
Data setup time	tDS	10	None	ns	Configurable

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Parameter	Symbol	Mim	Max	Unit	Remarks
Data hold time	tDH	10	None	ns	Configurable

Address Cycle Timing

Figure 2-16 shows the NANDC address cycle timing.

Figure 2-16 NANDC address cycle timing

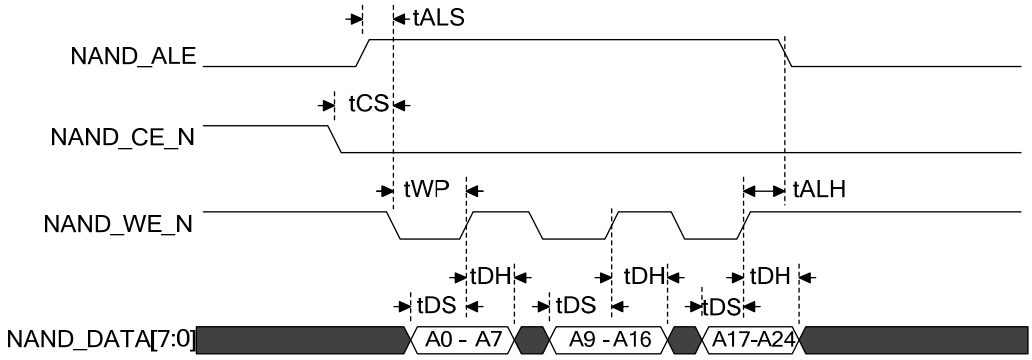

Table 2-95 describes the NANDC address cycle timing parameters.

Table 2-95 NANDC address cycle timing parameters

Parameter	Symbol	Mim	Max	Unit	Remarks
Setup time of NAND_CE_N	tCS	0	None	ns	None
Pulse width of NAND_WE_N	tWP	15	None	ns	Configurable
Setup time of NAND_ALE	tALS	0	None	ns	None
Hold time of NAND_ALE	tALH	10	None	ns	Configurable
Data setup time	tDS	10	None	ns	Configurable
Data hold time	tDH	10	None	ns	Configurable

Write Data Timing

Figure 2-17 shows the NANDC write data timing.

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Figure 2-17 NANDC write data timing

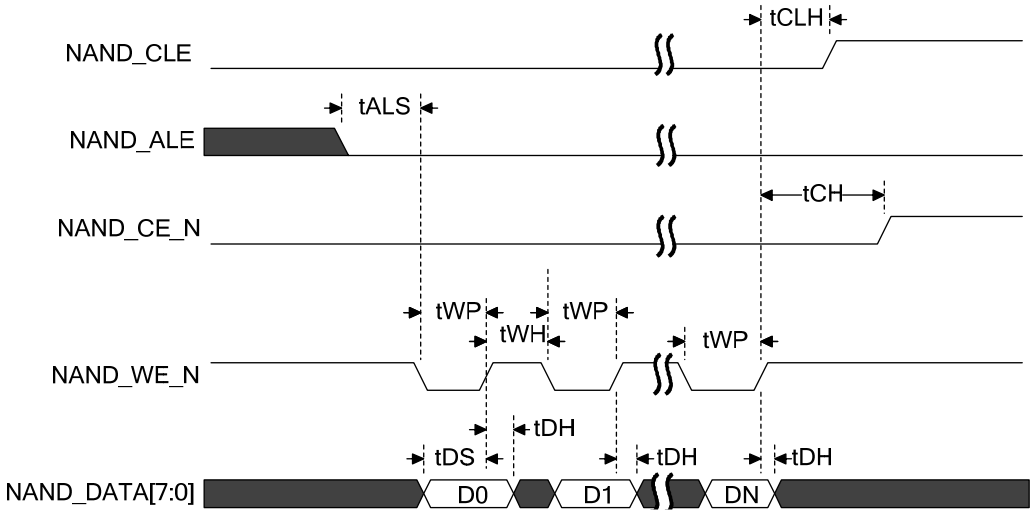

Table 2-96 describes the NANDC write data timing parameters.

Table 2-96 NANDC write data timing parameters

Parameter	Symbol	Min	Max	Unit	Remarks
Hold time of NAND_CLE	tCLH	10	None	ns	Configurable
Hold time of NAND_CE_N	tCH	10	None	ns	Configurable
Pulse width of NAND_WE_N	tWP	15	None	ns	Configurable
Setup time of NAND_ALE	tALS	0	None	ns	Configurable
Data setup time	tDS	10	None	ns	Configurable
Data hold time	tDH	10	None	ns	Configurable
High-level hold time of NAND_WE_N	tWH	15	None	ns	Configurable

Read Data Timing

Figure 2-18 shows the NANDC read data timing.

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Figure 2-18 NANDC read data timing

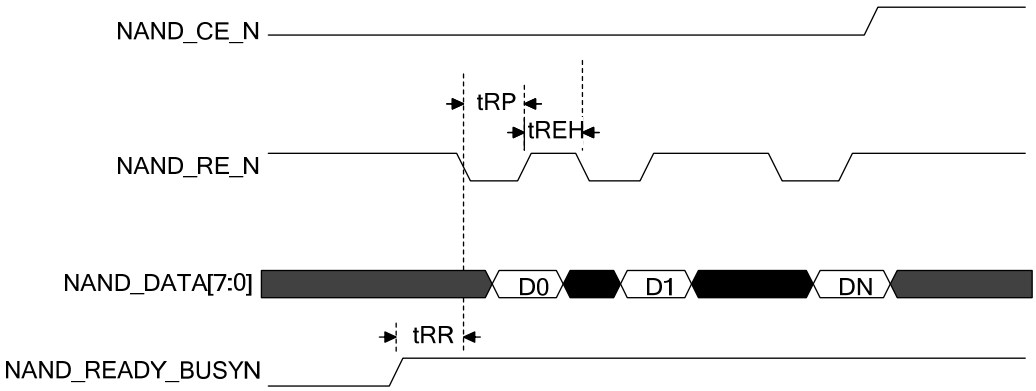

Table 2-97 describes the NANDC read data timing parameters.

Table 2-97 NANDC read data timing parameters

Parameter	Symbol	Min	Max	Unit	Remarks
Low-level wait time of NAND_RE_N	tRR	15	-	ns	Configurable
Pulse width of NAND_RE_N	tRP	15	-	ns	Configurable
High-level width of NAND_RE_N	tREH	15	-	ns	Configurable

NOTE

The tRR delay is configurable.

2.8.3 SFC Interface Timings

Figure 2-19 shows the SFC input timing.

Figure 2-19 SFC input timing

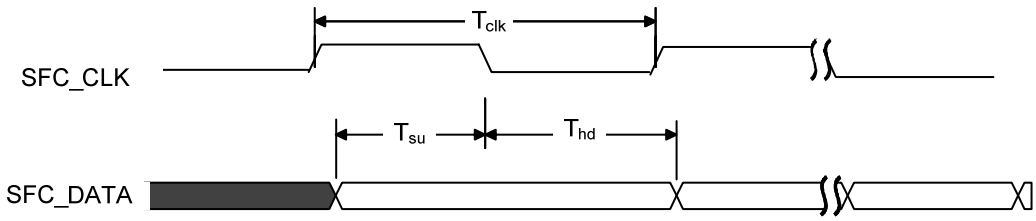

Table 2-98 describes the SFC input timing parameters.

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Table 2-98 SFC input timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFC_CLK	T_{clk}	16	None	83.2	ns
Input signal setup time	T_{su}	8	None	None	ns
Input signal hold time	T_{hd}	1.2	None	None	ns

Figure 2-20 shows the SFC output timing.

Figure 2-20 SFC output timing

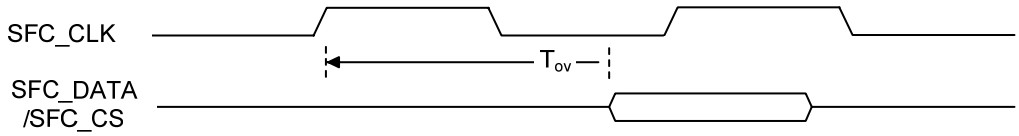

Table 2-99 describes the SFC output timing parameters.

Table 2-99 SFC output timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFCCLK	T	16	None	83.2	ns
Output data signal delay	T_{ov}	–5	None	3.0	ns
Output CS signal delay	T_{ov}	–5	None	3.0	ns

2.8.4 Ethernet MAC Port Timings

MII Timings

The Hi3521 provides standard MIIs that comply with the MII timing standard. These interfaces are used to connect to the physical layer (PHY).

Figure 2-21 shows the 100 Mbit/s receive timing of the MII.

Figure 2-21 100 Mbit/s receive timing of the MII

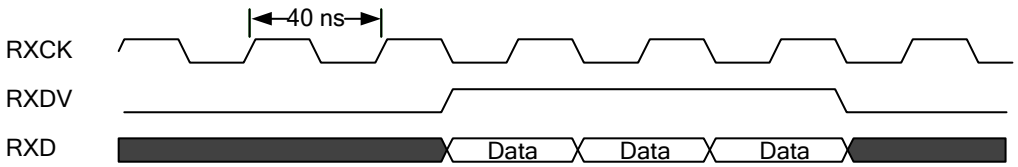

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Figure 2-22 shows the 100 Mbit/s transmit timing of the MII.

Figure 2-22 100 Mbit/s transmit timing of the MII

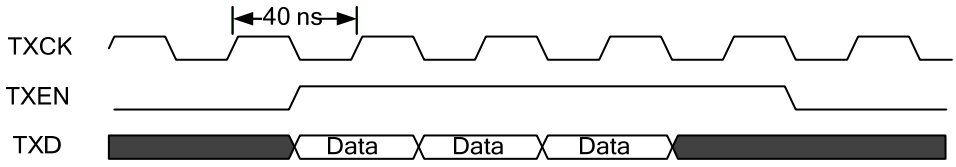

Figure 2-23 shows the 10 Mbit/s receive timing of the MII.

Figure 2-23 10 Mbit/s receive timing of the MII

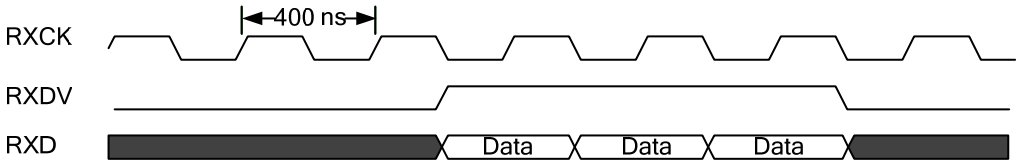

Figure 2-24 shows the 10 Mbit/s transmit timing of the MII.

Figure 2-24 10 Mbit/s transmit timing of the MII

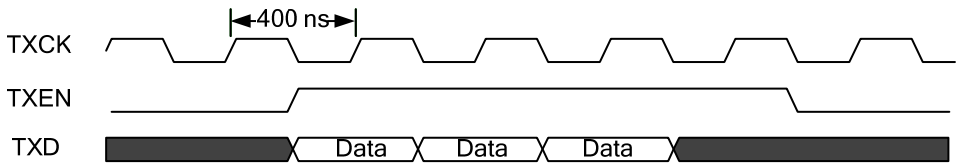

Figure 2-25 shows the receive timing parameters of the MII.

Figure 2-25 Receive timing parameters of the MII

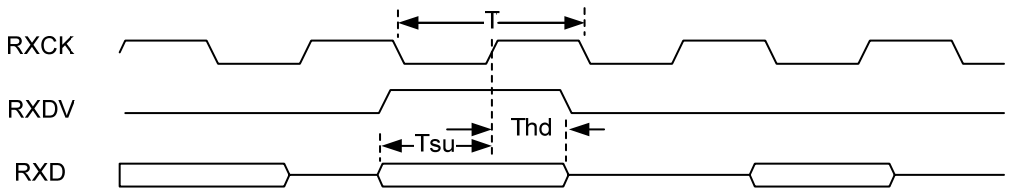

Figure 2-26 shows the transmit timing parameters of the MII.

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Figure 2-26 Transmit timing parameters of the MII

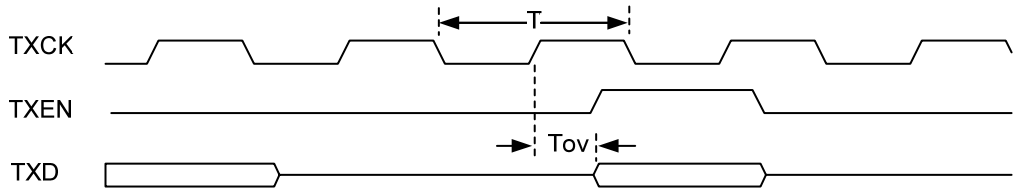

Table 2-100 describes the MII timing parameters.

Table 2-100 MII timing parameters

Parameter	Symbol	Signal	Min	Max	Unit
MII clock cycle	T	RXCK, TXCK	400(10Mbit/s)	400	ns
			40(100Mbit/s)	40	ns
MII signal setup time	Tsu (RX)	RXER, RXDV, RXD[3:0]	10	None	ns
MII signal hold time	Thd (RX)	RXER, RXDV, RXD[3:0]	10	None	ns
MII output signal delay	Tov (TX)	TXD[3:0], TXEN	0	25	ns

RGMII Timings

Figure 2-27 shows the 1000 Mbit/s receive timing of the RGMII.

Figure 2-27 1000 Mbit/s receive timing of the RGMII

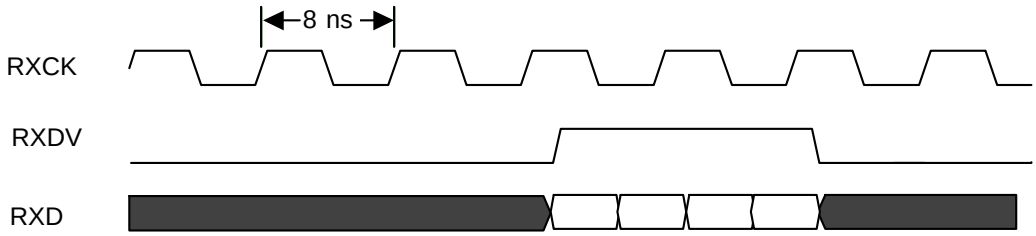

Figure 2-28 shows the 1000 Mbit/s transmit timing of the RGMII.

Figure 2-28 1000 Mbit/s transmit timing of the RGMII

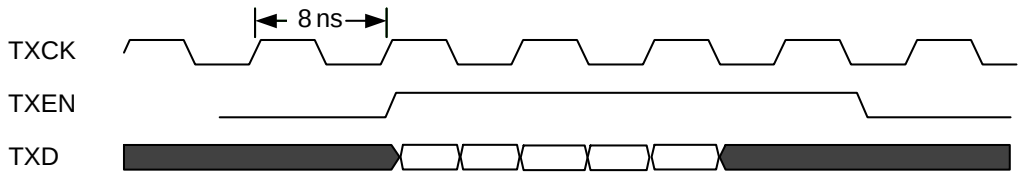

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Table 2-101 describes the RGMII timing parameters.

Table 2-101 RGMII timing parameters

Parameter	Symbol	Signal	Min	Max	Unit
RGMII clock cycle	T	RXCK, TXCK	8	8	ns
RGMII signal setup time	Tsu (RX)	RXER, RXDV, RXD[3:0]	1	None	ns
RGMII signal hold time	Thd (RX)	RXER, RXDV, RXD[3:0]	1	None	ns
RGMII output signal delay	Tov (TX)	TXD[3:0], TXEN	-0.5	0.5	ns

MDIO Interface Timings

Figure 2-29 shows the read timing of the MDIO interface.

Figure 2-29 Read timing of the MDIO interface

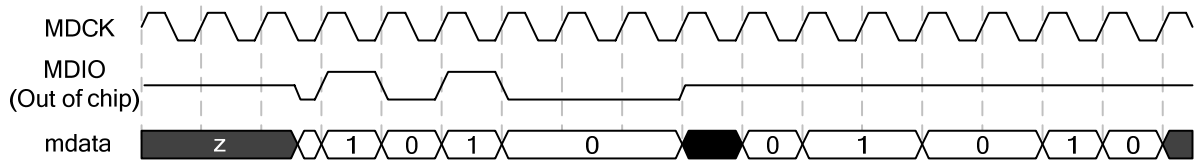

Figure 2-30 shows the write timing of the MDIO interface.

Figure 2-30 Write timing of the MDIO interface

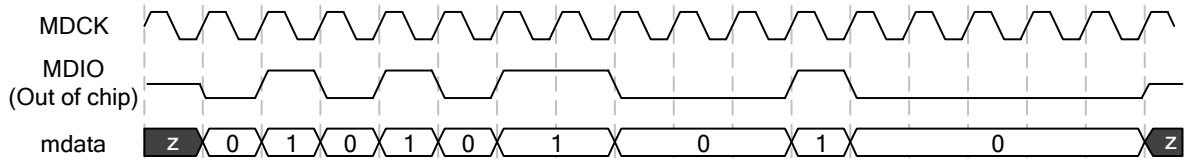

Figure 2-31 shows the receive timing parameters of the MDIO interface.

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Figure 2-31 Receive timing parameters of the MDIO interface

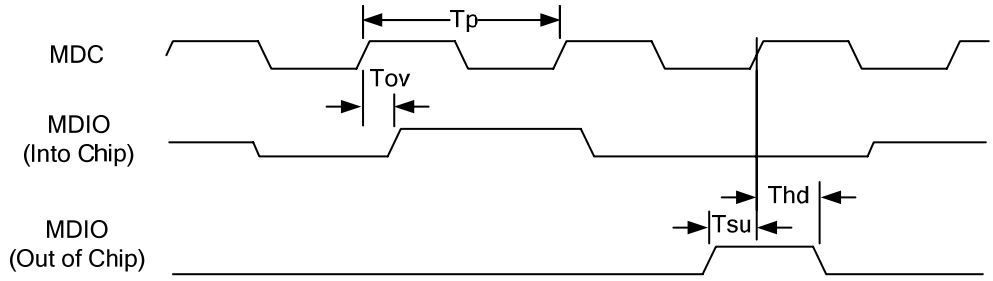

Table 2-102 describes the timing parameters of the MDIO interface.

Table 2-102 Timing parameters of the MDIO interface

Parameter	Symbol	Signal	Min	Max	Unit
MDIO data receive delay	Tov	MDIO	0	300	ns
MDIO clock cycle	Tp	MDCK	400	1240	ns
MDIO data transmit setup time	Tsu	MDIO	10	None	ns
MDIO data transmit hold time	Thd	MDIO	10	None	ns

NOTE

The MDC clock cycle Tp can be changed by adjusting the MDC frequency (MDIO_RWCTRL[frq_dv]). To be specific, you can divide the frequency of the ETH working clock by 102, 62, or other values. Tov is related to the clock cycle Tp of the MDC, and its value is about Tmdc/2.

2.8.5 VI Interface Timing

The VI clock is supplied externally. All the VI interfaces are input interfaces in slave mode.

Figure 2-32 shows the VI interface timing.

Figure 2-32 VI interface timing

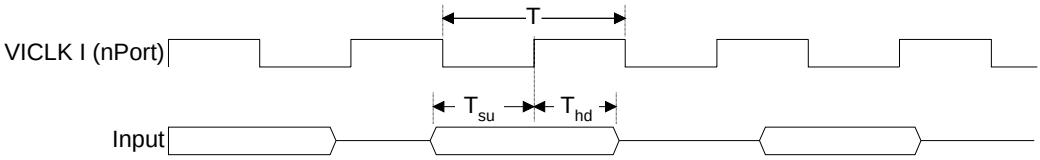

Table 2-103 describes the VI interface timing parameters.

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Table 2-103 VI interface timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
VICLK clock cycle	T	6.74	-	-	ns
Input signal setup time	T_{su}	1.5	-	-	ns
Input signal hold time	T_{hd}	1.0	-	-	ns

2.8.6 VO Interface Timing

Figure 2-33 shows the VO interface timing.

Figure 2-33 VO interface timing

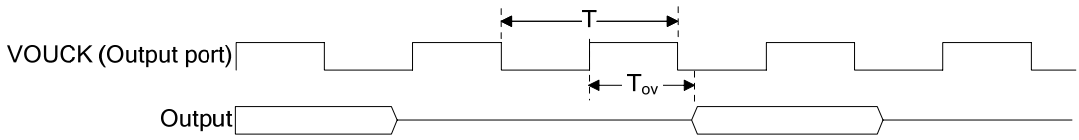

Table 2-104 describes the VO interface timing parameters.

Table 2-104 VO interface timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency 1					
VO1CLK clock cycle	T	None	37	None	ns
Output signal delay	T_{ov}	17	None	22	ns
Operating frequency 2					
VO0CLK clock cycle	T	None	6.74	None	ns
Output signal delay	T_{ov}	2.5	None	4.8	ns

2.8.7 SIO Interface Timings

I²S Interface Timings

Figure 2-34 shows the I^2S interface receive timing.

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Figure 2-34 I²S interface receive timing

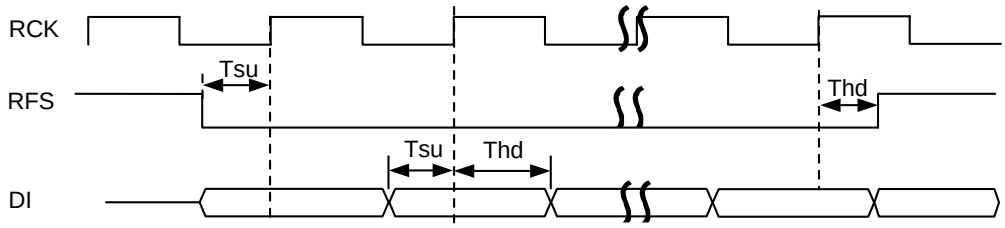

Figure 2-35 shows the I²S interface transmit timing.

Figure 2-35 I²S interface transmit timing

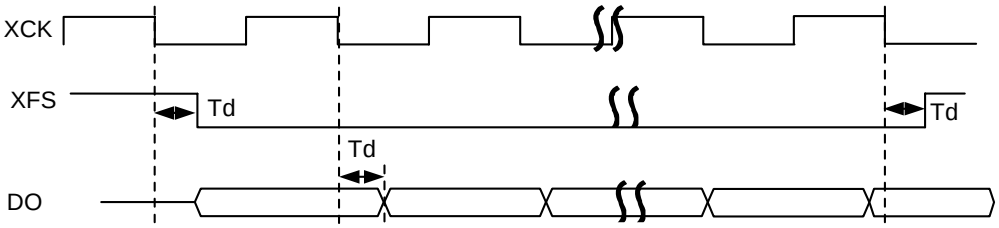

Table 2-105 describes the I²S interface timing parameters.

Table 2-105 I²S interface timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	10	None	None	ns
Input signal hold time	T_{hd}	10	None	None	ns
Output signal delay	T_d	0	None	8	ns

PCM Interface Timings

Figure 2-36 shows the PCM interface receive timing.

Figure 2-36 PCM interface receive timing

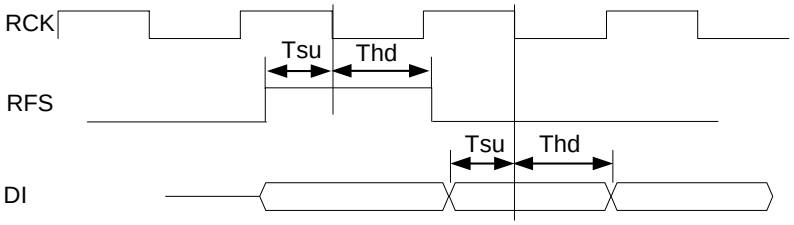

Figure 2-37 shows the PCM interface transmit timing.

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Figure 2-37 PCM interface transmit timing

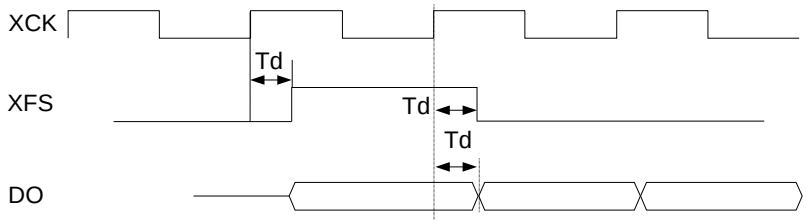

Table 2-106 describes the PCM interface timing parameters.

Table 2-106 PCM interface timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	10	None	None	ns
Input signal hold time	T_{hd}	10	None	None	ns
Output signal delay	T_d	0	None	8	ns

2.8.8 I2C Interface Timing

Figure 2-38 shows the I^2C transfer timing.

Figure 2-38 I^2C transfer timing

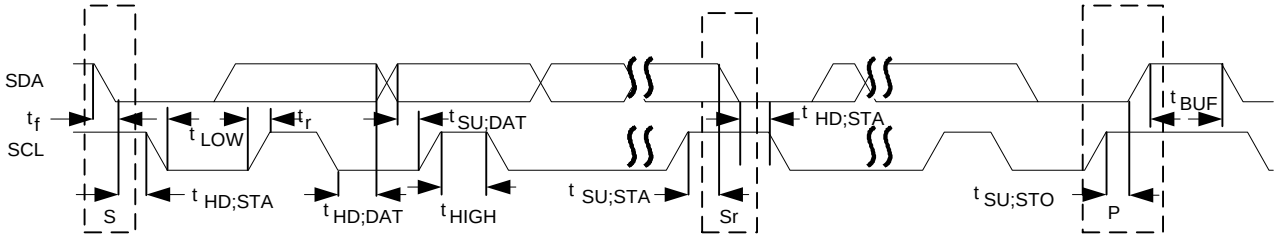

Table 2-107 describes the I^2C interface timing parameters.

Table 2-107 I^2C interface timing parameters

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
Serial clock (SCL) frequency	f_{SCL}	0	100	0	400	kHz
Start hold time	$t_{HD;STA}$	4.0	None	0.6	None	µs
SCL low-level cycle	t_{LOW}	4.7	None	1.3	None	µs

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Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL high-level cycle	t_{HIGH}	4.0	None	0.6	None	μs
Start setup time	$t_{SU;STA}$	4.7	None	0.6	None	μs
Data hold time	$t_{HD;DAT}$	0	3.45	0	0.9	μs
Data setup time	$t_{SU;DAT}$	250	None	100	None	ns
Serial data (SDA) and SCL rising time	t_r	None	1000	$20 + 0.1C_b$	300	ns
SDA and SCL falling time	t_f	None	300	$20 + 0.1C_b$	300	ns
End setup time	$t_{SU;STO}$	4.0	None	0.6	None	μs
Bus release time from start to end	t_{BUF}	4.7	None	1.3	None	μs
Bus load	C_b	None	400	None	400	pF
Low-level noise tolerance	V_{nL}	$0.1V_{DD}$	None	$0.1V_{DD}$	None	V
High-level noise tolerance	V_{nH}	$0.2V_{DD}$	None	$0.2V_{DD}$	None	V

2.8.9 SPI Timings

NOTE

In Figure Figure 2-39 to Figure 2-41, the conventions are as follows:

- MSB = most significant bit
- LSB = least significant bit
- SPI_CK(0):spo = 0
- SPI_CK(1):spo = 1

Figure 2-39 shows the SPI clock (SPICK) timing.

Figure 2-39 SPICK timing

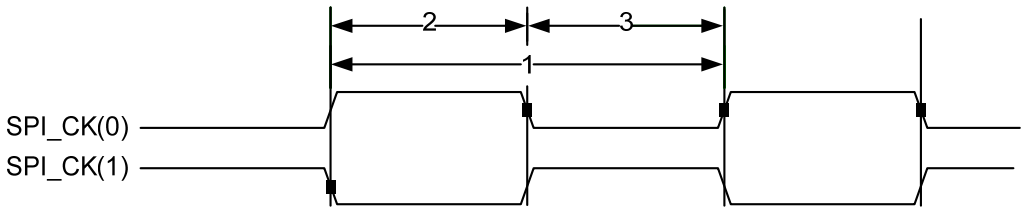

Figure 2-40 and Figure 2-41 show the SPI timings in master mode.

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Figure 2-40 SPI timing in master mode (sph = 0)

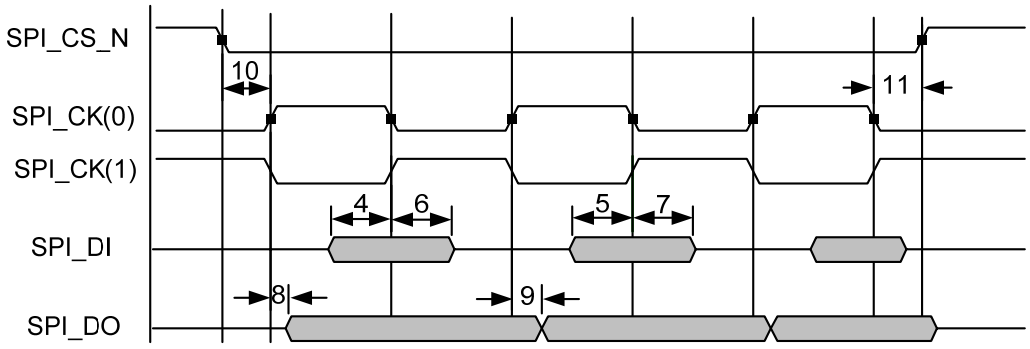

Figure 2-41 SPI timing in master mode (sph = 1)

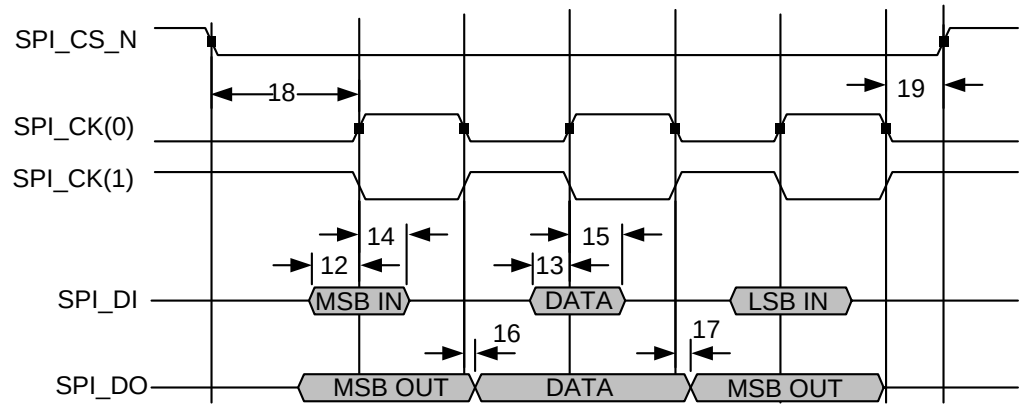

Table 2-108 describes the SPI timing parameters.

Table 2-108 SPI timing parameters

No.	Parameter	Symbol	Min	Typ	Max	Unit
1	Cycle time, SPI_CK	tc	None	None	None	ns
2	Pulse duration, SPI_CK high (all master modes)	tw1	None	None	None	ns
3	Pulse duration. SPI_CK low (all master modes)	tw2	None	None	None	ns
4	Setup time, SPI_DI (input) valid before SPI_CK (output) falling edge	tsu1	None	None	None	ns
5	Setup time, SPI_DI (in put) valid before SPICK (output) rising edge	tsu2	None	None	None	ns
6	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th1	None	None	None	ns

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No.	Parameter	Symbol	Min	Typ	Max	Unit
7	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th2	None	None	None	ns
8	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td1	None	None	None	ns
9	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td2	None	None	None	ns
10	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td3	None	None	None	ns
11	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td4	None	None	None	ns
12	Setup time, SPI_DI (input) valid before SPI_CK (output) rising edge	tsu3	None	None	None	ns
13	Setup time, SPI_DI (in put) valid before SPI_CK (output) falling edge	tsu4	None	None	None	ns
14	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th3	None	None	None	ns
15	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th4	None	None	None	ns
16	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td5	None	None	None	ns
17	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td6	None	None	None	ns
18	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td7	None	None	None	ns
19	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td8	None	None	None	ns

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Contents

3 System 3-1
3.1 Reset 3-1
3.1.1 Overview 3-1
3.1.2 Reset Control 3-1
3.1.3 Reset Configuration 3-2
3.2 Clock 3-3
3.2.1 Overview 3-3
3.2.2 Clock Control Block Diagram 3-3
3.2.3 Clock Configuration 3-4
3.2.4 Register Summary 3-21
3.2.5 Register Description 3-23
3.3 Interrupt System 3-70
3.4 System Controller 3-72
3.4.1 Overview 3-72
3.4.2 Features 3-72
3.4.3 Function Description 3-72
3.4.4 Register Summary 3-76
3.4.5 Register Description 3-77
3.5 DMA Controller 3-120
3.5.1 Overview 3-120
3.5.2 Features 3-120
3.5.3 Function Description 3-121
3.5.4 Operating Mode 3-125
3.5.5 Register Summary 3-130
3.5.6 Register Description 3-131
3.6 CIPHER 3-145
3.6.1 Overview 3-145
3.6.2 Features 3-145
3.6.3 Function Description 3-146
3.6.4 Operating Mode 3-156
3.6.5 Register Summary 3-158
3.6.6 Register Description 3-160

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3.7 Timer 3-178
3.7.1 Overview 3-178
3.7.2 Features 3-178
3.7.3 Function Description 3-179
3.7.4 Operating Mode 3-179
3.7.5 Register Summary 3-180
3.7.6 Register Description 3-181
3.8 Watchdog 3-186
3.8.1 Overview 3-186
3.8.2 Features 3-186
3.8.3 Function Description 3-186
3.8.4 Operating Mode 3-187
3.8.5 WatchDogRegister Summary 3-188
3.8.6 Register Description 3-189
3.9 RTC 3-192
3.9.1 Overview 3-192
3.9.2 Features 3-192
3.9.3 Function Description 3-192
3.9.4 Operating Mode 3-193
3.9.5 Register Summary 3-194
3.9.6 Register Description 3-194
3.10 Power Management and Low-Power Mode Control 3-198
3.10.1 Overview 3-198
3.10.2 Operating Modes of the System 3-199
3.10.3 Clock Gating and Clock Frequency Adjustment 3-199
3.10.4 Module Low-Power Control 3-200
3.10.5 DDR Low-Power Control 3-201
3.11 Processor Subsystem 3-201
3.11.1 ARM Cortex-A9 Processor 3-201
3.11.2 L2 Cache 3-202

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Figures

Figure 3-1 Diagram of controlling reset signals 3-1
Figure 3-2 Functional block diagram of the clock management module 3-3
Figure 3-3 Process of switching the system mode 3-74
Figure 3-4 Bit allocation of chip ID registers 3-76
Figure 3-5 Functional block diagram of the DMAC 3-121
Figure 3-6 Updating channel registers by using the LLIs 3-123
Figure 3-7 Structure of DMAC LLIs 3-125
Figure 3-8 3DES encryption of a 3-key operation and a 2-key operation 3-146
Figure 3-9 3DES decryption of a 3-key operation and a 2-key operation 3-147
Figure 3-10 ECB mode of the AES and DES algorithms 3-147
Figure 3-11 ECB mode of the 3DES algorithm 3-148
Figure 3-12 CBC mode of the AES and DES algorithms 3-149
Figure 3-13 CBC mode of the 3DES algorithm 3-150
Figure 3-14 S-bit CFB mode of the AES and DES algorithms 3-151
Figure 3-15 S-bit CFB mode of the 3DES algorithm 3-152
Figure 3-16 OFB mode of the AES algorithm 3-153
Figure 3-17 S-bit OFB mode of the DES algorithm 3-154
Figure 3-18 S-bit OFB mode of the 3DES algorithm 3-155
Figure 3-19 CTR mode of the AES algorithm 3-156
Figure 3-20 Structure of the linked list header of a multi-block encryption/decryption channel 3-157
Figure 3-21 Bits of cas 3-158
Figure 3-22 Application block diagram of the watchdog 3-186

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Tables

Table 3-1 Types of reset signals 3-2
Table 3-2 Configuration registers corresponding to Hi3521 PLLs 3-4
Table 3-3 Mapping between PLLs and functional modules 3-5
Table 3-4 Methods of calculating PLL output frequencies 3-5
Table 3-5 Frequency configurations of A9 clocks 3-6
Table 3-6 Mapping between the status of the system controller and clocks 3-7
Table 3-7 Frequency configurations of VICAP clocks 3-7
Table 3-8 Frequency configurations of VDP clocks 3-9
Table 3-9 Frequency configurations of HDMI clocks 3-10
Table 3-10 Frequency configurations of GMAC clocks 3-10
Table 3-11 Frequency configurations of VEDU clocks 3-11
Table 3-12 Frequency configurations of VPSS clocks 3-11
Table 3-13 Frequency configurations of VDH clocks 3-12
Table 3-14 Frequency configurations of TDE clocks 3-13
Table 3-15 Frequency configurations of JPGE clocks 3-13
Table 3-16 Frequency configurations of JPGD clocks 3-14
Table 3-17 Frequency configurations of MDU clocks 3-14
Table 3-18 Frequency configurations of VAPU clocks 3-15
Table 3-19 Frequency configuration of the SATA clock 3-15
Table 3-20 Frequency configuration of the TOE clock 3-16
Table 3-21 Frequency configurations of SDIO clocks 3-16
Table 3-22 Frequency configuration of the SFC clock 3-16
Table 3-23 Frequency configuration of NFC clock 3-17
Table 3-24 Frequency configurations of SIO0, SIO1, SIO2, and SIO3 clocks 3-17
Table 3-25 Summary of CRG registers (base address: 0x2003_0000) 3-21
Table 3-26 A9 interrupt sources of A9 3-70

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Table 3-27 Summary of the system controller registers (base address: 0x2005_0000) 3-76
Table 3-28 DMAC hardware request signals and corresponding peripheral requests 3-123
Table 3-29 Mapping between the value of DBSize or SBSize and burst length 3-127
Table 3-30 Mapping between the value of DWidth or SWidth and transfer bit width 3-127
Table 3-31 Definitions of the prot field of DMAC_Cn_CONTROL 3-128
Table 3-32 Flow controllers and transfer types corresponding to the flow_cntrl field 3-129
Table 3-33 Summary of the DMAC registers (base address: 0x100D_0000) 3-130
Table 3-34 Summary of CIPHER registers (base address: 0x100C_0000) 3-158
Table 3-35 Variable in the offset addresses of CIPHER registers 3-160
Table 3-36 Summary of timer registers 3-181
Table 3-37 Summary of watchdog registers (base address: 0x2004_0000) 3-188
Table 3-38 Summary of RTC registers (base address: 0x2006_0000) 3-194
Table 3-39 Ratio of the frequency of the CPU to the frequency of the AXI bus 3-202

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3 System

3.1 Reset

3.1.1 Overview

The reset management module resets the entire chip and all functional modules in a unified manner as follows:

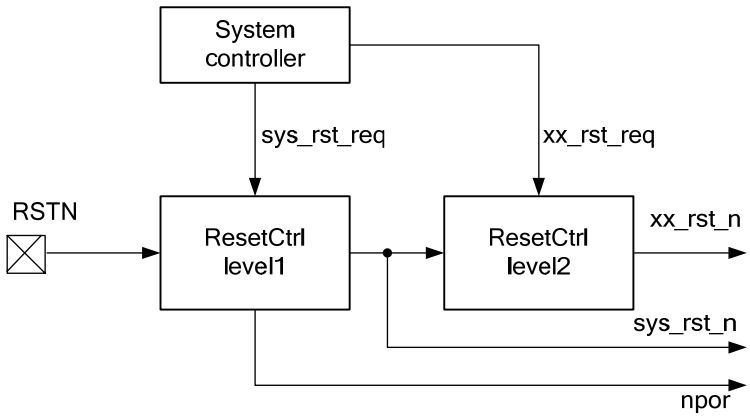
- Manages and controls power-on reset.
- Controls the system soft reset and the separate soft reset of each functional module.
- Synchronizes reset signals to the clock domain corresponding to each module.

The reset management module also generates reset signals for each internal functional module.

3.1.2 Reset Control

Figure 3-1 shows the diagram of controlling reset signals.

Figure 3-1 Diagram of controlling reset signals



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NOTE

- RSTN: power-on reset signal. This signal is derived from the input pin RSTN of the chip.
- sys_rst_req: global soft reset request signal. This signal is derived from the system controller.
- xx_rst_req: separate soft reset request signal of each submodule. This signal is derived from the clock and reset generator (CRG) system controller.
- xx_rst_n, sys_rst_n, and npor: reset signals.

Table 3-1 Types of reset signals

Type	Generation Mode	Function
Global hard reset signal (npor)	Derived from the RSTN reset pin.	Globally resets the entire Hi3521.
Global soft reset signal (syn_rst_n)	Derived from the global soft reset register of the software configuration system controller.	Globally resets all the modules of the Hi3521 excluding the clock reset circuit and the test circuit.
Submodule reset signal (xx_rst_n)	Derived from the submodule reset control register of the CRG system controller.	Separately resets each submodule of the Hi3521.

3.1.3 Reset Configuration

Power-On Reset

The RSTN is the functional reset input/output (IO) pin of the Hi3521. To implement power-on reset, the following conditions must be met:

- The power-on reset IO pin inputs a low-level pulse.
- The clock input by the XIN pin of the crystal oscillator clock works properly.
- The low pulse width of the power-on reset signal is longer than 12 XIN clock cycles.

System Reset

The system is reset in either of the following ways:

- Power-on reset
- Global soft reset, controlled by the system controller

Soft Reset

The soft reset is controlled by configuring the corresponding system controller. For details about configurations, see the description of the reset register for each module.

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CAUTION

- After a system soft reset request is sent, the circuit reset is deasserted after at least 360 system clock cycles.
- The separate soft reset of each module is not automatically deasserted. For example, if a module is reset after 1 is written to the related bit, the reset of this module is deasserted only when the related bit is set to 0.

3.2 Clock

3.2.1 Overview

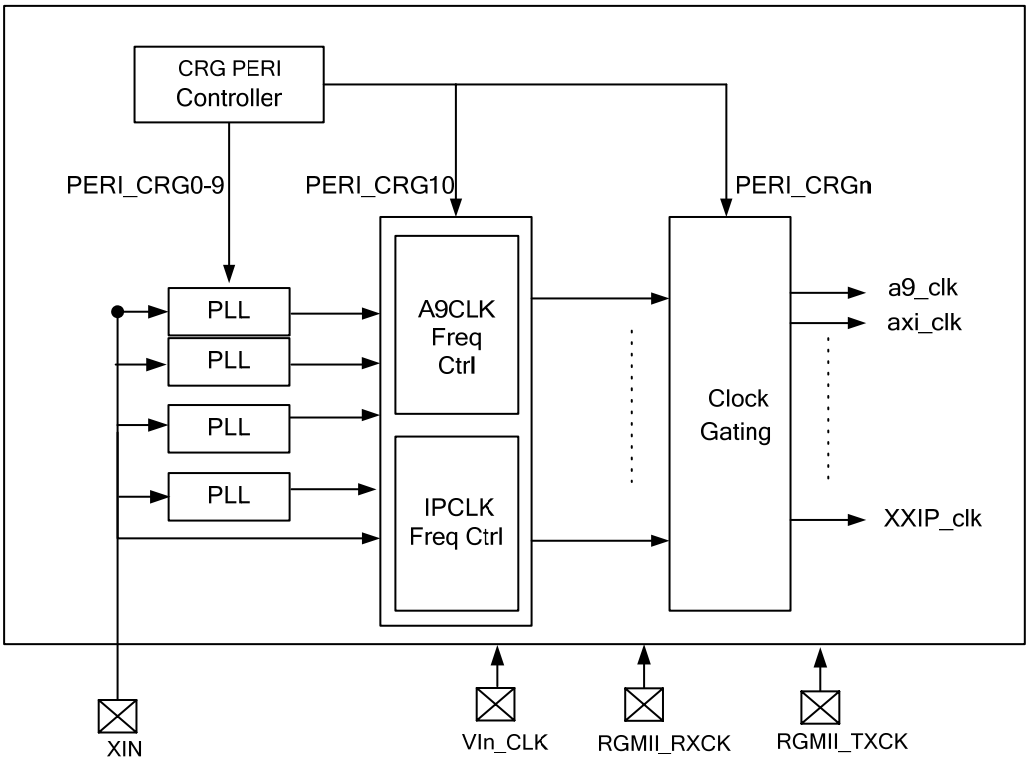
The clock management module manages clock input, clock generation, and clock control in a unified manner as follows:

- Manages and controls clock inputs
- Divides and controls clock frequencies
- Generates working clocks for each module

3.2.2 Clock Control Block Diagram

Figure 3-2 shows the functional block diagram of the clock management module.

Figure 3-2 Functional block diagram of the clock management module



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NOTE

The value of *n* in VInCK ranges from 0 to 3.

The inputs of the clock management module are as follows:

- Clock inputs from the XIN, VIn_CLK, RGMII_RXCK, and RGMII_TXCK pins.
  - XIN is the phase-locked loop (PLL) input clock that connects only to the 24 MHz crystal.
  - VIn_CLK is a video input (VI) clock.
  - RGMII_RXCK and RGMII_TXCK are the interface clocks of the gigabit media access control (GMAC) module.
- Clock control registers derived from the CRG system controller.
  - PLL frequency configuration
  - IP clock frequency configuration
  - Clock gating configuration

The clock management module consists of the following parts:

- PLL unit. This unit is used to generate A9 clock, bus clock, and the clocks required by peripherals.
- Control units including the A9 frequency control unit (A9 Freq Ctrl) and module clock frequency control unit (IPCLK Freq Ctrl)
- Clock gating management unit

3.2.3 Clock Configuration

PLL Configuration

The Hi3521 has four internal PLLs. Each PLL uses two configuration registers. See Table 3-2.

Table 3-2 Configuration registers corresponding to Hi3521 PLLs

PLL	Configuration Register 1	Configuration Register 0
APLL	PERI_CRG0	PERI_CRG1
VPLL0	PERI_CRG2	PERI_CRG3
VPLL2	PERI_CRG6	PERI_CRG7
EPLL	PERI_CRG8	PERI_CRG9

Table 3-3 shows the mapping between PLLs and functional modules.

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Table 3-3 Mapping between PLLs and functional modules

PLL	Output Pin of Each PLL	Function
APLL	FOUTPOSTDIV	• Generates the CPU working clock. • Generates the DDR working clock. • Generates the advanced eXtensible interface (AXI) bus clock by dividing the DDR clock by 2. • Generates the advanced peripheral bus (APB) clock by dividing the DDR clock by 4.
VPLL0	FOUTPOSTDIV	The default clock is a 268.5 MHz clock. It acts as one of the source clocks of the VDP HD or HDMI module.
VPLL2	FOUT2	The default clock is a 405 MHz clock. It acts as the working clock of the working clock of the VEDU, VPSS, or TDE.
	FOUT3	The default clock is a 270 MHz clock. It is divided by 5 to generate a clock to act as the working clock of the VDP SD module.
	FOUT4	The default clock is a 202.5 MHz clock. It acts as the working clock of the CIPHER module.
EPLL	FOUTVCO	The default clock is a 1500 MHz clock. It is divided by 5 to generate a 300 MHz clock to act as the working clock of the MDU, JPGE, JPGD, or IVE.
	FOUTPOSTDIV	• The default clock is a 500 MHz clock. It acts as the source clock of the SIO module. • The 500 MHz clock is divided by 5 to generate a 100 MHz clock to act as the working clock or source clock of the NFC, SDIO, SFC, or TOE module.
	FOUT1	The default clock is a 250 MHz clock. It acts as the working clock of the VDH or JPGD.
	FOUT2	The default clock is a 125 MHz clock. It acts as the reference interface clock or reference clock of the GMAC, SATA, or SFC module.

All PLLs use the input crystal oscillator clock of the XIN pin as the input clock. For details on how to calculate PLL output frequencies, see Table 3-4.

Table 3-4 Methods of calculating PLL output frequencies

PLL Pin	Formula	Remarks
FREF	PLL input reference clock	The input clock must be 24 MHz.

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PLL Pin	Formula	Remarks
FOUTVCO	FREF x (fbdiv + frac/2^24)/refdiv	PLL working frequency. It must be greater than 800 MHz but less than or equal to 2.4 GHz.
FOUTPOSTDIV	FOUTVCO/(pstdiv1 x pstdiv2)	None
FOUT1ph0	FOUTVCO/(pstdiv1 x pstdiv2 x 2)	None
FOUT2	FOUTVCO/(pstdiv1 x pstdiv2 x 4)	None
FOUT3	FOUTVCO/(pstdiv1 x pstdiv2 x 6)	None
FOUT4	FOUTVCO/(pstdiv1 x pstdiv2 x 8)	None

The following is an example using VPLL0. VPLL0 outputs the FOUTPOSTDIV to the video output unit (VOU), and the working clock required by the VOU is 268.5 MHz.

If postdiv2 is 4 and postdiv1 is 1, the value of FOUTVCO is 1074 MHz.

If refdiv is 4, the value of FOUTVCO is calculated as follows: 24 x (fbdiv + frac/2^24)/2 = 1074 MHz.

Based on the preceding results, fbdiv is 179 and frac is 000000.

Frequency Configurations of A9 clocks

Table 3-5 describes the frequency configurations of A9/AXI clocks.

Table 3-5 Frequency configurations of A9 clocks

Signal	Description
freqmode_a9_sys	Frequency reduction configuration of the A9 clock. By masking the A9 clock pulse, the A9 frequency can be reduced and the ration of the A9 frequency to the AXI frequency can be adjusted. 00: A9:AXI = 3:1 01: A9:AXI = 3:1 10: A9:AXI = 2:1 11: A9:AXI = 1:1 This signal can be controlled by configuring PERI_CRG10 bits[3:2].

Table 3-6 shows the mapping between the status of the system controller and clocks.

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Table 3-6 Mapping between the status of the system controller and clocks

Status of the System Controller	Enable Status of the 46.875 kHz Clock	Enable Status of the 24 MHz Crystal Oscillator	Enable Status of the APLL	Status of the System Clock
Normal	Enabled	Enabled	Enabled	The working clocks of the ARM subsystem are derived from the PLL.
Slow	Enabled	Enabled	Disabled	The working clocks of the ARM subsystem are derived from the 24 MHz crystal oscillator.
Doze	Enabled	Enabled	Disabled	The working clocks of the ARM subsystem are derived from the 46.875 kHz clock. The 46.875 kHz clock is generated by dividing the 24 MHz crystal oscillator.

Frequency Configurations of Module Clocks

Table 3-7 describes the frequency configurations of video capture (VICAP) clocks.

The VICAP module supports four ports and 16 channels. Each port corresponds to four channels.

Table 3-7 Frequency configurations of VICAP clocks

Signal	Description
vi0div_sel	VI0 div ch clock select. VI0 div ch is output to channel 0, channel 1, channel 2, and channel 3. 00: div2 (divide the clock by 2) 01: div4 (divide the clock by 4) 10: div1 (no frequency division) 11: reserved This signal can be controlled by configuring PERI_CRG12 bit[19:18].

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Signal	Description
vi1div_sel	VI1 div ch clock select. VI1 div ch is output to channel 4, channel 5, channel 6, and channel 7. 00: div2 (divide the clock by 2) 01: div4 (divide the clock by 4) 10: div1 (no frequency division) 11: reserved This signal can be controlled by configuring PERI_CRG12 bit[17:16].
vi2div_sel	VI2 div ch clock select. VI2 div ch is output to channel 8, channel 9, channel 10, and channel 11. 00: div2 (divide the clock by 2) 01: div4 (divide the clock by 4) 10: div1 (no frequency division) 11: reserved This signal can be controlled by configuring PERI_CRG12 bit[15:14].
vi3div_sel	VI3 div ch clock select. VI3 div ch is output to channel 12, channel 13, channel 14, and channel 15. 00: div2 (divide the clock by 2) 01: div4 (divide the clock by 4) 10: div1 (no frequency division) 11: reserved This signal can be controlled by configuring PERI_CRG12 bit[13:12].
vi0_sc_sel	VI0 ch clock source select. 00: VI0 pad input clock 01: VI1 pad input clock 10: VI2 pad input clock 11: VI3 pad input clock This signal can be controlled by configuring PERI_CRG12 bit[25:24].
vi1_sc_sel	VI1 ch clock source select. 00: VI0 pad input clock 01: VI1 pad input clock 10: VI2 pad input clock 11: VI3 pad input clock This signal can be controlled by configuring PERI_CRG12 bit[27:26].

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Signal	Description
vi2_sc_sel	VI2 ch clock source select. 00: VI0 pad input clock 01: VI1 pad input clock 10: VI2 pad input clock 11: VI3 pad input clock This signal can be controlled by configuring PERI_CRG12 bit[29:28].
vi3_sc_sel	VI3 ch clock source select. 00: VI0 pad input clock 01: VI1 pad input clock 10: VI2 pad input clock 11: VI3 pad input clock This signal can be controlled by configuring PERI_CRG12 bit[31:30].
vi_selftest	Clock source select for all VI ch self tests. This signal can be controlled by configuring PERI_CRG12 bit[22].
vi*n*_pctrl	VIn input associated clock phase control. The value range of n is 0–3. The normal phase clock is selected by default. 0: normal phase clock 1: reverse phase clock This signal can be controlled by configuring PERI_CRG11 bit[15:12].

Table 3-8 describes the frequency configurations of VDP clocks.

Table 3-8 Frequency configurations of VDP clocks

Signal	Description
vohd_out_cksel	VO HD output associated clock source select. 0: HD1120 clock/LCD clock 1: SD656 clock This signal can be controlled by configuring PERI_CRG13 bit[12].
vosd_out_pctrl	VOU SD output associated clock phase control. 0: normal phase clock 1: reverse phase clock This signal can be controlled by configuring PERI_CRG13 bit[5].

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Signal	Description
vohd_out_pctrl	VOU HD output associated clock phase control. 0: normal phase clock 1: reverse phase clock This signal can be controlled by configuring PERI_CRG13 bit[4].

Table 3-9 describes the frequency configurations of HDMI clocks.

Table 3-9 Frequency configurations of HDMI clocks

Signal	Description
hdmi_test_sel	HDMI test clock select. 0: asclk clock 1: cec_clk clock This signal can be controlled by configuring PERI_CRG15 bit[7].
hdmi_cec_clk_sel	HDMI CEC CLK clock select. 0: XTAL div12 clock 1: 2.04 MHz clock generated by dividing the PLL clock This signal can be controlled by configuring PERI_CRG15 bit[6].
hdmi_asclk_sel	HDMI ASCLK clock select. 0: HDMI PHY clock 1: PLL clock This signal can be controlled by configuring PERI_CRG15 bit[5].
hdmi_osclk_sel	HDMI OSCLK clock select. 0: HDMI PHY clock 1: PLL clock This signal can be controlled by configuring PERI_CRG15 bit[4].

Table 3-10 describes the frequency configurations of GMAC clocks.

Table 3-10 Frequency configurations of GMAC clocks

Signal	Description
macif_mac_speed	MACIF0 10 Mbps or 100 Mbps mode select. 0: 10 Mbps 1: 100 Mbps This signal can be controlled by configuring PERI_CRG59 bit[1].

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Signal	Description
macif_port_select	MACIF gigabit mode select. 0: 1000 Mbps 1: 10/100 Mbps This signal can be controlled by configuring PERI_CRG59 bit[0].

Table 3-11 describes the frequency configurations of VEDU clocks.

Table 3-11 Frequency configurations of VEDU clocks

Signal	Description
veduclk_loaden	VEDU clock frequency division configuration enable. To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to veduclk_loaden. 3 Write 1 to veduclk_loaden. This signal can be controlled by configuring PERI_CRG16 bit[9].
veduclk_skipcfg	VEDU clock frequency division configuration. N: N-beat clocks are disabled every 32-beat VEDU clocks.This signal can be controlled by configuring PERI_CRG16 bit[8:4]. The source working clock of VEDU is 405 MHz. If veduclk_skipcfg is set to 00, VEDU works in full-speed mode; if veduclk_skipcfg is set to 01, VEDU works in speed-down mode. The actual frequency is calculated as follows: 405 x 31/32 = 392 MHz This rule applies to ther configurations.

Table 3-12 describes the frequency configurations of VPSS clocks.

Table 3-12 Frequency configurations of VPSS clocks

Signal	Description
vpssclk_loaden	VPSS clock frequency division configuration enable. To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to vpssclk_loaden. 3 Write 1 to vpssclk_loaden. This signal can be controlled by configuring PERI_CRG18 bit[9].

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Signal	Description
vpssclk_skipcfg	VPSS clock frequency division configuration. N: N-beat clocks are disabled every 32-beat VPSS clocks. This signal can be controlled by configuring PERI_CRG18 bit[8:4]. The source working clock of VPSS is 405 MHz. If vpssclk_skipcfg is set to 00, VPSS works in full-speed mode; if vpssclk_skipcfg is set to 01, VPSS works in speed-down mode. The actual frequency is calculated as follows: 405 x 31/32 = 392 MHz This rule applies to ther configurations.

Table 3-13 describes the frequency configurations of VDH clocks.

Table 3-13 Frequency configurations of VDH clocks

Signal	Description
vdhclk_loaden	VDH clock frequency division configuration enable. To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to vdhclk_loaden. 3 Write 1 to vdhclk_loaden. This signal can be controlled by configuring PERI_CRG20 bit[9].
vdhclk_skipcfg	VDH clock frequency division configuration. N: N-beat clocks are disabled every 32-beat VDH clocks. This signal can be controlled by configuring PERI_CRG18 bit[8:4]. The source working clock of VDH is 250 MHz. If vdhclk_skipcfg is set to 00, VDH works in full-speed mode; if vdhclk_skipcfg is set to 01, VDH works in speed-down mode. The actual frequency is calculated as follows: 250 x 31/32 = 242 MHz This rule applies to ther configurations.

Table 3-14 describes the frequency configurations of TDE clocks.

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Table 3-14 Frequency configurations of TDE clocks

Signal	Description
tdeclk_loaden	TDE clock frequency division configuration enable. To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to tdeclk_loaden. 3 Write 1 to tdeclk_loaden. This signal can be controlled by configuring PERI_CRG22 bit[9].
tdeclk_skipcfg	TDE clock frequency division configuration. N: N-beat clocks are disabled every 32-beat TDE clocks. This signal can be controlled by configuring PERI_CRG22 bit[8:4]. The source working clock of the TDE is 405 MHz. If tdeclk_skipcfg is set to 00, the TDE works in full-speed mode; if tdeclk_skipcfg is set to 01, the TDE works in speed-down mode. The actual frequency is calculated as follows: 405 x 31/32 = 392 MHz This rule applies to ther configurations.

Table 3-15 describes the frequency configurations of JPGE clocks.

Table 3-15 Frequency configurations of JPGE clocks

Signal	Description
jpgeclk_loaden	JPGE clock frequency division configuration enable. To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to jpgeclk_loaden. 3 Write 1 to jpgeclk_loaden. This signal can be controlled by configuring PERI_CRG24 bit[9].
jpgeclk_skipcfg	JPGE clock frequency division configuration. N: N-beat clocks are disabled every 32-beat JPGE clocks. This signal can be controlled by configuring PERI_CRG24 bit[8:4]. The source working clock of the JPGE is 300 MHz. If jpgeclk_skipcfg is set to 00, the JPGE works in full-speed mode; if jpgeclk_skipcfg is set to 01, the JPGE works in speed-down mode. The actual frequency is calculated as follows: 300 x 31/32 = 290 MHz This rule applies to ther configurations.

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Table 3-16 describes the frequency configurations of JPGD clocks.

Table 3-16 Frequency configurations of JPGD clocks

Signal	Description
jpgd_cksel	JPGD clock source select. 0: 300 MHz clock 1: 250 MHz clock This signal can be controlled by configuring PERI_CRG25 bit[10].
jpgdclk_loaden	JPGD clock frequency division configuration enable. To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to jpgdclk_loaden. 3 Write 1 to jpgdclk_loaden. This signal can be controlled by configuring PERI_CRG25 bit[9].
jpgdclk_skipcfg	JPGD clock frequency division configuration. N: N-beat clocks are disabled every 32-beat JPGE clocks. This signal can be controlled by configuring PERI_CRG25 bit[8:4]. The source working clock of the JPGD is 300 MHz. If jpgdclk_skipcfg is set to 00, the JPGD works in full-speed mode; if jpgdclk_skipcfg is set to 01, the JPGD works in speed-down mode. The actual frequency is calculated as follows: 300 x 31/32 = 290 MHz This rule applies to ther configurations.

Table 3-17 describes the frequency configuration of the MDU clocks.

Table 3-17 Frequency configurations of MDU clocks

Signal	Description
mduclk_loaden	MDU clock frequency division configuration enable. To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to mduclk_loaden. 3 Write 1 to mduclk_loaden. This signal can be controlled by configuring PERI_CRG26 bit[9].

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Signal	Description
mduclk_skipcfg	MDU clock frequency division configuration. N: N-beat clocks are disabled every 32-beat MDU clocks. This signal can be controlled by configuring PERI_CRG26 bit[8:4]. The source working clock of the MDU is 300 MHz. If mduclk_skipcfg is set to 00, the MDU works in full-speed mode; if mduclk_skipcfg is set to 01, the MDU works in speed-down mode. The actual frequency is calculated as follows: 300 x 31/32 = 290 MHz This rule applies to ther configurations.

Table 3-18 describes the frequency configurations of VAPU clocks.

Table 3-18 Frequency configurations of VAPU clocks

Signal	Description
vapuclk_loaden	VAPU clock frequency division configuration enable. To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to vapuclk_loaden. 3 Write 1 to vapuclk_loaden. This signal can be controlled by configuring PERI_CRG27 bit[9].
vapuclk_skipcfg	VAPU clock frequency division configuration. N: N-beat clocks are disabled every 32-beat VAPU clocks. This signal can be controlled by configuring PERI_CRG27 bit[8:4]. The source working clock of the VAPU is 300 MHz. If vapuclk_skipcfg is set to 00, the VAPU works in full-speed mode; if vapuclk_skipcfg is set to 01, the VAPU works in speed-down mode. The actual frequency is calculated as follows: 300 x 31/32 = 290 MHz This rule applies to ther configurations.

Table 3-19 describes the frequency configuration of the SATA clock.

Table 3-19 Frequency configuration of the SATA clock

Signal	Description
sata_clk_sel	SATA PHY reference clock select. 0: 125 MHz clock 1: 100 MHz clock This signal can be controlled by configuring PERI_CRG45 bit[11].

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Table 3-20 describes the frequency configuration of the TOE clock.

Table 3-20 Frequency configuration of the TOE clock

Signal	Description
toe_cksel	TOE working clock select. 0: APB clock 1: 100 MHz clock This signal can be controlled by configuring PERI_CRG51 bit[4].

Table 3-21 describes the frequency configurations of SDIO clocks.

Table 3-21 Frequency configurations of SDIO clocks

Signal	Description
sdioclk_pctrl	Polarity of the SDIO SAP clock. 0: normal phase 1: reverse phase This signal can be controlled by configuring PERI_CRG49 bit[3].
sdioclk_sel	SDIO working clock select. 0: 24 MHz 1: 50 MHz This signal can be controlled by configuring PERI_CRG49 bit[2].

Table 3-22 describes the frequency configuration of the SFC clock.

Table 3-22 Frequency configuration of the SFC clock

Signal	Description
sfc_cksel	SFC2X clock source select. The 24 MHz clock is selected by default. x0: 24 MHz clock 01: 100 MHz clock 11: 125 MHz clock This signal can be controlled by configuring PERI_CRG48 bit[3:2].

Table 3-23 describes the frequency configuration of the NFC clock.

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Table 3-23 Frequency configuration of NFC clock

Signal	Description
nfc_cksel	NFC clock source select. The 24 MHz clock is selected by default. 0: 24 MHz clock 1: 100 MHz clock This signal can be controlled by configuring PERI_CRG52 bit[2].

Table 3-24 describes the frequency configurations of SIO0, SIO1, SIO2, and SIO3 clocks.

Table 3-24 Frequency configurations of SIO0, SIO1, SIO2, and SIO3 clocks

Signal	Description
sio0_ckcfg[23:0]	Division clock of SIO0/SIO1/SIO2/SIO3 MCLK. The configured value is calculated as follows: (MCLK0/Frequency of the SIO clock source) x 2^27. The clock source frequency is 500 MHz, and the maximum value of the MCLK is 62.5 MHz. This signal can be controlled by configuring PERI_CRG32 bit[23:0]. Note that SIO0 and SIO1 share an MCLK.
sio2_ckcfg[23:0]	Division clock of SIO2 MCLK. The configured value is calculated as follows: (MCLK2/Frequency of the SIO clock source) x 2^27. The clock source frequency is 500 MHz, and the maximum value of the MCLK is 62.5 MHz. This signal can be controlled by configuring PERI_CRG33 bit[23:0].
sio3_ckcfg[23:0]	Division clock of SIO3 MCLK. The configured value is calculated as follows: (MCLK3/Frequency of the SIO clock source) x 2^27. The clock source frequency is 500 MHz, and the maximum value of the MCLK is 62.5 MHz. This signal can be controlled by configuring PERI_CRG34 bit[23:0].
sio0_fsclk_div	Division relationship between the bit clock BCLK and sampling clock FS of SIO0. 000: The FS is generated by dividing the BCLK by 16. 001: The FS is generated by dividing the BCLK by 32. 010: The FS is generated by dividing the BCLK by 48. 011: The FS is generated by dividing the BCLK by 64. 100: The FS is generated by dividing the BCLK by 128. 101: The FS is generated by dividing the BCLK by 256. Other values: The FS is generated by dividing the BCLK by 8. This signal can be controlled by configuring PERI_CRG35 bit[14:12].
sio0_bclk_div	Division relationship between the main clock MCLK and bit clock BCLK of SIO0. 0000: The BCLK is generated by dividing the MCLK by 1. 0001: The BCLK is generated by dividing the MCLK by 3.

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Signal	Description
	0010: The BCLK is generated by dividing the MCLK by 2. 0011: The BCLK is generated by dividing the MCLK by 4. 0100: The BCLK is generated by dividing the MCLK by 6. 0101: The BCLK is generated by dividing the MCLK by 8. 0110: The BCLK is generated by dividing the MCLK by 12. 0111: The BCLK is generated by dividing the MCLK by 16. 1000: The BCLK is generated by dividing the MCLK by 24. 1001: The BCLK is generated by dividing the MCLK by 32. 1010: The BCLK is generated by dividing the MCLK by 48. 1011: The BCLK is generated by dividing the MCLK by 64. Other values: The BCLK is generated by dividing the MCLK by 8. This signal can be controlled by configuring PERI_CRG35 bit[11:8].
sio0_bclk_sel	SIO0 BCLK clock source select. 0: external BCLK of the Hi3521 1: internal BCLK of the Hi3521 This signal can be controlled by configuring PERI_CRG35 bit[4]. If the internal BCLK of the Hi3521 is selected, the FS CLK must be an internal clock generated in the Hi3521.
sio1_fsclk_div	Division relationship between the bit clock BCLK and sampling clock FS of SIO1. 000: The FS is generated by dividing the BCLK by 16. 001: The FS is generated by dividing the BCLK by 32. 010: The FS is generated by dividing the BCLK by 48. 011: The FS is generated by dividing the BCLK by 64. 100: The FS is generated by dividing the BCLK by 128. 101: The FS is generated by dividing the BCLK by 256. Other values: The FS is generated by dividing the BCLK by 8. This signal can be controlled by configuring PERI_CRG36 bit[14:12].
sio1_bclk_div	Division relationship between the main clock MCLK and bit clock BCLK of SIO1. 0000: The BCLK is generated by dividing the MCLK by 1. 0001: The BCLK is generated by dividing the MCLK by 3. 0010: The BCLK is generated by dividing the MCLK by 2. 0011: The BCLK is generated by dividing the MCLK by 4. 0100: The BCLK is generated by dividing the MCLK by 6. 0101: The BCLK is generated by dividing the MCLK by 8. 0110: The BCLK is generated by dividing the MCLK by 12. 0111: The BCLK is generated by dividing the MCLK by 16. 1000: The BCLK is generated by dividing the MCLK by 24.

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Signal	Description
	1001: The BCLK is generated by dividing the MCLK by 32. 1010: The BCLK is generated by dividing the MCLK by 48. 1011: The BCLK is generated by dividing the MCLK by 64. Other values: The BCLK is generated by dividing the MCLK by 8. This signal can be controlled by configuring PERI_CRG36 bit[11:8].
sio1_bclk_sel	SIO1 BCLK clock source select. 0: external BCLK of the Hi3521 1: internal BCLK of the Hi3521 This signal can be controlled by configuring PERI_CRG36 bit[4]. If the internal BCLK of the Hi3521 is selected, the FS CLK must be an internal clock generated in the Hi3521.
sio2_fsclk_div	Division relationship between the bit clock BCLK and sampling clock FS of SIO2. 000: The FS is generated by dividing the BCLK by 16. 001: The FS is generated by dividing the BCLK by 32. 010: The FS is generated by dividing the BCLK by 48. 011: The FS is generated by dividing the BCLK by 64. 100: The FS is generated by dividing the BCLK by 128. 101: The FS is generated by dividing the BCLK by 256. Other values: The FS is generated by dividing the BCLK by 8. This signal can be controlled by configuring PERI_CRG37 bit[14:12].
sio2_bclk_div	Division relationship between the main clock MCLK and bit clock BCLK of SIO2. 0000: The BCLK is generated by dividing the MCLK by 1. 0001: The BCLK is generated by dividing the MCLK by 3. 0010: The BCLK is generated by dividing the MCLK by 2. 0011: The BCLK is generated by dividing the MCLK by 4. 0100: The BCLK is generated by dividing the MCLK by 6. 0101: The BCLK is generated by dividing the MCLK by 8. 0110: The BCLK is generated by dividing the MCLK by 12. 0111: The BCLK is generated by dividing the MCLK by 16. 1000: The BCLK is generated by dividing the MCLK by 24. 1001: The BCLK is generated by dividing the MCLK by 32. 1010: The BCLK is generated by dividing the MCLK by 48. 1011: The BCLK is generated by dividing the MCLK by 64. Other values: The BCLK is generated by dividing the MCLK by 8. This signal can be controlled by configuring PERI_CRG37 bit[11:8].
sio2_bclk_sel	SIO2 BCLK clock source select. 0: external bclk of the Hi3521

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Signal	Description
	1: internal bclk of the Hi3521 This signal can be controlled by configuring PERI_CRG37 bit[4]. If the internal BCLK of the Hi3521 is selected, the FS CLK must be an internal clock generated in the Hi3521.
sio3_fsclk_div	Division relationship between the bit clock BCLK and sampling clock FS of SIO2. 000: The FS is generated by dividing the BCLK by 16. 001: The FS is generated by dividing the BCLK by 32. 010: The FS is generated by dividing the BCLK by 48. 011: The FS is generated by dividing the BCLK by 64. 100: The FS is generated by dividing the BCLK by 128. 101: The FS is generated by dividing the BCLK by 256. Other values: The FS is generated by dividing the BCLK by 8. This signal can be controlled by configuring PERI_CRG38 bit[14:12].
sio3_bclk_div	Division relationship between the main clock MCLK and bit clock BCLK of SIO2. 0000: The BCLK is generated by dividing the MCLK by 1. 0001: The BCLK is generated by dividing the MCLK by 3. 0010: The BCLK is generated by dividing the MCLK by 2. 0011: The BCLK is generated by dividing the MCLK by 4. 0100: The BCLK is generated by dividing the MCLK by 6. 0101: The BCLK is generated by dividing the MCLK by 8. 0110: The BCLK is generated by dividing the MCLK by 12. 0111: The BCLK is generated by dividing the MCLK by 16. 1000: The BCLK is generated by dividing the MCLK by 24. 1001: The BCLK is generated by dividing the MCLK by 32. 1010: The BCLK is generated by dividing the MCLK by 48. 1011: The BCLK is generated by dividing the MCLK by 64. Other values: The BCLK is generated by dividing the MCLK by 8. This signal can be controlled by configuring PERI_CRG38 bit[11:8].
sio3_bclk_sel	SIO2 BCLK clock source. 0: external bclk of the Hi3521 1: internal bclk of the Hi3521 This signal can be controlled by configuring PERI_CRG38 bit[4]. If the internal BCLK of the Hi3521 is selected, the FS CLK must be an internal clock generated in the Hi3521.

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The sampling rate clock frequency FSCLK is specified in general; however, the values of the bit clock BCLK and main clock MCLK are variable multiples of the value of FS. The following describes how to configure the clock frequency.

The clock source for SIO0 decimal division is fixed at 500 MHz. In this case, the required working clock frequencies of SIO0 are as follows: FSCLK = 48 kHz, MCLK = 256 FSCLK = 12.288 MHz, and BCLK = 16 FSCLK = 768 kHz. The following configurations are performed:

- The MCLK is generated by dividing a 500 MHz clock by a clock divider N. The value of N is calculated as follows: N = 12.288/500. Then sioclk_sel[23:0] is N x 2^{27}. The result is rounded off to 3298535. Therefore, the correct frequency of the MCLK is obtained after sioclk_sel is set to 0x0032_54E7.
- The BCLK is generated by dividing the MCLK. The clock divider is calculated as follows: BCLK/MCLK = 16/256 = 1/16. According to the mapping in Table 3-24, set sio0_bclk_div[3:0] to 0b0111 (corresponding to the clock divider 16). Then the correct frequency of the BCLK is obtained.
- FSCLK is generated by dividing the BCLK by 1/16. According to the mapping in Table 3-24, set sio0_fsclk_div to 0b000 (corresponding to the frequency divider 16). Then the correct frequency of the FS CLK is obtained.

Precautions

Take the following precautions when configuring clocks:

- By default, the A9 working clock is in crystal oscillator mode after power-on. That is, the crystal oscillator clock input by the XIN pin is selected.
- If the frequency of the PLL is changed, the PLL can output a stable clock 0.1 ms later. The frequency of the PLL can be changed only when the system runs in slow mode.
- If the PLL output clock is not stable, the system mode cannot be switched to PLL mode. You can view the PLL lock bit to check whether the PLL is locked. The status of the PLL lock bit can be obtained by reading PERI_CRG58 bit[4:0].

3.2.4 Register Summary

Table 3-25 describes CRG registers.

Table 3-25 Summary of CRG registers (base address: 0x2003_0000)

Offset Address	Register	Description	Page
0x0000	PERI_CRG0	APLL configuration register 0	3-23
0x0004	PERI_CRG1	APLL configuration register 1	3-24
0x0008	PERI_CRG2	VPLL0 configuration register 0	3-25
0x000C	PERI_CRG3	VPLL0 configuration register 1	3-25
0x0018	PERI_CRG6	VPLL2 configuration register 0	3-26
0x001C	PERI_CRG7	VPLL2 configuration register 1	3-27
0x0020	PERI_CRG8	EPLL configuration register 0	3-28

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Offset Address	Register	Description	Page
0x0024	PERI_CRG9	EPLL configuration register 1	3-29
0x0028	PERI_CRG10	A9 frequency mode and reset configuration register	3-30
0x002C	PERI_CRG11	VICAP clock and reset configuration register A	3-31
0x0030	PERI_CRG12	VICAP clock and reset configuration register B	3-33
0x0034	PERI_CRG13	VOU clock and reset control register	3-35
0x003C	PERI_CRG15	HDMI clock and reset control register	3-37
0x0040	PERI_CRG16	VEDU clock and soft reset control register	3-38
0x0048	PERI_CRG18	VPSS clock and soft reset control register	3-39
0x0050	PERI_CRG20	VDH clock and soft reset control register	3-40
0x0058	PERI_CRG22	TDE clock and soft reset control register	3-41
0x0060	PERI_CRG24	JPGE clock and soft reset control register	3-42
0x0064	PERI_CRG25	JPGD clock and soft reset control register	3-43
0x0068	PERI_CRG26	MDU clock and soft reset control register	3-44
0x006C	PERI_CRG27	VAPU clock and soft reset control register	3-45
0x0070	PERI_CRG28	VOIE clock and soft reset control register	3-46
0x0074	PERI_CRG29	VCMP clock and soft reset control register	3-47
0x007C	PERI_CRG31	CIPHER clock and soft reset control register	3-48
0x0080	PERI_CRG32	SIO0/SIO1 MCLK control register	3-48
0x0084	PERI_CRG33	SIO2 MCLK control register	3-49
0x0088	PERI_CRG34	SIO3 MCLK control register	3-49
0x008C	PERI_CRG35	SIO0 clock and soft reset control register	3-50
0x0090	PERI_CRG36	SIO1 clock and soft reset control register	3-51
0x0094	PERI_CRG37	SIO2 clock and soft reset control register	3-53
0x0098	PERI_CRG38	SIO3 clock and soft reset control register	3-55
0x00B4	PERI_CRG45	SATA clock and soft reset control register	3-56
0x00B8	PERI_CRG46	USB clock and soft reset control register	3-58
0x00C0	PERI_CRG48	SFC clock and soft reset control register	3-59
0x00C4	PERI_CRG49	SDIO clock and soft reset control register	3-59

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Offset Address	Register	Description	Page
0x00CC	PERI_CRG51	TOE and MAC interface clock and soft reset control register	3-60
0x00D0	PERI_CRG52	NANDC clock and soft reset control register	3-61
0x00D4	PERI_CRG53	SCD clock and soft reset control register	3-62
0x00D8	PERI_CRG54	eFUSE and DDRTEST clock and soft reset control register	3-63
0x00E0	PERI_CRG56	Direct memory access (DMA) clock and soft reset control register	3-64
0x00E4	PERI_CRG57	Soft reset control register for other CRG interface modules	3-64
0x00E8	PERI_CRG58	CRG status register	3-66
0x00EC	PERI_CRG59	GMAC port control register	3-67
0x00F0	PERI_CRG60	GMAC port status register	3-68
0x00F4	PERI_CRG61	Speed monitor control register	3-68
0x00F8	PERI_CRG62	Speed monitor status register 1	3-69
0x00FC	PERI_CRG63	Speed monitor status register 2	3-70

3.2.5 Register Description

PERI_CRG0

PERI_CRG0 is APLL configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0000	PERI_CRG0	0x0900_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		apll_bypass		apll_postdiv2				apll_postdiv1				apll_frac																			
Reset	0		0		0		0		1		0		0		0		0		0		0		0		0		0		0		0	

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.

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[30]	RW	apll_bypass	APLL clock frequency-division bypass control. 0: no bypass 1: bypass
[29:27]	RW	apll_postdiv2	Level-2 output divider of the APLL.
[26:24]	RW	apll_postdiv1	Level-1 output divider of the APLL.
[23:0]	RW	apll_frac	Decimal divider of the APLL.

PERI_CRG1

PERI_CRG1 is APLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0004	PERI_CRG1	0x006C_209B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								apll_dacpd	apll_dsmpd	apll_pd	apll_foutvcopd	apll_postdivpd	apll_fout4phasepd	apll_refdiv						apll_fbdiv											
Reset	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23]	RW	apll_dacpd	APLL test signal control. 0: power down 1: normal
[22]	RW	apll_dsmpd	APLL decimal frequency-division control. 0: decimal frequency-division mode 1: integer frequency-division mode
[21]	RW	apll_pd	APLL power down control. 0: power down 1: normal
[20]	RW	apll_foutvcopd	Power down control for the APLL VCO output. 0: no output clock 1: normal output clock

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[19]	RW	apll_postdivpd	Power down control for the APLL POSTDIV output. 0: no output clock 1: normal output clock
[18]	RW	apll_fout4phasepd	Power down control for the APLL FOUT output. 0: no output clock 1: normal output clock
[17:12]	RW	apll_refdiv	Divider of the APLL reference clock.
[11:0]	RW	apll_fbdiv	Integral multiplier of the APLL.

PERI_CRG2

PERI_CRG2 is VPLL0 configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0008	PERI_CRG2	0x0C00_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		vpll0_bypass		vpll0_postdiv2			vpll0_postdiv1					vpll0_frac																			
Reset	0		0		0		0		1		1		0		0		0		0		0		0		0		0		0		0	

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30]	RW	vpll0_bypass	VPLL0 clock frequency-division bypass control. 0: no bypass 1: bypass
[29:27]	RW	vpll0_postdiv2	Level-2 output divider of VPLL0.
[26:24]	RW	vpll0_postdiv1	Level-1 output divider of VPLL0.
[23:0]	RW	vpll0_frac	Decimal divider of VPLL0.

PERI_CRG3

PERI_CRG3 is VPLL0 configuration register 1.

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Offset Address	Register Name	Total Reset Value
0x000C	PERI_CRG3	0x006C_40B2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								vpll0_dacpd	vpll0_dsmpd	vpll0_pd	vpll0_foutvcopd	vpll0_postdivpd	vpll0_fout4phasepd	vpll0_refdiv						vpll0_fbdiv											
Reset	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	1	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23]	RW	vpll0_dacpd	VPLL0 test signal control. 0: power down 1: normal
[22]	RW	vpll0_dsmpd	VPLL0 decimal frequency-division control. 0: decimal frequency-division mode 1: integer frequency-division mode
[21]	RW	vpll0_pd	VPLL0 power down control. 0: power down 1: normal
[20]	RW	vpll0_foutvcopd	Power down control for the VPLL0 VCO output. 0: no output clock 1: normal output clock
[19]	RW	vpll0_postdivpd	Power down control for the VPLL0 POSTDIV output. 0: no output clock 1: normal output clock
[18]	RW	vpll0_fout4phasepd	Power down control for the VPLL0 FOUT output. 0: no output clock 1: normal output clock
[17:12]	RW	vpll0_refdiv	Divider of the VPLL0 reference clock.
[11:0]	RW	vpll0_fbdiv	Integral multiplier of VPLL0.

PERI_CRG6

PERI_CRG6 is VPLL2 configuration register 0.

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Offset Address	Register Name	Total Reset Value
0x0018	PERI_CRG6	0x0900_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	vpll2_bypass	vpll2_postdiv2				vpll2_postdiv1		vpll2_frac																							
Reset	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30]	RW	vpll2_bypass	VPLL2 clock frequency-division bypass control. 0: no bypass 1: bypass
[29:27]	RW	vpll2_postdiv2	Level-2 output divider of VPLL2.
[26:24]	RW	vpll2_postdiv1	Level-1 output divider of VPLL2.
[23:0]	RW	vpll2_frac	Decimal divider of VPLL2.

PERI_CRG7

PERI_CRG7 is VPLL2 configuration register 1.

Offset Address	Register Name	Total Reset Value
0x001C	PERI_CRG7	0x007C_2087

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								vpll2_dacpd	vpll2_dsmpd	vpll2_pd	vpll2_foutvcopd	vpll2_postdivpd	vpll2_fout4phasepd	vpll2_refdiv						vpll2_fbdiv											
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.

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Offset Address	Register Name	Total Reset Value
0x001C	PERI_CRG7	0x007C_2087

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								vpll2_dacpd	vpll2_dsmpd	vpll2_pd	vpll2_foutvcopd	vpll2_postdivpd	vpll2_fout4phasepd	vpll2_refdiv						vpll2_fbdiv												
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	1	1

Bits	Access	Name	Description
[23]	RW	vpll2_dacpd	VPLL2 test signal control. 0: power down 1: normal
[22]	RW	vpll2_dsmpd	VPLL2 decimal frequency-division control. 0: decimal frequency-division mode 1: integer frequency-division mode
[21]	RW	vpll2_pd	VPLL2 power down control. 0: power down 1: normal
[20]	RW	vpll2_foutvcopd	Power down control for the VPLL2 VCO output. 0: no output clock 1: normal output clock
[19]	RW	vpll2_postdivpd	Power down control for the VPLL2 POSTDIV output. 0: no output clock 1: normal output clock
[18]	RW	vpll2_fout4phasepd	Power down control for the VPLL2 FOUT output. 0: no output clock 1: normal output clock
[17:12]	RW	vpll2_refdiv	Divider of the VPLL2 reference clock.
[11:0]	RW	vpll2_fbdiv	Integral multiplier of VPLL2.

PERI_CRG8

PERI_CRG8 is EPLL configuration register 0.

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Offset Address	Register Name	Total Reset Value
0x0020	PERI_CRG8	0x0B00_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		epll_bypass		epll_postdiv2				epll_postdiv1				epll_frac																			
Reset	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30]	RW	epll_bypass	EPLL clock frequency-division bypass control. 0: no bypass 1: bypass
[29:27]	RW	epll_postdiv2	Level-2 output divider of the EPLL.
[26:24]	RW	epll_postdiv1	Level-1 output divider of the EPLL.
[23:0]	RW	epll_frac	Decimal divider of the EPLL.

PERI_CRG9

PERI_CRG9 is EPLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0024	PERI_CRG9	0x007C_207D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								epll_dacpd	epll_dsmpd	epll_pd	epll_foutvcopd	epll_postdivpd	epll_fout4phasepd	epll_refdiv						epll_fbdiv											
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	1	0	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.

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[23]	RW	epll_dacpd	EPLL test signal control. 0: power down 1: normal
[22]	RW	epll_dsmpd	EPLL decimal frequency-division control. 0: decimal frequency-division mode 1: integer frequency-division mode
[21]	RW	epll_pd	EPLL power down control. 0: power down 1: normal
[20]	RW	epll_foutvcopd	Power down control for the EPLLVCO output. 0: no output clock 1: normal output clock
[19]	RW	epll_postdivpd	Power down control for the EPLL POSTDIV output. 0: no output clock 1: normal output clock
[18]	RW	epll_fout4phasepd	Power down control for the EPLL FOUT output. 0: no output clock 1: normal output clock
[17:12]	RW	epll_refdiv	Divider of the EPLL reference clock.
[11:0]	RW	epll_fbdiv	Integral multiplier of the EPLL.

PERI_CRG10

PERI_CRG10 is an A9 frequency mode and reset configuration register.

Offset Address	Register Name	Total Reset Value
0x0028	PERI_CRG10	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cs_srst_req	cluster_scu_srst_req	r cluster_peri_srst_req	reserved	sc_wd_srst_req	cluster_dbg_srst_req	cpu_srst_req	reserved	freqmode_a9_sys		reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.

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[11]	RW	cs_srst_req	Chip select (CS) soft reset request. 0: deassert reset 1: reset
[10]	RW	cluster_scu_srst_req	Snoop control unit (SCU) soft reset request. 0: deassert reset 1: reset
[9]	RW	cluster_peri_srst_req	Peripheral (PERI) soft reset request. 0: deassert reset 1: reset
[8]	RO	reserved	Reserved.
[7]	RW	sc_wd_srst_req	WDG soft reset request. 0: deassert reset 1: reset
[6]	RW	cluster_dbg_srst_req	DBG soft reset request. 0: deassert reset 1: reset
[5]	RW	cpu_srst_req	CPU soft reset request. This bit is valid only in slave loading mode. 0: deassert reset 1: reset
[4]	RO	reserved	Reserved.
[3:2]	RW	freqmode_a9_sys	Frequency reduction configuration of the A9 clock. By masking the A9 clock pulse, the A9 frequency can be reduced and the ration of the A9 frequency to the AXI frequency can be adjusted. 00: A9:AXI = 3:1 01: A9:AXI = 3:1 10: A9:AXI = 2:1 11: A9:AXI = 1:1
[1:0]	RO	reserved	Reserved

PERI_CRG11

PERI_CRG11 is VICAP clock and reset configuration register A.

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Offset Address	Register Name	Total Reset Value
0x002C	PERI_CRG11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vi0_cken	vi1_cken	vi2_cken	vi3_cken	reserved				vi0div_cken	vi1div_cken	vi2div_cken	vi3div_cken	reserved				vi0_pctrl	vi1_pctrl	vi2_pctrl	vi3_pctrl	reserved				vi0_rst_req	vi1_rst_req	vi2_rst_req	vi3_rst_req	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	vi0_cken	VI0 ch clock gating. 0: disabled 1: enabled
[30]	RW	vi1_cken	VI1 ch clock gating. 0: disabled 1: enabled
[29]	RW	vi2_cken	VI2 ch clock gating. 0: disabled 1: enabled
[28]	RW	vi3_cken	VI3 ch clock gating. 0: disabled 1: enabled
[27:24]	RO	reserved	Reserved
[23]	RW	vi0div_cken	VI0 div ch clock gating. 0: disabled 1: enabled
[22]	RW	vi1div_cken	VI1 div ch clock gating. 0: disabled 1: enabled
[21]	RW	vi2div_cken	VI2 div ch clock gating. 0: disabled 1: enabled
[20]	RW	vi3div_cken	VI3 div ch clock gating. 0: disabled 1: enabled
[19:16]	RO	reserved	Reserved

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[15]	RW	vi0_pctrl	VI0 input associated clock phase control. 0: normal phase clock 1: reverse phase clock
[14]	RW	vi1_pctrl	VI1 input associated clock phase control. 0: normal phase clock 1: reverse phase clock
[13]	RW	vi2_pctrl	VI2 input associated clock phase control. 0: normal phase clock 1: reverse phase clock
[12]	RW	vi3_pctrl	VI3 input associated clock phase control. 0: normal phase clock 1: reverse phase clock
[11:8]	RO	reserved	Reserved
[7]	RW	vi0_rst_req	VI0 soft reset request. 0: deassert reset 1: reset
[6]	RW	vi1_rst_req	VI1 soft reset request. 0: deassert reset 1: reset
[5]	RW	vi2_rst_req	VI2 soft reset request. 0: deassert reset 1: reset
[4]	RW	vi3_rst_req	VI3 soft rest request. 0: deassert reset 1: reset
[3:0]	RO	reserved	Reserved

PERI_CRG12

PERI_CRG12 is VICAP clock and reset configuration register B.

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Offset Address	Register Name	Total Reset Value
0x0030	PERI_CRG12	0xE40A_A000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vi3_sc_sel		vi2_sc_sel		vi1_sc_sel		vi0_sc_sel		reserved	vi_selftest	vi_hcken	vi_hrst_req	vi0div_sel		vi1div_sel		vi2div_sel		vi3div_sel		reserved											
Reset	1	1	1	0	0	1	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	vi3_sc_sel	VI3 ch clock source select. 00: VI0 pad input clock 01: VI1 pad input clock 10: VI2 pad input clock 11: VI3 pad input clock
[29:28]	RW	vi2_sc_sel	VI2 ch clock source select. 00: VI0 pad input clock 01: VI1 pad input clock 10: VI2 pad input clock 11: VI3 pad input clock
[27:26]	RW	vi1_sc_sel	VI1 ch clock source select. 00: VI0 pad input clock 01: VI1 pad input clock 10: VI2 pad input clock 11: VI3 pad input clock
[25:24]	RW	vi0_sc_sel	VI0 ch clock source select. 00: VI0 pad input clock 01: VI1 pad input clock 10: VI2 pad input clock 11: VI3 pad input clock
[23]	RO	reserved	Reserved
[22]	RW	vi_selftest	VICAP selftest mode. 0: normal mode. The I/O input clock is selected. 1: self test mode. The on-chip 24 MHz test clock is selected.
[21]	RW	vi_hcken	VI bus clock gating. 0: disabled 1: enabled

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[20]	RW	vi_hrst_req	Soft reset request of the VIU bus. 0: deassert reset 1: reset
[19:18]	RW	vi0div_sel	VI0 div ch clock select. 00: div2 01: div4 10: div1 11: reserved
[17:16]	RW	vi1div_sel	VI1 div ch clock select. 00: div2 01: div4 10: div1 11: reserved
[15:14]	RW	vi2div_sel	VI2 div ch clock select. 00: div2 01: div4 10: div1 11: reserved
[13:12]	RW	vi3div_sel	VI3 div ch clock select. 00: div2 01: div4 10: div1 11: reserved
[11:0]	RO	reserved	Reserved

PERI_CRG13

PERI_CRG13 is VOU clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0034	PERI_CRG13	0x0000_0037

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vou_sdate0_cken	vou_sdate1_cken	vohd_out_cksel	vou_sd0_cken	vou_sd1_cken	vou_hd_cken	vou_hcken	sddac_pd_req	hddac_pd_req	vosd_out_pctrl	vohd_out_pctrl	reserved	vo_sd_srst_req	vo_hd_srst_req	vo_hrst_req	

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14]	RW	vou_sdate0_cken	VOU SDATE0 clock gating. 0: disabled 1: enabled
[13]	RW	vou_sdate1_cken	VOU SDATE1 clock gating. 0: disabled 1: enabled
[12]	RW	vohd_out_cksel	VO HD output associated clock source select. 0: HD1120 clock 1: SD656 clock
[11]	RW	vou_sd0_cken	VOU SD0 clock gating. 0: disabled 1: enabled
[10]	RW	vou_sd1_cken	VOU SD1 clock gating. 0: disabled 1: enabled
[9]	RW	vou_hd_cken	VOU HD clock gating. 0: disabled 1: enabled
[8]	RW	vou_hcken	VOU bus clock gating. 0: disabled 1: enabled
[7]	RW	sddac_pd_req	VOU SD DAC power-down configuration. 0: normal mode 1: power down
[6]	RW	hddac_pd_req	VOU HD DAC power-down configuration. 0: normal mode 1: power down
[5]	RW	vosd_out_pctrl	VOU SD output associated clock phase control. 0: normal phase clock 1: reverse phase clock
[4]	RW	vohd_out_pctrl	VOU HD output associated clock phase control. 0: normal phase clock 1: reverse phase clock
[3]	RO	reserved	Reserved.

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[2]	RW	vo_sd_srst_req	VO SD soft reset request. 0: deassert reset 1: reset
[1]	RW	vo_hd_srst_req	VO HD soft reset request. 0: deassert reset 1: reset
[0]	RW	vo_hrst_req	VOU bus soft reset request. 0: deassert reset 1: reset

PERI_CRG15

PERI_CRG15 is an HDMI clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x003C	PERI_CRG15	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								hdmi_test_sel	hdmi_cec_clk_sel	hdmi_asclk_sel	hdmi_osclk_sel	hdmi_idcken	hdmi_hcken	reserved	hdmi_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	RW	hdmi_test_sel	HDMI test clock select. 0: asclk clock 1: cec_clk clock
[6]	RW	hdmi_cec_clk_sel	HDMI CEC CLK clock select. 0: XTAL div12 clock 1: 2.04 MHz clock generated by dividing the PLL clock
[5]	RW	hdmi_asclk_sel	HDMI ASCLK clock select. 0: HDMI PHY clock 1: PLL clock
[4]	RW	hdmi_osclk_sel	HDMI OSCLK clock select. 0: HDMI PHY clock 1: PLL clock

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[3]	RW	hdmi_idcken	HDMI pixel clock gating. 0: disabled 1: enabled
[2]	RW	hdmi_hcken	HDMI bus clock gating. 0: disabled 1: enabled
[1]	RO	reserved	Reserved.
[0]	RW	hdmi_srst_req	HDMI soft reset request. 0: deassert reset 1: reset

PERI_CRG16

PERI_CRG16 is a VEDU clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0040	PERI_CRG16	0x0000_0C03

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				sed_cken	reserved	vedu0clk_loaden	vedu0clk_skipcfg					reserved		vedu_cken	vedu0_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11]	RW	sed_cken	SED clock gating. 0: disabled 1: enabled
[10]	RO	reserved	Reserved.

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[9]	RW	veduclk_loaden	VEDU clock frequency division configuration enable. 0: disabled 1: enabled To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to veduclk_loaden. 3 Write 1 to veduclk_loaden.
[8:4]	RW	veduclk_skipcfg	VEDU clock frequency division configuration. N: N-beat clocks are disabled every 32-beat VEDU clocks.
[3:2]	RO	reserved	Reserved.
[1]	RW	vedu_cken	VEDU clock gating. 0: disabled 1: enabled
[0]	RW	vedu_srst_req	VEDU soft reset request. 0: deassert reset 1: reset

PERI_CRG18

PERI_CRG18 is a VPSS clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0048	PERI_CRG18	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						vpsclk_loaden		vpsclk_skipcfg					reserved		vps_cken	vps_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.

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Offset Address	Register Name	Total Reset Value
0x0048	PERI_CRG18	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						vpsclk_loaden		vpsclk_skipcfg					reserved		vps_cken	vps_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[9]	RW	vpsclk_loaden	VPSS clock frequency division configuration enable. 0: disabled 1: enabled To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to vpsclk_loaden. 3 Write 1 to vpsclk_loaden.
[8:4]	RW	vpsclk_skipcfg	VPSS clock frequency division configuration. N: N-beat clocks are disabled every 32-beat VPSS clocks.
[3:2]	RO	reserved	Reserved.
[1]	RW	vps_cken	VPSS clock gating. 0: disabled 1: enabled
[0]	RW	vps_srst_req	VPSS soft reset request. 0: deassert reset 1: reset

PERI_CRG20

PERI_CRG20 is a VDH clock and soft reset control register.

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Offset Address	Register Name	Total Reset Value
0x0050	PERI_CRG20	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					vdh_pwrup_srst_req	vdhclk_loaden	vdhclk_skipcfg					reserved		vdh_cken	vdh_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved.
[10]	RW	vdh_pwrup_srst_req	VDH soft reset request 2. When the VDH module is restarted, it works properly only after being reset. 0: deassert reset 1: reset
[9]	RW	vdhclk_loaden	VDH clock frequency division configuration enable. 0: disabled 1: enabled To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to vdhclk_loaden. 3 Write 1 to vdhclk_loaden.
[8:4]	RW	vdhclk_skipcfg	VDH clock frequency division configuration. N: N-beat clocks are disabled every 32-beat VDH clocks.
[3:2]	RO	reserved	Reserved.
[1]	RW	vdh_cken	VDH clock gating. 0: disabled 1: enabled
[0]	RW	vdh_srst_req	VDH soft reset request 1. 0: deassert reset 1: reset

PERI_CRG22

PERI_CRG22 is a TDE clock and soft reset control register.

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Offset Address	Register Name	Total Reset Value
0x0058	PERI_CRG22	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						tdeclk_loaden	tdeclk_skipcfg					reserved		tde_cken	tde_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9]	RW	tdeclk_loaden	TDE clock frequency division configuration enable. 0: disabled 1: enabled To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to tdeclk_loaden. 3 Write 1 to tdeclk_loaden.
[8:4]	RW	tdeclk_skipcfg	TDE clock frequency division configuration. N: N-beat clocks are disabled every 32-beat TDE clocks.
[3:2]	RO	reserved	Reserved.
[1]	RW	tde_cken	TDE clock gating. 0: disabled 1: enabled
[0]	RW	tde_srst_req	TDE soft reset request. 0: deassert reset 1: reset

PERI_CRG24

PERI_CRG24 is a JPGE clock and soft reset control register.

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Offset Address	Register Name	Total Reset Value
0x0060	PERI_CRG24	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						jpgeclk_loaden		jpgeclk_skipcfg					reserved		jpge_cken	jpge_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9]	RW	jpgeclk_loaden	JPGE clock frequency division configuration enable. 0: disabled 1: enabled To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to jpgeclk_loaden. 3 Write 1 to jpgeclk_loaden.
[8:4]	RW	jpgeclk_skipcfg	JPGE clock frequency division configuration. N: N-beat clocks are disabled every 32-beat JPGE clocks.
[3:2]	RO	reserved	Reserved.
[1]	RW	jpge_cken	JPGE clock gating. 0: disabled 1: enabled
[0]	RW	jpge_srst_req	JPGE soft reset request. 0: deassert reset 1: reset

PERI_CRG25

PERI_CRG25 is a JPGD clock and soft reset control register.

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Offset Address	Register Name	Total Reset Value
0x0064	PERI_CRG25	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					jpgd_cksel	jpgdclk_loaden	jpgdclk_skipcfg					reserved		jpgd_cken	jpgd_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved.
[10]	RW	jpgd_cksel	JPGD clock source select. 0: 300 MHz clock 1: 250 MHz clock
[9]	RW	jpgdclk_loaden	JPGD clock frequency division configuration enable. 0: disabled 1: enabled To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to jpgdclk_loaden. 3 Write 1 to jpgdclk_loaden.
[8:4]	RW	jpgdclk_skipcfg	JPGD clock frequency division configuration. N: N-beat clocks are disabled every 32-beat JPGD clocks.
[3:2]	RO	reserved	Reserved.
[1]	RW	jpgd_cken	JPGD clock gating. 0: disabled 1: enabled
[0]	RW	jpgd_srst_req	JPGD soft reset request. 0: deassert reset 1: reset

PERI_CRG26

PERI_CRG26 is an MDU clock and soft reset control register.

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Offset Address	Register Name	Total Reset Value
0x0068	PERI_CRG26	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						mduclk_loaden	mduclk_skipcfg					reserved		mdu_cken	mdu_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9]	RW	mduclk_loaden	MDU clock frequency division configuration enable. 0: disabled 1: enabled To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to mduclk_loaden. 3 Write 1 to mduclk_loaden.
[8:4]	RW	mduclk_skipcfg	MDU clock frequency division configuration. N: N-beat clocks are disabled every 32-beat MDU clocks.
[3:2]	RO	reserved	Reserved.
[1]	RW	mdu_cken	MDU clock gating. 0: disabled 1: enabled
[0]	RW	mdu_srst_req	MDU soft reset request. 0: deassert reset 1: reset

PERI_CRG27

PERI_CRG27 is a VAPU clock and soft reset control register.

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Offset Address	Register Name	Total Reset Value
0x006C	PERI_CRG27	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						vapuclk_loaden	vapuclk_skipcfg					reserved		vapu_cken	vapu_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9]	RW	vapuclk_loaden	VAPU clock frequency division configuration enable. 0: disabled 1: enabled To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to vapuclk_loaden. 3 Write 1 to vapuclk_loaden.
[8:4]	RW	vapuclk_skipcfg	VAPU clock frequency division configuration. N: N-beat clocks are disabled every 32-beat VAPU clocks.
[3:2]	RO	reserved	Reserved.
[1]	RW	vapu_cken	VAPU clock gating. 0: disabled 1: enabled
[0]	RW	vapu_srst_req	VAPU soft reset request. 0: deassert reset 1: reset

PERI_CRG28

PERI_CRG28 is a VOIE clock and soft reset control register.

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Offset Address	Register Name	Total Reset Value
0x0070	PERI_CRG28	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														aenc_cken	aenc_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RW	reserved	Reserved.
[1]	RW	voie_cken	VOIE clock gating. 0: disabled 1: enabled
[0]	RW	voie_srst_req	VOIE soft reset request. 0: deassert reset 1: reset

PERI_CRG29

PERI_CRG29 is a VCMP clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0074	PERI_CRG29	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												reserved		vcmp_cken	vcmp_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	vcmp_cken	VCMP clock gating. 0: disabled 1: enabled

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[0]	RW	vcmp_srst_req	VCMP soft reset request. 0: deassert reset 1: reset

PERI_CRG31

PERI_CRG31 is a CIPHER clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x007C	PERI_CRG31	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														cipher_cken	cipher_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	cipher_cken	CIPHER clock gating. 0: disabled 1: enabled
[0]	RW	cipher_srst_req	CIPHER soft reset request. 0: deassert reset 1: reset

PERI_CRG32

PERI_CRG32 is SIO0/SIO1 MCLK control register.

Offset Address	Register Name	Total Reset Value
0x0080	PERI_CRG32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								sio0_ckcfg																							

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:0]	RW	sio0_ckcfg	Division clock of SIO0 or SIO1 MCLK. The configured value is calculated as follows: (MCLK0/Frequency of the SIO clock source) x 2^27. The clock source frequency is 500 MHz, and the maximum value of the MCLK is 62.5 MHz.

PERI_CRG33

PERI_CRG33 is SIO2 MCLK control register.

Offset Address	Register Name	Total Reset Value
0x0084	PERI_CRG33	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								sio2_ckcfg																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:0]	RW	sio2_ckcfg	Division clock of SIO2 MCLK. The configured value is calculated as follows: (MCLK0/Frequency of the SIO clock source) x 2^27. The clock source frequency is 500 MHz, and the maximum value of the MCLK is 62.5 MHz.

PERI_CRG34

PERI_CRG34 is SIO3 MCLK control register.

Offset Address	Register Name	Total Reset Value
0x0088	PERI_CRG34	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								sio3_ckcfg																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:0]	RW	sio3_ckcfg	Division clock of SIO3 MCLK. The configured value is calculated as follows: (MCLK0/Frequency of the SIO clock source) x 2^27. The clock source frequency is 500 MHz, and the maximum value of the MCLK is 62.5 MHz.

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PERI_CRG35

PERI_CRG35 is SIO0 clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x008C	PERI_CRG35	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				sio0_fsclk_div				sio0_bclk_div				sio0_fs_rxtx_sel	sio0_bclk_rxtx_sel	reserved	sio0_bclk_sel	sio0_bclkout_pctrl		sio0_bclk_pctrl		sio0_cken		sio0_srst_req	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14:12]	RW	sio0_fsclk_div	Division relationship between the bit clock BCLK and sampling clock FS. 000: The FS is generated by dividing the BCLK by 16. 001: The FS is generated by dividing the BCLK by 32. 010: The FS is generated by dividing the BCLK by 48. 011: The FS is generated by dividing the BCLK by 64. 100: The FS is generated by dividing the BCLK by 128. 101: The FS is generated by dividing the BCLK by 256. Other values: The FS is generated by dividing the BCLK by 8.
[11:8]	RW	sio0_bclk_div	Division relationship between the main clock MCLK and bit clock BCLK. 0000: The BCLK is generated by dividing the MCLK by 1. 0001: The BCLK is generated by dividing the MCLK by 3. 0010: The BCLK is generated by dividing the MCLK by 2. 0011: The BCLK is generated by dividing the MCLK by 4. 0100: The BCLK is generated by dividing the MCLK by 6. 0101: The BCLK is generated by dividing the MCLK by 8. 0110: The BCLK is generated by dividing the MCLK by 12. 0111: The BCLK is generated by dividing the MCLK by 16. 1000: The BCLK is generated by dividing the MCLK by 24. 1001: The BCLK is generated by dividing the MCLK by 32. 1010: The BCLK is generated by dividing the MCLK by 48. 1011: The BCLK is generated by dividing the MCLK by 64. Other values: The BCLK is generated by dividing the MCLK by 8.

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[7]	RW	sio0_fs_rxtx_sel	Multiplexing relationship between the SIO0 TX FS and RX FS. 0: The RX FS is independent of the TX FS. 1: The TX FS multiplexes with the RX FS.
[6]	RW	sio0_bclk_rxtx_sel	Multiplexing relationship between the SIO0 TX BCLK and RX BCLK. 0: The RX BCLK is independent of the TX BCLK. 1: The TX BCLK multiplexes with the RX BCLK.
[5]	RO	reserved	Reserved.
[4]	RW	sio0_bclk_sel	SIO0 BCLK select. 0: external BCLK of the Hi3521 1: internal BCLK of the Hi3521
[3]	RW	sio0_bclkout_pctrl	Polarity of SIO0 BCLK output. 0: normal phase 1: reverse phase
[2]	RW	sio0_bclk_pctrl	SIO0 BCLK polarity. 0: normal phase 1: reverse phase
[1]	RW	sio0_cken	SIO0 clock gating. 0: disabled 1: enabled
[0]	RW	sio0_srst_req	SIO0 soft reset request. 0: deassert reset 1: reset

PERI_CRG36

PERI_CRG36 is SIO1 clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0090	PERI_CRG36	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5	4	3	2	1	0
Name	reserved				sio1_fsclk_div	sio1_bclk_div	sio1_fs_rxtx_sel	sio1_bclk_rxtx_sel	reserved	sio1_bclk_sel	sio1_bclkout_pctrl	sio1_bclk_pctrl	sio1_cken	sio1_srst_req

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14:12]	RW	sio1_fsclk_div	Division relationship between the bit clock BCLK and sampling clock FS of SIO1. 000: The FS is generated by dividing the BCLK by 16. 001: The FS is generated by dividing the BCLK by 32. 010: The FS is generated by dividing the BCLK by 48. 011: The FS is generated by dividing the BCLK by 64. 100: The FS is generated by dividing the BCLK by 128. 101: The FS is generated by dividing the BCLK by 256. Other values: The FS is generated by dividing the BCLK by 8.
[11:8]	RW	sio1_bclk_div	Division relationship between the main clock MCLK and bit clock BCLK of SIO1. 0000: The BCLK is generated by dividing the MCLK by 1. 0001: The BCLK is generated by dividing the MCLK by 3. 0010: The BCLK is generated by dividing the MCLK by 2. 0011: The BCLK is generated by dividing the MCLK by 4. 0100: The BCLK is generated by dividing the MCLK by 6. 0101: The BCLK is generated by dividing the MCLK by 8. 0110: The BCLK is generated by dividing the MCLK by 12. 0111: The BCLK is generated by dividing the MCLK by 16. 1000: The BCLK is generated by dividing the MCLK by 24. 1001: The BCLK is generated by dividing the MCLK by 32. 1010: The BCLK is generated by dividing the MCLK by 48. 1011: The BCLK is generated by dividing the MCLK by 64. Other values: The BCLK is generated by dividing the MCLK by 8.
[7]	RW	sio1_fs_rxtx_sel	Multiplexing relationship between the SIO1 TX FS and RX FS. 0: The RX FS is independent of the TX FS. 1: The TX FS multiplexes with the RX FS.
[6]	RW	sio1_bclk_rxtx_sel	Multiplexing relationship between the SIO1 TX BCLK and RX BCLK. 0: The RX BCLK is independent of the TX BCLK. 1: The TX BCLK multiplexes with the RX BCLK.
[5]	RO	reserved	Reserved.
[4]	RW	sio1_bclk_sel	SIO1 BCLK select. 0: external BCLK of the Hi3521 1: internal BCLK of the Hi3521

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[3]	RW	sio1_bclkout_pctrl	Polarity of SIO1 BCLK output. 0: normal phase 1: reverse phase
[2]	RW	sio1_bclk_pctrl	SIO1 BCLK polarity. 0: normal phase 1: reverse phase
[1]	RW	sio1_cken	SIO1 clock gating. 0: disabled 1: enabled
[0]	RW	sio1_srst_req	SIO1 soft reset request. 0: deassert reset 1: reset

PERI_CRG37

PERI_CRG37 is SIO2 clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0094	PERI_CRG37	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			sio2_fsclk_div				sio2_bclk_div				sio2_fs_rxtx_sel	sio2_bclk_rxtx_sel	reserved	sio2_bclk_sel	sio2_bclkout_pctrl	sio2_bclk_pctrl	sio2_cken	sio2_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14:12]	RW	sio2_fsclk_div	Division relationship between the bit clock BCLK and sampling clock FS of SIO2. 000: The FS is generated by dividing the BCLK by 16. 001: The FS is generated by dividing the BCLK by 32. 010: The FS is generated by dividing the BCLK by 48. 011: The FS is generated by dividing the BCLK by 64. 100: The FS is generated by dividing the BCLK by 128. 101: The FS is generated by dividing the BCLK by 256. Other values: The FS is generated by dividing the BCLK by 8.

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[11:8]	RW	sio2_bclk_div	Division relationship between the main clock MCLK and bit clock BCLK of SIO2. 0000: The BCLK is generated by dividing the MCLK by 1. 0001: The BCLK is generated by dividing the MCLK by 3. 0010: The BCLK is generated by dividing the MCLK by 2. 0011: The BCLK is generated by dividing the MCLK by 4. 0100: The BCLK is generated by dividing the MCLK by 6. 0101: The BCLK is generated by dividing the MCLK by 8. 0110: The BCLK is generated by dividing the MCLK by 12. 0111: The BCLK is generated by dividing the MCLK by 16. 1000: The BCLK is generated by dividing the MCLK by 24. 1001: The BCLK is generated by dividing the MCLK by 32. 1010: The BCLK is generated by dividing the MCLK by 48. 1011: The BCLK is generated by dividing the MCLK by 64. Other values: The BCLK is generated by dividing the MCLK by 8.
[7]	RW	sio2_fs_rxtx_sel	Multiplexing relationship between the SIO2 TX FS and RX FS. 0: The RX FS is independent of the TX FS. 1: The TX FS multiplexes with the RX FS.
[6]	RW	sio2_bclk_rxtx_sel	Multiplexing relationship between the SIO2 TX BCLK and RX BCLK. 0: The RX BCLK is independent of the TX BCLK. 1: The TX BCLK multiplexes with the RX BCLK.
[5]	RO	reserved	Reserved.
[4]	RW	sio2_bclk_sel	SIO2 BCLK select. 0: external BCLK of the Hi3521 1: internal BCLK of the Hi3521
[3]	RW	sio2_bclkout_pctrl	Polarity of SIO2 BCLK output. 0: normal phase 1: reverse phase
[2]	RW	sio2_bclk_pctrl	SIO2 BCLK polarity. 0: normal phase 1: reverse phase
[1]	RW	sio2_cken	SIO2 clock gating. 0: disabled 1: enabled
[0]	RW	sio2_srst_req	SIO2 soft reset request. 0: deassert reset 1: reset

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PERI_CRG38

PERI_CRG38 is SIO3 clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0098	PERI_CRG38	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		sio3_fsclk_div				sio3_bclk_div				sio3_fs_rxtx_sel	sio3_bclk_rxtx_sel	reserved	sio3_bclk_sel	sio3_bclkout_pctrl	sio3_bclk_pctrl	sio3_cken	sio3_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14:12]	RW	sio3_fsclk_div	Division relationship between the bit clock BCLK and sampling clock FS of SIO3. 000: The FS is generated by dividing the BCLK by 16. 001: The FS is generated by dividing the BCLK by 32. 010: The FS is generated by dividing the BCLK by 48. 011: The FS is generated by dividing the BCLK by 64. 100: The FS is generated by dividing the BCLK by 128. 101: The FS is generated by dividing the BCLK by 256. Other values: The FS is generated by dividing the BCLK by 8.
[11:8]	RW	sio3_bclk_div	Division relationship between the main clock MCLK and bit clock BCLK of SIO3. 0000: The BCLK is generated by dividing the MCLK by 1. 0001: The BCLK is generated by dividing the MCLK by 3. 0010: The BCLK is generated by dividing the MCLK by 2. 0011: The BCLK is generated by dividing the MCLK by 4. 0100: The BCLK is generated by dividing the MCLK by 6. 0101: The BCLK is generated by dividing the MCLK by 8. 0110: The BCLK is generated by dividing the MCLK by 12. 0111: The BCLK is generated by dividing the MCLK by 16. 1000: The BCLK is generated by dividing the MCLK by 24. 1001: The BCLK is generated by dividing the MCLK by 32. 1010: The BCLK is generated by dividing the MCLK by 48. 1011: The BCLK is generated by dividing the MCLK by 64. Other values: The BCLK is generated by dividing the MCLK by 8.

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[7]	RW	sio3_fs_rxtx_sel	Multiplexing relationship between the SIO3 TX FS and RX FS. 0: The RX FS is independent of the TX FS. 1: The TX FS multiplexes with the RX FS.
[6]	RW	sio3_bclk_rxtx_sel	Multiplexing relationship between the SIO3 TX BCLK and RX BCLK. 0: The RX BCLK is independent of the TX BCLK. 1: The TX BCLK multiplexes with the RX BCLK.
[5]	RO	reserved	Reserved.
[4]	RW	sio3_bclk_sel	SIO3 BCLK select. 0: external BCLK of the Hi3521 1: internal BCLK of the Hi3521
[3]	RW	sio3_bclkout_pctrl	Polarity of SIO3 BCLK output. 0: normal phase 1: reverse phase
[2]	RW	sio3_bclk_pctrl	SIO3 BCLK polarity. 0: normal phase 1: reverse phase
[1]	RW	sio3_cken	SIO3 clock gating. 0: disabled 1: enabled
[0]	RW	sio3_srst_req	SIO3 soft reset request. 0: deassert reset 1: reset

PERI_CRG45

PERI_CRG45 is a SATA clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00B4	PERI_CRG45	0x0000_0700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				sata_clk_sel	sata_cken	sata0_cken	sata1_cken	rst_alive_s	rst_rx1_s	rst_rx0_s	rst_tx1_s	rst_tx0_s	rst_sata_s	hrst_sata_s	rst_sataphy_s

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11]	RW	sata_clk_sel	SATA PHY reference clock select. 0: 125 MHz clock 1: 100 MHz clock
[10]	RW	sata_cken	Status of the SATA PHY and bus clock. 0: disabled 1: enabled
[9]	RW	sata0_cken	Status of the SATA controller port0 clock. 0: disabled 1: enabled
[8]	RW	sata1_cken	Status of the SATA controller port1 clock. 0: disabled 1: enabled
[7]	RW	rst_alive_s	Soft reset control for the alive clock domain of the SATA controller. 0: deassert reset 1: reset
[6]	RW	rst_rx1_s	Soft reset control for the clock domain of SATA controller rx1. 0: deassert reset 1: reset
[5]	RW	rst_rx0_s	Soft reset control for the clock domain of SATA controller rx0. 0: deassert reset 1: reset
[4]	RW	rst_tx1_s	Soft reset control for the clock domain of SATA controller tx1. 0: deassert reset 1: reset
[3]	RW	rst_tx0_s	Soft reset control for the clock domain of SATA controller tx0. 0: deassert reset 1: reset
[2]	RW	rst_sata_s	Soft reset control for the SATA controller interface. 0: deassert reset 1: reset
[1]	RW	hrst_sata_s	Soft reset control for the SATA controller bus. 0: deassert reset 1: reset

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[0]	RW	rst_sataphy_s	Soft reset control for the SATA PHY. 0: deassert reset 1: reset

PERI_CRG46

PERI_CRG46 is a USB clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00B8	PERI_CRG46	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								usb_cken	usb_ctrl_utmi1_req	usb_ctrl_utmi0_req	usb_ctrl_hub_req	usbphy_port1_treq	usbphy_port0_treq	usbphy_req	usb_ahb_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	RW	usb_cken	USB PHY reference clock gating. 0: disabled 1: enabled
[6]	RW	usb_ctrl_utmi1_req	Soft reset request of USB controller port1. 0: deassert reset 1: reset
[5]	RW	usb_ctrl_utmi0_req	Soft reset request of USB controller port0. 0: deassert reset 1: reset
[4]	RW	usb_ctrl_hub_req	Soft reset request of the USB controller hub. 0: deassert reset 1: reset
[3]	RW	usbphy_port1_treq	Soft reset request of USB PHY port1. 0: deassert reset 1: reset
[2]	RW	usbphy_port0_treq	Soft reset request of USB PHY port0. 0: deassert reset 1: reset

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[1]	RW	usbphy_req	Soft reset request of the USB PHY. 0: deassert reset 1: reset
[0]	RW	usb_ahb_srst_req	Soft reset request of the USB controller bus. 0: deassert reset 1: reset

PERI_CRG48

PERI_CRG48 is an SFC clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00C0	PERI_CRG48	0x0000_0002

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved							sfc_cksel	sfc_cken	sfc_srst_req
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	1	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3:2]	RW	sfc_cksel	SFC2X clock source select. The 24 MHz clock is selected by default. x0: 24MHz clock 01: 100 MHz clock 11: 125 MHz clock
[1]	RW	sfc_cken	SFC clock gating. 0: disabled 1: enabled
[0]	RW	sfc_srst_req	SFC soft reset request. 0: deassert reset 1: reset

PERI_CRG49

PERI_CRG49 is an SDIO clock and soft reset control register.

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Offset Address	Register Name	Total Reset Value
0x00C4	PERI_CRG49	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												sdioclk_pctrl	sdioclk_sel	sdio_cken	sdio_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	RW	sdioclk_pctrl	Polarity of the SDIO SAP clock. 0: normal phase 1: reverse phase
[2]	RW	sdioclk_sel	SDIO working clock select. 0: 24 MHz 1: 50 MHz
[1]	RW	sdio_cken	SDIO clock gating. 0: disabled 1: enabled
[0]	RW	sdio_srst_req	SDIO soft reset request. 0: deassert reset 1: reset

PERI_CRG51

PERI_CRG51 is a TOE and MAC interface clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00CC	PERI_CRG51	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										gmac0_if_srst_req	toe_cksel	toe_hcken	toe_hrst_req	toe_cken	toe_srst_req

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved.
[5]	RW	gmac0_if_srst_req	GMAC0_IF soft reset request. 0: deassert reset 1: reset
[4]	RW	toe_cksel	TOE working clock select. 0: 155MHz APB clock 1: 100 MHz clock
[3]	RW	toe_hcken	TOE bus clock gating. 0: disabled 1: enabled
[2]	RW	toe_hrst_req	TOE bus soft reset request. 0: deassert reset 1: reset
[1]	RW	toe_cken	TOE clock gating. 0: disabled 1: enabled
[0]	RW	toe_srst_req	TOE soft reset request. 0: deassert reset 1: reset

PERI_CRG52

PERI_CRG52 is a NANDC clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00D0	PERI_CRG52	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													nfc_cksel	nfc_cken	nfc_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.

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Offset Address	Register Name	Total Reset Value
0x00D0	PERI_CRG52	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													nfc_cksel	nfc_cken	nfc_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[2]	RW	nfc_cksel	NFC clock source select. The 24 MHz clock is selected by default. 0: 24 MHz clock 1: 100 MHz clock
[1]	RW	nfc_cken	NFC clock gating. 0: disabled 1: enabled
[0]	RW	nfc_srst_req	NFC soft reset request. 0: deassert reset 1: reset

PERI_CRG53

PERI_CRG53 is SCD clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00D4	PERI_CRG53	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												scd_cken	reserved	scd_srst_req	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.

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[3]	RW	scd_cken	SCD clock gating. 0: disabled 1: enabled
[2]	RO	reserved	Reserved.
[1]	RW	scd_srst_req	SCD0 soft reset request. 0: deassert reset 1: reset
[0]	RO	reserved	Reserved.

PERI_CRG54

PERI_CRG54 is an eFUSE and DDRTEST clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00D8	PERI_CRG54	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ddrtest_cken	ddrtest_srst_req	efuse_cken	efuse_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	RW	ddrtest_cken	DDRTEST clock gating. 0: disabled 1: enabled
[2]	RW	ddrtest_srst_req	DDRTEST soft reset request. 0: deassert reset 1: reset
[1]	RW	efuse_cken	eFUSE clock gating. 0: disabled 1: enabled
[0]	RW	efuse_srst_req	eFUSE soft reset request. 0: deassert reset 1: reset

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PERI_CRG56

PERI_CRG56 is a DMA clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00E0	PERI_CRG56	0x0000_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dma_cken	dma_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	dma_cken	DMA clock gating. 0: disabled 1: enabled
[0]	RW	dma_srst_req	DMA soft reset request. 0: deassert reset 1: reset

PERI_CRG57

PERI_CRG57 is a soft reset control register for other CRG interface modules.

Offset Address	Register Name	Total Reset Value
0x00E4	PERI_CRG57	0x0000_E060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																test_clk_sel	ddr0_pcken	uart_cksel	ssp_srst_req	i2c_srst_req	uart3_srst_req	uart2_srst_req	uart1_srst_req	uart0_srst_req	reserved	ddr_cken	reserved	ddrcomp_srst_req	rtc_srst_req	ir_srst_req	test_clk_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.

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[15]	RW	test_clk_sel	Test clock group select. 0: test clock group 2 (usb ohci_12m/usb free_clk/sata ckoword div2) 1: test clock group 1 (apb div2 /hdmi asclk/hdmi osclk/hdmi v_ck2x)
[14]	RW	ddr_pcken	DDR PCLK clock gating. 0: disabled 1: enabled
[13]	RW	uart_cksel	UART0, UART1, UART2, or UART3 clock select. 0: clk_apb clock 1: clk_3m clock
[12]	RW	ssp_srst_req	SSP soft reset request. 0: deassert reset 1: reset
[11]	RW	i2c_srst_req	I^2C soft reset request. 0: deassert reset 1: reset
[10]	RW	uart3_srst_req	UART3 soft reset request. 0: deassert reset 1: reset
[9]	RW	uart2_srst_req	UART2 soft reset request. 0: deassert reset 1: reset
[8]	RW	uart1_srst_req	UART1 soft reset request. 0: deassert reset 1: reset
[7]	RW	uart0_srst_req	UART0 soft reset request. 0: deassert reset 1: reset
[6]	RO	reserved	Reserved.
[5]	RW	ddr_cken	DDR 2X and 1X clock gating. 0: disabled 1: enabled
[4]	RO	reserved	Reserved.
[3]	RW	ddrcomp_srst_req	DDR COMP soft reset request. 0: deassert reset 1: reset

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[2]	RW	rtc_srst_req	RTC soft reset request. 0: deassert reset 1: reset
[1]	RW	ir_srst_req	IR soft reset request. 0: deassert reset 1: reset
[0]	RW	test_clk_en	Test clock enable. 0: All test clocks are disabled. 1: All test clocks are enabled.

PERI_CRG58

PERI_CRG58 is a CRG status register.

Offset Address	Register Name	Total Reset Value
0x00E8	PERI_CRG58	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												epll_lock	vpll2_lock	vpll0_lock	apll_lock
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	RO	epll_lock	EPLL lock status. 0: unlocked 1: locked
[2]	RO	vpll2_lock	VPLL2 lock status. 0: unlocked 1: locked
[1]	RO	vpll0_lock	VPLL0 lock status. 0: unlocked 1: locked
[0]	RO	apll_lock	APLL lock status. 0: unlocked 1: locked

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PERI_CRG59

PERI_CRG59 is a GMAC interface control register.

Offset Address	Register Name	Total Reset Value
0x00EC	PERI_CRG59	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								macif_phy_select			macif_duplex_mode	macif_tx_config		macif_link_status		macif_mac_speed		macif_port_select
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:5]	RW	macif_phy_select	Configure MACIF PHY interface mode. 000: MII mode 001: RGMII mode Others: reserved
[4]	RW	macif_duplex_mode	Configure MACIF PHY duplex mode. 0: half duplex mode 1: full duplex mode
[3]	RW	macif_tx_config	Configure MACIF transmit configuration enable signals 0: Tx Config Disable 1: Tx Config Enable
[2]	RW	macif_link_status	Configure MACIF PHY link status. 0: link down 1: link up
[1]	RW	macif_mac_speed	Configure MACIF 10/100 Mbps mode. 0: 10 Mbps 1: 100 Mbps
[0]	RW	macif_port_select	Configure MACIF 1000 Mbps mode enable. 0: 1000 Mbps 1: 10/100 Mbps

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PERI_CRG60

PERI_CRG60 is a GMAC port status register.

Offset Address	Register Name	Total Reset Value
0x00F0	PERI_CRG60	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												phy0_link_status		phy0_link_status		phy0_link_speed	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	RO	phy_link_status	PHY link status. 0: link down 1: link up
[2:1]	RO	phy_link_speed	Frequency of PHYconnecting to the clock. 00: 2.5 MHz 01: 25 MHz 10: 125 MHz 11: reserved
[0]	RO	phy_link_duplex_mode	PHY connect duplex mode. 0: half duplex mode 1: full duplex mode

PERI_CRG61

PERI_CRG61 is a speed monitor control register.

Offset Address	Register Name	Total Reset Value
0x00F4	PERI_CRG61	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													osc_en		osc_mode		osc_clk_en	

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RW	osc_en	Speed monitor enable. 0: disabled 1: enabled
[1]	RW	osc_mode	Speed monitor mode. 0: 150-step level 1: 200-step level
[0]	RW	osc_clk_en	Speed monitor clock enable. 0: disabled 1: enabled

PERI_CRG62

PERI_CRG62 is speed monitor status register 1.

Offset Address	Register Name	Total Reset Value
0x00F8	PERI_CRG62	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										osc_valid						osc_cpu_value								osc_vdh_value							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21:18]	RW	osc_valid	Status of the RING_OSC counter. 0: invalid; 1: valid. bit[21]: CPU RING_OSC Valid; bit[20]: VDH RING_OSC Valid; bit[19]: DDRC RING_OSC Valid; bit[18]: VEDU RING_OSC Valid.
[17:9]	RO	osc_cpu_value	Value of the CPU RING_OSC counter.
[8:0]	RO	osc_vdh_value	Value of the VDH RING_OSC_HVT counter.

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PERI_CRG63

PERI_CRG63 is speed monitor status register 2.

Offset Address	Register Name	Total Reset Value
0x00FC	PERI_CRG63	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																osc_vedu_value								osc_ddrc_value							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved.
[17:9]	RO	osc_vedu_value	Value of the VEDU RING_OSC counter.
[8:0]	RO	osc_ddrc_value	Value of the DDRC RING_OSC counter.

3.3 Interrupt System

The Hi3521 uses the integrated generic interrupt controller (GIC) of Cortex-A9 and supports a maximum of 128 interrupt sources. Table 3-26 describes the A9 interrupt sources.

Table 3-26 A9 interrupt sources of A9

Interrupt Bit	Interrupt Source	Interrupt Bit	Interrupt Source
0–31	For A9 internal use	80	Reserved
32	COMMTX[0]	81	Reserved
33	COMMRX[0]	82	Reserved
34	Watchdog	83	Reserved
35	Timer0	84	Reserved
36	Timer1	85	Reserved
37	Timer2	86	Reserved
38	Timer3	87	Reserved
39	RTC	88	IVE
40	UART0	89	HDMI
41	UART1	90	VICAP
42	UART2	91	VDP

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Interrupt Bit	Interrupt Source	Interrupt Bit	Interrupt Source
43	UART3	92	VEDU
44	SSP	93	Reserved
45	I2C	94	JPGE
46	NandC	95	JPGD
47	SFC	96	VDH
48	IR	97	Reserved
49	SIO0	98	TDE
50	SIO1	99	Reserved
51	SIO2	100	MD
52	SIO3	101	VCMP
53	Reserved	102	VOIE
54	Reserved	103	SCD
55	Reserved	104	Reserved
56	Reserved	105	GPIO0
57	Reserved	106	GPIO1
58	Software int	107	GPIO2
59	Reserved	108	GPIO3
60	Cipher	109	GPIO4
61	DMAC0	110	GPIO5
62	DMAC1	111	GPIO6
63	USB_EHCI	112	GPIO7
64	USB_OHCI	113	GPIO8
65	Reserved	114	GPIO9/GPIO10
66	Reserved	115	GPIO11/GPIO12
67	SDIO	116	GPIO13/GPIO14
68	SATA	117	Reserved
69	L2CACHE_CHK0_INT	118	toe_lpi_int
70	L2CACHE_CHK1_INT	119	toe_int
71	L2CACHE_INT_COMB	120	DDR_TEST

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Interrupt Bit	Interrupt Source	Interrupt Bit	Interrupt Source
72	A9_PMU_INT0	121	Reserved
73	Reserved	122	Reserved
74	Reserved	123	Reserved
75	Reserved	124	Reserved
76	Reserved	125	Reserved
77	Reserved	126	Reserved
78	Reserved	127	Reserved
79	VPSS		

3.4 System Controller

3.4.1 Overview

The system controller controls the operating mode from several aspects. To be specific, it controls the operating mode of the system, monitors the system status, manages the key functions of the system, and configures some functions of peripherals.

3.4.2 Features

The system controller has the following features:

- Controls and monitors the operating mode of the system.
- Controls the system clock and queries its status.
- Controls the system address remap and monitors its status.
- Provides general peripheral registers
- Provides write protection for key registers.
- Provides chip identification (ID) registers.

3.4.3 Function Description

Controlling the System Operating Mode

The system can work in any of the following modes:

- Normal mode

  In general, the system works in normal mode. In this mode, the system is driven by the output clock of the on-chip APLL. All modules can work properly under this clock source. Some peripherals can be driven by the output clock of VPLL0, VPLL1, or EPLL.

- Slow mode

  The slow mode is a low-speed mode. In this mode, the system is driven by the external crystal oscillator clock. Only part of on-chip peripherals (such as system controller, timer,

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NANDC, and SFC) work properly. Modules (such as the DDRC) that require high-speed clock cannot work under the crystal oscillator clock.

- Doze mode

  The doze mode is also a slow-speed mode, but its speed is lower than the speed of the slow mode. Only a few on-chip peripherals can work in doze mode. In this mode, the system is driven by a 46.875 kHz low-frequency clock. This clock is generated by dividing the external crystal oscillator. Except the CPU and a few modules (such as the system controller, timer, and IR), most on-chip peripherals and the memory interface cannot work in this mode.

The system controller provides a mode switching mechanism to switch the system clock source. The mode is switched by configuring three bits of the mode control register SC_CTRL [modectrl]. These bits define the operating mode to which the system is switched.

- 000: reserved
- 001: doze mode
- 010: slow mode
- 100: normal mode
- Other values: reserved

When the required system operating mode is specified by configuring the system mode control register, the system operating mode is switched to the target mode. In this case, no software intervention or command intervention is required.

The current system status can be queried by reading SC_CTRL [modestatus]. SC_CTRL [modestatus] shows not only the preceding three main modes (normal, slow, and doze modes), but also the following intermediate status between the main modes: SWfromPLL, SWtoPLL, PLLCTL, SWfromXTAL, SWtoXTAL, and XTALCTL.

NOTE

The normal, slow, and doze modes can be switched directly. For example, if the system is in normal mode, you can switch the system to doze mode by setting SC_CTRL [modectrl] to 001. The system mode is switched to SWfromPLL, slow, and then SWfromXTAL modes before being switched to the doze mode.

Figure 3-3 shows the process of switching the system mode.

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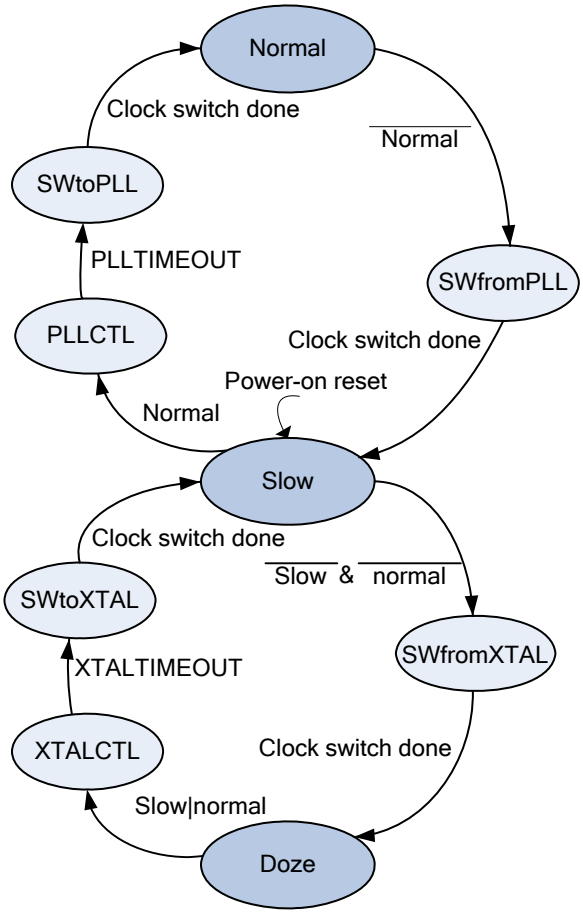
Figure 3-3 Process of switching the system mode



The operations involved in mode switching are as follows:

- When the most significant bit (MSB) of SC_CTRL [modectrl] is set to 0, the system exits the normal mode and is switched to the slow mode.
- Before being switched from the normal mode to the slow mode, the system is switched to the SWfromPLL status. This indicates that the system clock source is switched from the PLL to the crystal oscillator. After the clock switching is done, the system enters the slow mode.
- After power-on reset, the system is in slow mode. When the MSB of SC_CTRL [modectrl] is set to 1, the system enters the normal mode. During the switching to normal mode, the system is switched to the PLLCTL status to enable the ARMPLL. After a fixed wait time (the wait time depends on SC_XTALCTRL[plltime]), the system enters the SWtoPLL status to switch the clock source. After the switching is done, the system enters the normal mode.
- When the upper two bits of SC_CTRL [modectrl] are set to 0, the system is switched to the doze mode. In this case, the system is first switched to the SWfromXTAL status. This indicates that the system clock source is switched from the crystal oscillator clock to a

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46.875 kHz low-frequency clock. The 46.875 kHz clock is generated by dividing the crystal oscillator clock. After the clock switching is done, the system enters the doze mode.

- When either of the upper two bits of SC_CTRL [modectrl] is set to 1, the system is switched to the slow mode. During the switching to the slow mode, the system is switched to the XTALCTL status to initialize the clock module. After a fixed wait time (the wait time depends on SC_XTALCTRL[xtaltime]), the system enters the SWtoXTAL status to switch the clock source. After the switching is done, the system enters the slow mode.

For details about the mapping between the status of the system controller and system clocks, see Table 3-6.

Soft Reset

The system controller can soft-reset the entire chip or some modules.

After the global soft reset register SC_SYSRES is configured, the system controller transmits a reset request to the on-chip reset module for setting the Hi3521.

System Address Remap Control

For details, see section 1.3 "Boot Modes."

Write Protection for Key Registers

To avoid the entire system being severely affected by the misoperation on the system controller, the system controller provides write protection for key configuration registers. The key configuration registers are as follows:

- Mode switching control register: SC_CTRL
- Control register for system global soft reset: SC_SYSRES
- Peripheral control register 0 and peripheral control register 1: PERIPHCTRL0 and PERIPHCTRL1

Before writing to these key registers, you must disable the write protection function by configuring SC_LOCKEN. After writes, you need to enable the write protection function by configuring SC_LOCKEN again. This ensures that these key registers are not overwritten by the software arbitrarily.

NOTE

By default, write protection is not enabled for key registers after reset. It is recommended that you enable write protection by configuring SC_LOCKEN when the system starts.

System ID Register of the Chip

The system controller provides a chip ID register SC_SYSID. This register is a virtual 32-bit read-only register. It consists of four 8-bit ID registers: SC_SYSID3, SC_SYSID2, SC_SYSID1, and SC_SYSID0. After the values of these four registers are read and combined, the value of SC_SYSID, namely, 0x3521_0100, is obtained. Figure 3-4 shows the bit allocation of chip ID registers.

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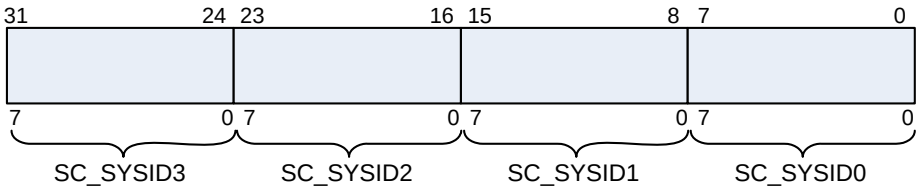
Figure 3-4 Bit allocation of chip ID registers



3.4.4 Register Summary

Table 3-27 describes the registers of the system controller.

Table 3-27 Summary of the system controller registers (base address: 0x2005_0000)

Offset Address	Register	Description	Page
0x000	SC_CTRL	System control register	3-77
0x004	SC_SYSRES	System soft reset register	3-81
0x008	SC_IMCTRL	Interrupt mode control register	3-81
0x00C	SC_IMSTAT	Interrupt mode status register	3-82
0x010	SC_XTALCTRL	Crystal oscillator control register	3-83
0x014	SC_PLLCTRL	PLL control register	3-83
0x01C	PERIPHCTRL0	Peripheral control register 0	3-85
0x0030	PERISTAT	Peripheral status register	3-86
0x0034	PERIPHCTRL2	Peripheral control register 2	3-87
0x0038	PERIPHCTRL3	Peripheral control register 3	3-88
0x003C	PERIPHCTRL4	Peripheral control register 4	3-89
0x0040	PERIPHCTRL5	Peripheral control register 5	3-90
0x0044	SC_LOCKEN	Lock register of key system control registers	3-91
0x0048	PERIPHCTRL6	Peripheral control register 6	3-91
0x004C	PERIPHCTRL7	Peripheral control register 7	3-92
0x0054	PERIPHCTRL9	Peripheral control register 9	3-93
0x0058	PERIPHCTRL10	Peripheral control register 10	3-94
0x005C	PERIPHCTRL11	Peripheral control register 11	3-95
0x0064	PERIPHCTRL13	Peripheral control register 13	3-95

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Offset Address	Register	Description	Page
0x0068	PERIPHCTRL14	Peripheral control register 14	3-96
0x006C	PERIPHCTRL15	Peripheral control register 15	3-97
0x0070	PERIPHCTRL16	Peripheral control register 16	3-97
0x0074	PERIPHCTRL17	Peripheral control register 17	3-98
0x0078	PERIPHCTRL18	Peripheral control register 18	3-99
0x007C	PERIPHCTRL19	Peripheral control register 19	3-100
0x0080	PERIPHCTRL20	USB control register (peripheral control register 20)	3-101
0x0084	PERIPHCTRL21	USB PHY control register 0 (peripheral control register 21)	3-103
0x0088	PERIPHCTRL22	USB PHY control register 1 (peripheral control register 22)	3-105
0x008C	SYSSTAT	System status register (PLL_LOCK)	3-107
0x00C0	PERIPHCTRL35	Software interrupt register	3-109
0x00D8	PERIPHCTRL41	Peripheral control register 41	3-110
0x00E4	PERIPHCTRL44	TOE control register	3-112
0x00E8	PERIPHCTRL45	TOE status register	3-113
0x00EC	PERIPHCTRL46	Peripheral control register 46	3-114
0x00F0	PERIPHCTRL47	Peripheral control register 47	3-115
0x0100	PERIPHCTRL51	Peripheral control register 51	3-115
0x0104	PERIPHCTRL52	Peripheral control register 52	3-117
0xEE0	SCSYSID0	Chip ID register 0	3-118
0xEE4	SCSYSID1	Chip ID register 1	3-119
0xEE8	SCSYSID2	Chip ID register 2	3-119
0xEEC	SCSYSID3	Chip ID register 3	3-119

3.4.5 Register Description

SC_CTRL

SC_CTRL is a system control register. It is used to specify the operations that are performed by the system.

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CAUTION

Write protection for this register can be enabled by configuring SC_LOCKEN. This register can be written only when write protection is disabled.

Offset Address	Register Name	Total Reset Value
0x000	SC_CTRL	0x0000_0212

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timeren7ov	timeren7sel	timeren6ov	timeren6sel	timeren5ov	timeren5sel	timeren4ov	timeren4sel	wdogenov	timeren3ov	timeren3sel	timeren2ov	timeren2sel	timeren1ov	timeren1sel	timeren0ov	timeren0sel	reserved					remapstat	remapclear	reserved	modestatus					modectrl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[31]	RW	timeren7ov	Count clock select of timer7. 0: The enable signals are provided by the reference clock. The reference clock is specified by [timeren7sel]. 1: bus clock
[30]	RW	timeren7sel	Count clock frequency select of timer7. This bit must be set to 0. 0: 3 MHz clock 1: reserved
[29]	RW	timeren6ov	Count clock select of timer6. 0: The enable signals are provided by the reference clock. The reference clock is specified by [timeren6sel]. 1: bus clock
[28]	RW	timeren6sel	Count clock frequency select of timer6. This bit must be set to 0. 0: 3 MHz clock 1: reserved
[27]	RW	timeren5ov	Count clock select of timer5. 0: The enable signals are provided by the reference clock. The reference clock is specified by [timeren5sel]. 1: bus clock
[26]	RW	timeren5sel	Count clock frequency select of timer5. This bit must be set to 0. 0: 3 MHz clock 1: reserved

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[25]	RW	timeren4ov	Count clock select of timer4. 0: The enable signals are provided by the reference clock. The reference clock is specified by [timeren4sel]. 1: bus clock
[24]	RW	timeren4sel	Count clock frequency select of timer4. This bit must be set to 0. 0: 3 MHz clock 1: reserved
[23]	RW	wdogenov	Watchdog count clock select. 0: 3 MHz clock 1: bus clock
[22]	RW	timeren3ov	Count clock select of timer3. 0: The enable signals are provided by the reference clock. The reference clock is specified by [timeren3sel]. 1: bus clock
[21]	RW	timeren3sel	Count clock frequency select of timer3. This bit must be set to 0. 0: 3 MHz clock 1: reserved
[20]	RW	timeren2ov	Count clock select of timer2. 0: The enable signals are provided by the reference clock. The reference clock is specified by [timeren2sel]. 1: bus clock
[19]	RW	timeren2sel	Count clock frequency select of timer2. This bit must be set to 0. 0: 3 MHz clock 1: reserved
[18]	RW	timeren1ov	Count clock select of timer1. 0: The enable signals are provided by the reference clock. The reference clock is specified by [timeren1sel]. 1: bus clock
[17]	RW	timeren1sel	Count clock frequency select of timer1. This bit must be set to 0. 0: 3 MHz clock 1: reserved
[16]	RW	timeren0ov	Count clock select of timer0. 0: The enable signals are provided by the reference clock. The reference clock is specified by [timeren0sel]. 1: bus clock

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[15]	RW	timeren0sel	Count clock frequency select of timer0. This bit must be set to 0. 0: 3 MHz clock 1: reserved
[14:10]	-	reserved	Reserved. Reading this field returns 0 and writing to this field has no effect.
[9]	RO	remapstat	Status of address remap. 0: The address is not remapped. 1: The address is remapped. The details are as follows: In auto-loading mode, NANDC CS0 or SFC CS1 is remapped to address 0. In slave loading mode, DDRCSN is remapped to address 0.
[8]	RW	remapclear	Address remap clear. 0: keep the remap status 1: clear the remap status For details about the address mappings before and after remapping is cleared, see Table 1-1.
[7]	-	reserved	Reserved. Reading this bit returns 0 and writing to this bit has no effect.
[6:3]	RW	modestatus	Mode status. The current operating mode of the system is returned. 0x0: reserved 0x1: doze 0x2: slow 0x3: XTAL CTL 0x4: normal 0x6: PLL CTL 0x9: SW from XTAL 0xA: SW from PLL 0xB: SW to XTAL 0xE: SW to PLL Other values: reserved
[2:0]	RW	modectrl	Mode control. This field defines the operating mode to which the system controller is switched. 000: reserved 001: doze 010: slow 100: normal

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SC_SYSRES

SC_SYSRES is a system soft reset register. When any value is written to this register, the system controller transmits a system soft reset request to the reset module. Then the reset module resets the system.

CAUTION

Write protection for this register can be enabled by configuring SC_LOCKEN. This register can be written only when write protection is disabled.

Offset Address	Register Name	Total Reset Value
0x004	SC_SYSRES	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	softresreq																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:0]	WO	softresreq	The system is reset when any value is written to this register.

SC_IMCTRL

SC_IMCTRL is an interrupt mode control register. It is used to control the system mode when an interrupt is generated.

Offset Address	Register Name	Total Reset Value
0x008	SC_IMCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								inmdtype	reserved			itmdctrl			itmden
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved. Reading this field returns 0x000000 and writing to this field has no effect.
[7]	RW	inmdtype	Type of the interrupt for triggering the interrupt mode of the system. 0: fast interrupt request (FIQ) interrupt 1: FIQ interrupt or interrupt request (IRQ) interrupt
[6:4]	-	reserved	Reserved.

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[3:1]	RW	itmdctrl	Operating mode of the system with the lowest speed in interrupt mode. The value obtained after the values of this register and SC_CTRL[modectrl] are ORed indicates the operating mode of the system after an interrupt is generated. The definitions of these bits are as follows: 000: sleep 001: doze 01X: slow 1XX: normal
[0]	RW	itmden	Interrupt mode enable. 0: disabled 1: enabled. When an interrupt is generated, the system enters the interrupt mode.

SC_IMSTAT

SC_IMSTAT is an interrupt mode status register. It is used to check whether the system is in interrupt mode. The system can be set to the interrupt mode forcibly by configuring this register.

CAUTION

When the interrupt service routine (ISR) ends, the interrupt mode must be cleared manually.

Offset Address	Register Name	Total Reset Value
0x00C	SC_IMSTAT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								itmdstat
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved. Reading this field returns 0x00000000 and writing to this field has no effect.

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[0]	RW	itmdstat	Interrupt mode status. The bit is used by software for controlling whether the system enters the interrupt mode. When the register is read: 0: The system is not in interrupt mode. 1: The system is in interrupt mode. When the register is written: 0: Software controls whether the system enters the interrupt mode. 1: Software does not control whether the system enters the interrupt mode.

SC_XTALCTRL

SC_XTALCTRL is a crystal oscillator control register. It is used to specify the stable wait time after the clock module is initialized. The stable wait time is the period when the system is switched from the XTAL CTL mode to the SW-to-XTAL mode.

Offset Address	Register Name	Total Reset Value
0x010	SC_XTALCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												xaltime																reserved		reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	-	reserved	Reserved. Reading this field returns 0x0000 and writing to this field has no effect.
[18:3]	RW	xtaltime	Wait time of crystal oscillator switching. The value of this field is used to specify the time spent on switching the system mode from XTAL CTL to SW-to-XTAL. The wait cycle can be calculated as follows: (65536 – xtaltime) x T46.8 K. T46.8 K indicates the clock cycle of the 46.8 kHz clock.
[2]	-	reserved	Reserved. Reading this bit returns 0x0 and writing to this bit has no effect.
[1:0]	-	reserved	Reserved. Reading this field returns the written value and writing to this field has no effect.

SC_PLLCTRL

SC_PLLCTRL is a PLL control register. It is used to control whether to enable the on-chip ARMPLL through software or system mode switching. It also sets the stable time of the ARMPLL.

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CAUTION

Write protection for this register can be enabled by configuring SC_LOCKEN. This register can be written only when write protection is disabled.

When the ARMPLL is enabled by switching the system mode (namely, by configuring SC_PLLCTRL[pllover]), the ARMPLL is disabled automatically if the system is not in normal mode.

The clock frequency of the APLL is controlled by PERI_CRG0 and PERI_CRG1. When the PLL frequency is changed, a stable clock can be output only after 0.5 ms. Therefore, the plltime of this register must meet this requirement.

Offset Address	Register Name	Total Reset Value
0x014	SC_PLLCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				plltime																								reserved		reserved	pllover
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved. Reading this bit returns 0x0 and writing to this bit has no effect.
[27:3]	RW	plltime	Stable time of the ARMPLL. This time refers to the period from the start of the PLL to the output of a stable PLL clock. That is, the wait time of switching the system mode from PLL CTL to SW-to-PLL. The timeout is calculated as follows: (33554432 – plltime) x TXIN. TXIN indicates the clock cycle of the external crystal oscillator of the Hi3521.
[2]	-	reserved	Reserved. Reading this bit returns 0x0 and writing to this bit has no effect.
[1]	-	reserved	Reserved.
[0]	RW	pllover	Whether the ARMPLL is enabled is controlled by the software rather than system mode switching. This bit must be set to 0. 0: The ARMPLL is enabled by switching the system mode. 1: reserved

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PERIPHCTRL0

PERIPHCTRL0 is peripheral control register 0.

Offset Address	Register Name	Total Reset Value
0x01C	PERIPHCTRL0	0x0000_3020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ddrc0_apb_gt_en	reserved		ddr0_odis_datah	ddr0_odis_datal	reserved			cfgsdisable	reserved		cfgnmfi	reserved	cp15sdisable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved.
[12]	RW	ddrc_apb_gt_en	DDRC APB clock gating. 0: disabled 1: enabled
[11:10]	RO	reserved	Reserved.
[9]	RW	ddr_odis_datah	Control for the upper 16-bit data pins of DDR. 0: enabled 1: disabled
[8]	RW	ddr_odis_datal	Control for the lower 16-bit data pins of DDR. 0: enabled 1: disabled
[7:5]	RO	reserved	Reserved.
[4]	RW	cfgsdisable	CPU set[4]. Disable write access to internal key configuration registers of the processor, including ICDDCR[0]=EnableSecure, secure interrupt defined in ICDICTR, and ICCICR (excluding the EnableNS bit). 0: disabled 1: enabled
[3]	RO	reserved	Reserved.
[2]	RW	cfgnmfi	CPU set[2]. CPU FIQ set to non-maskable interrupt (NMI) enable. 0: disabled 1: set the FIQs of CPU to NMIs
[1]	RO	reserved	Reserved.

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[0]	RW	cp15sdisable	CPU set[0]. Disable write access to internal secure registers of the processor, including c1 (SCTLR), c2 (TTBR0 and TTBCR), c3 (DACR), c10 (PRRR and NMRR), c12 (VBAR and MVBAR), and c13 (FCSEIDR) of the CP15 coprocessor. 0: disabled 1: enable

PERISTAT

PERISTAT is a peripheral status register.

Offset Address	Register Name	Total Reset Value
0x0030	PERISTAT	0x0000_07E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						vdh_poweroff_stat	reserved			vedu_poweroff_stat	vicap_poweroff_stat	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9]	RO	vdh_poweroff_stat	VDH power-off status. 0: powered off 1: not powered off
[8:6]	RO	reserved	Reserved.
[5]	RO	vedu_poweroff_stat	VEDU power-off status. 0: powered off 1: not powered off
[4]	RO	vicap_poweroff_stat	VICAP power-off status. 0: powered off 1: not powered off
[3:0]	RO	reserved	Reserved.

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PERIPHCTRL2

PERIPHCTRL2 is peripheral control register 2.

Offset Address	Register Name	Total Reset Value
0x0034	PERIPHCTRL2	0x0015_5500

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												vdh_iso_req	vdh_poweroff_req	reserved						vedu_iso_req	vedu_poweroff_req	vicap_iso_req	vicap_poweroff_req	ram2_2k_retn	ram2_2k_pgen	ram1_4k_retn	ram1_4k_pgen	ram0_4k_retn	ram0_4k_pgen	reserved	rom_pgen
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19]	RW	vdh_iso_req	VDH isolation area control. 0: not isolated 1: isolated
[18]	RW	vdh_poweroff_req	VDH power-off control. 0: powered off 1: not powered off
[17:12]	RO	reserved	Reserved.
[11]	RW	vedu_iso_req	VEDU isolation area control. 0: not isolated 1: isolated
[10]	RW	vedu_poweroff_req	VEDU power-off control. 0: powered off 1: not powered off
[9]	RW	vicap_iso_req	VICAP isolation area control. 0: not isolated 1: isolated
[8]	RW	vicap_poweroff_req	VICAP power-off control. 0: powered off 1: not powered off
[7]	RW	ram2_2k_retn	RAM2 data hold enable. 0: disabled 1: enabled

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[6]	RW	ram2_2k_pgen	RAM2 power supply enable. 0: enabled 1: disabled
[5]	RW	ram1_4k_retn	RAM1 data hold enable. 0: disabled 1: enabled
[4]	RW	ram1_4k_pgen	RAM1 power supply enable. 0: enabled 1: disabled
[3]	RW	ram0_4k_retn	RAM0 data hold enable. 0: disabled 1: enabled
[2]	RW	ram0_4k_pgen	RAM0 power supply enable. 0: enabled 1: disabled
[1]	RO	reserved	Reserved.
[0]	RW	rom_pgen	ROM power supply enable. 0: enabled 1: disabled

PERIPHCTRL3

PERIPHCTRL3 is peripheral control register 3.

Offset Address	Register Name	Total Reset Value
0x0038	PERIPHCTRL3	0x5D75_F000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9 8	7 6 5 4	3 2 1 0
Name	reserved						sata_phy0_mpll_ss_sel	sata_phy0_ref_clk_sel	

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Reset	0	1	0	1	1	1	0	1	0	1	1	1	0	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9:8]	RW	sata_phy0_mpll_ss_sel	Spread spectrum select. Reserved. This bit must be set to 0.
[7:0]	RW	sata_phy0_ref_clk_sel	Reference clock frequency select. A fixed offset value (in ppm) is set for the MPLL output clock. 0x00: no offset (default) 0x01–0xFF: reserved

PERIPHCTRL4

PERIPHCTRL4 is peripheral control register 4.

Offset Address	Register Name	Total Reset Value
0x003C	PERIPHCTRL4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												ram2_ck_gt_en	ram1_ck_gt_en	ram0_ck_gt_en	cbar_en	reserved		ssp_cs_sel		reserved								sdio0_det_mode		uart1_rts_ctrl	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved.
[19]	RW	ram2_ck_gt_en	RAM2 clock gating. 0: disabled 1: enabled
[18]	RW	ram1_ck_gt_en	RAM1 clock gating. 0: disabled 1: enabled
[17]	RW	ram0_ck_gt_en	RAM0 clock gating. 0: disabled 1: enabled

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[16]	RW	cbar_en	cbar_en output enable. 0: disabled 1: enabled
[15:14]	RO	reserved	Reserved.
[13:12]	RW	ssp_cs_sel	SSP CS select. 00: CS 0 01: CS 1 10: CS 2 11: CS 3
[11:3]	RO	reserved	Reserved.
[2]	RW	sdio0_det_mode	Signal detection mode of the SDIO0 card. 0: active low 1: active high
[1]	RW	uart1_rts_ctrl	UART1 RTS output control. 0: normal output 1: reverse output
[0]	RO	reserved	Reserved.

PERIPHCTRL5

PERIPHCTRL5 is peripheral control register 5.

Offset Address	Register Name	Total Reset Value
0x0040	PERIPHCTRL5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	count_en_media0_port1	over_value_media0_port1															count_en_media0_port0	over_value_media0_port0														

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	count_en_media0_port1	Timeout count enable for the VDH port. 0: disabled 1: enabled
[30:16]	RW	over_value_media0_port1	Timeout count value of the VDH port. Count value = over_value_media0_port1 x 2
[15]	RW	count_en_media0_port0	Timeout count enable for the VENC port. 0: disabled 1: enabled
[14:0]	RW	over_value_media0_port0	Timeout count value of the VENC port. Count value = over_value_media0_port0 x 2

SC_LOCKEN

SC_LOCKEN is a register for locking key system control registers.

Offset Address	Register Name	Total Reset Value
0x0044	SC_LOCKEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	scper_lockl																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	scper_lockl	Register for locking key system control registers. The key registers include SC_CTRL, SYSSTAT, and SC_PLLCTRL. When 0x1ACC_E551 is written to SC_LOCKEN, the write permission for all registers is enabled; when any other value is written to SC_LOCKEN, the write permission is disabled. Reading this register returns the lock status rather than its written value. 0x0000_0000: The write permission is enabled (unlocked). 0x0000_0001: The write permission is disabled (locked).

PERIPHCTRL6

PERIPHCTRL6 is peripheral control register 6.

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Offset Address	Register Name	Total Reset Value
0x0048	PERIPHCTRL6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	count_en_media0_port3	over_value_media0_port3															count_en_media0_port2	over_value_media0_port2														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	count_en_media0_port3	Timeout count enable for the JPGD port. 0: disabled 1: enabled
[30:16]	RW	over_value_media0_port3	Timeout count value of the JPGD port. Count value = over_value_media0_port3 x 2
[15]	RW	count_en_media0_port2	Timeout count enable for the JPGE port. 0: disabled 1: enabled
[14:0]	RW	over_value_media0_port2	Timeout count value of the JPGE port. Count value = over_value_media0_port2 x 2

PERIPHCTRL7

PERIPHCTRL7 is peripheral control register 7.

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Offset Address	Register Name	Total Reset Value
0x004C	PERIPHCTRL7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																count_en_media0_port4	over_value_media0_port4														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15]	RW	count_en_media0_port4	Timeout count enable for the MDU port. 0: disabled 1: enabled
[14:0]	RW	over_value_media0_port4	Timeout count value of the MDU port. Count value = over_value_media0_port4 x 2

PERIPHCTRL9

PERIPHCTRL9 is peripheral control register 9.

Offset Address	Register Name	Total Reset Value
0x0054	PERIPHCTRL9	0x0012_3456

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												media0_port4_pri				reserved	media0_port3_pri			reserved	media0_port2_pri			reserved	media0_port1_pri			reserved	media0_port0_pri		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	0	1	0	1	0	1	1	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved.

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[18:16]	RW	media0_port4_pri	MDU priority. The value 7 indicates the highest priority.
[15]	RO	reserved	Reserved.
[14:12]	RW	media0_port3_pri	JPGD priority. The value 7 indicates the highest priority.
[11]	RO	reserved	Reserved.
[10:8]	RW	media0_port2_pri	JPGE priority. The value 7 indicates the highest priority.
[7]	RO	reserved	Reserved.
[6:4]	RW	media0_port1_pri	VDH priority. The value 7 indicates the highest priority.
[3]	RO	reserved	Reserved.
[2:0]	RW	media0_port0_pri	VENC priority. The value 7 indicates the highest priority.

PERIPHCTRL10

PERIPHCTRL10 is peripheral control register 10.

Offset Address	Register Name	Total Reset Value
0x0058	PERIPHCTRL10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	count_en_port1	over_value_port1															count_en_port0	over_value_port0														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	count_en_port1	Timeout count enable for the advanced high-performance (AHB) bridge port 1. 0: disabled 1: enabled
[30:16]	RW	over_value_port1	Timeout count value of AHB bridge port 1 Count value = over_value_port1 x 2

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[15]	RW	count_en_port0	Timeout count enable for the AHB bridge port 0. 0: disabled 1: enabled
[14:0]	RW	over_value_port0	Timeout count value of the AHB bridge port 0. Count value = over_value_port0 x 2

PERIPHCTRL11

periphctrl11 is peripheral control register 11.

Offset Address	Register Name	Total Reset Value
0x005C	PERIPHCTRL11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	count_en_port3	over_value_port3															count_en_port2	over_value_port2														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	count_en_port3	Timeout count enable for the A9 port. 0: disabled 1: enabled
[30:16]	RW	over_value_port3	Timeout count value of the A9 port. Count value = over_value_port3 x 2
[15]	RW	count_en_port2	Timeout count enable for the IVE port. 0: disabled 1: enabled
[14:0]	RW	over_value_port2	Timeout count value of the IVE port. Count value = over_value_port2 x 2

PERIPHCTRL13

PERIPHCTRL13 is peripheral control register 13.

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Offset Address	Register Name	Total Reset Value
0x0064	PERIPHCTRL13	0x0012_3456

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																reserved	mst_pri3			reserved	mst_pri2			reserved	mst_pri1			reserved	mst_pri0		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	0	1	0	1	0	1	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15]	RO	reserved	Reserved.
[14:12]	RW	mst_pri3	A9 priority. The value 7 indicates the highest priority.
[11]	RO	reserved	Reserved.
[10:8]	RW	mst_pri2	IVE priority. The value 7 indicates the highest priority.
[7]	RO	reserved	Reserved.
[6:4]	RW	mst_pri1	Priority of AHB bridge 1. The value 7 indicates the highest priority.
[3]	RO	reserved	Reserved.
[2:0]	RW	mst_pri0	Priority of AHB bridge 0. The value 7 indicates the highest priority.

PERIPHCTRL14

PERIPHCTRL14 is peripheral control register 14.

Offset Address	Register Name	Total Reset Value
0x0068	PERIPHCTRL14	0x0012_3456

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	slave_priority_s4			reserved	slave_priority_s3			reserved	slave_priority_s2			reserved	slave_priority_s1		

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Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	0	1	0	1	0	1	1	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved.
[18:15]	RO	reserved	Reserved.
[14:12]	RW	slave_priority_s4	Priority for accessing the MDDRC0 bus over the SYS AXI s4 port. The value 7 indicates the highest priority.
[11]	RO	reserved	Reserved.
[10:8]	RW	slave_priority_s3	Priority for accessing the APB_MEDIA bus over the SYS AXI s3 port. The value 7 indicates the highest priority.
[7]	RO	reserved	Reserved.
[6:4]	RW	slave_priority_s2	Priority for accessing the APB_SYS bus over the SYS AXI s2 port. The value 7 indicates the highest priority.
[3]	RO	reserved	Reserved.
[2:0]	RW	slave_priority_s1	Priority for accessing the AHB of the SYS AXI s1 port. The value 7 indicates the highest priority.

PERIPHCTRL15

PERIPHCTRL15 is peripheral control register 15.

Offset Address	Register Name	Total Reset Value
0x006C	PERIPHCTRL15	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								chipid							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RO	chipid	8-bit chip ID. The chip ID is burnt by using the eFUSE module.

PERIPHCTRL16

PERIPHCTRL16 is peripheral control register 16.

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Offset Address	Register Name	Total Reset Value
0x0070	PERIPHCTRL16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	count_en_port1_media1	over_value_port1_media1															count_en_port0_media1	over_value_port0_media1														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	count_en_port1_media1	Timeout count enable for the TDE0 port. 0: disabled 1: enabled
[30:16]	RW	over_value_port1_media1	Timeout count value of the TDE0 port. Count value = over_value_port1_media1 x 2
[15]	RW	count_en_port0_media1	Timeout count enable for the VPSS port. 0: disabled 1: enabled
[14:0]	RW	over_value_port0_media1	Timeout count value of the VPSS port. Count value = over_value_port0_media1 x 2

PERIPHCTRL17

PERIPHCTRL17 is peripheral control register 17.

Offset Address	Register Name	Total Reset Value
0x0074	PERIPHCTRL17	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	count_en_port3_media1	over_value_port3_media1															count_en_port2_media1	over_value_port2_media1														

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	count_en_port3_media1	Timeout count enable for the VCMP port. 0: disabled 1: enabled
[30:16]	RW	over_value_port3_media1	Timeout count value of the VCMP port. Count value = over_value_port3_media1 x 2
[15]	RW	count_en_port2_media1	Timeout count enable for the TDE1 port. 0: disabled 1: enabled
[14:0]	RW	over_value_port2_media1	Timeout count value of the TDE1 port. Count value = over_value_port2_media1 x 2

PERIPHCTRL18

PERIPHCTRL18 is peripheral control register 18.

Offset Address	Register Name	Total Reset Value
0x0078	PERIPHCTRL18	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	count_en_port5_media1	over_value_port5_media1															count_en_port4_media1	over_value_port4_media1														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	count_en_port5_media1	Timeout count enable for the DDRTEST port. 0: disabled 1: enabled
[30:16]	RW	over_value_port5_media1	Timeout count value of the DDRTEST port. Count value = over_value_port5_media1 x 2
[15]	RW	count_en_port4_media1	Timeout count enable for the VOIE port. 0: disabled 1: enabled

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[14:0]	RW	over_value_port4_media1	Timeout count value of the VOIE port. Count value = over_value_port4_media1 x 2

PERIPHCTRL19

PERIPHCTRL19 is peripheral control register 19.

Offset Address	Register Name	Total Reset Value
0x007C	PERIPHCTRL19	0x0012_3456

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									mst_pri5_media1			reserved	mst_pri4_media1			reserved	mst_pri3_media1			reserved	mst_pri2_media1			reserved	mst_pri1_media1			reserved	mst_pri0_media1		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	0	1	0	1	0	1	1	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved.
[22:20]	RW	mst_pri5_media1	DDRTEST priority. The value 7 indicates the highest priority.
[19]	RO	reserved	Reserved.
[18:16]	RW	mst_pri4_media1	VOIE priority. The value 7 indicates the highest priority.
[15]	RO	reserved	Reserved.
[14:12]	RW	mst_pri3_media1	VCMP priority. The value 7 indicates the highest priority.
[11]	RO	reserved	Reserved.
[10:8]	RW	mst_pri2_media1	TDE1 priority. The value 7 indicates the highest priority.
[7]	RO	reserved	Reserved.
[6:4]	RW	mst_pri1_media1	TDE0 priority. The value 7 indicates the highest priority.
[3]	RO	reserved	Reserved.
[2:0]	RW	mst_pri0_media1	VPSS priority. The value 7 indicates the highest priority.

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PERIPHCTRL20

PERIPHCTRL20 is a USB control register (peripheral control register 20).

Offset Address	Register Name	Total Reset Value
0x0080	PERIPHCTRL20	0x0003_33A8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											preamble_sel	ovr_merge_en	pwr_merge_en	usbovr_p_ctrl	usbpwr_p_ctrl	phy1_ovrcur_en	phy0_ovrcur_en	phy1_pwr_en	phy0_pwr_en	reserved		ss_ena_incr16_i	ss_ena_incr8_i	ss_ena_incr4_i	ss_ena_incrx_align_i	ss_autoppd_on_overcur_en_i	reserved	ulpi_bypass_en	app_start_clk_i	ohci_susp_lgcy_i	wordinterface
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	1	0	1	0	1	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20]	RW	preamble_sel	Number of full-speed idle cycles after the full-speed signal preamble packet. 0: five full-speed idle cycles 1: four full-speed idle cycles
[19]	RW	ovr_merge_en	Share enable for the port overcurrent signal when [phy1_ovrcur_en] or [phy0_ovrcur_en] is 1. 0: disabled 1: enabled
[18]	RW	pwr_merge_en	[phy1_pwr_en] and [phy0_pwr_en] enable when a port is powered on. 0: disabled 1: enabled
[17]	RW	usbovr_p_ctrl	Polarity for overcurrent protection. 0: active low 1: active high
[16]	RW	usbpwr_p_ctrl	Polarity for power enable. 0: active low 1: active high
[15]	RW	phy1_ovrcur_en	Overcurrent protection enable for PHY1. 0: disabled 1: enabled

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[14]	RW	phy0_ovrcur_en	Overcurrent protection enable for PHY0. 0: disabled 1: enabled
[13]	RW	phy1_pwr_en	Power-off control for the PHY1 power supply. 0: powered off 1: enable the power output of the controller
[12]	RW	phy0_pwr_en	Power-off control for the PHY0 power supply. 0: powered off 1: enable the power output of the controller
[11:10]	RO	reserved	Reserved.
[9]	RW	ss_ena_incr16_i	AHB burst16 enable. 0: disabled 1: enabled
[8]	RW	ss_ena_incr8_i	AHB burst8 enable. 0: disabled 1: enabled
[7]	RW	ss_ena_incr4_i	AHB burst4 enable. 0: disabled 1: enabled
[6]	RW	ss_ena_incrx_align_i	Burst alignment enable. 0: disabled 1: enabled
[5]	RW	ss_autoppd_on_overcur_en_i	Port automatic power-off enable during overcurrent. 0: disabled 1: enabled
[4]	RO	reserved	Reserved (ULPI mode16_en).
[3]	RW	ulpi_bypass_en	ULPI bypass control. **This bit must be set to 1**. 0: ULPI mode 1: UTMI mode
[2]	RW	app_start_clk_i	Open host controller interface (OHCI) clock control. 0: The OHCI works properly. 1: The OHCI clock is enabled in suspend mode.
[1]	RW	ohci_susp_lgcy_i	Strap input signal when the OHCI is suspended.
[0]	RW	wordinterface	Data bit width select of the UTMI interface. 0: 8 bits 1: 16 bits

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PERIPHCTRL21

PERIPHCTRL21 is USB PHY control register 0 (peripheral control register 21).

Offset Address	Register Name	Total Reset Value
0x0084	PERIPHCTRL21	0x001D_2188

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								siddq	commononn	phy0_txhsxvtune		phy0_sleepm	phy0_loopbackenb	phy0_compdistune		phy0_sqrxtune		phy0_txfslstune				phy0_txpreemphasistune		reserved		phy0_txrisetune		phy0_txverftune			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0	1	0	0	0	0	1	1	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:23]	-	reserved	Reserved.
[22]	RW	siddq	Analog power-off test enable of the PHY. 0: do not power off the analog power 1: power off the analog power The default value is 0. The bit must be set to 0 before the built-in self test (BIST).
[21]	RW	commononn	Indicates whether XO BIAS BANDGAP PLL works when the PHY is suspended. 0: clk48m_ohci output is always valid even when the PHY is suspended. 1: clk48m_ohci output is valid except when the PHY is suspended.
[20:19]	RW	phy0_txhsxvtune	Crossover voltage tune signal of DP/DM. 00: reserved 01: –15 mV 10: +15 mV 11: default
[18]	RW	phy0_sleepm	Sleep mode of port 0. 0: sleep mode 1: normal mode
[17]	RW	phy0_loopbackenb	Loopback (from D+ to D-) test enable signal of PHY0. This bit must be set to 0.

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[16:14]	RW	phy0_compdistune	HOSDISCONNECT threshold level tune signal of PHY0. 000: –6% 001: –4.5% 010: –3% 100: default value 101: +1.5% 110: +3% 111: +4.5% Other values: reserved
[13:11]	RW	phy0_sqrxtune	Squelch circuit tune signal of PHY0. 000: +20% 001: +15% 010: +10% 011: +5% 100: default value 101: –5% 110: –10% 111: –15%
[10:7]	RW	phy0_txfslstune	FS LS impedance tune signal of PHY0. 0x0: +5% 0x1: +2.5% 0x3: default value 0x7: –2.5% 0xF: –5% Other values: reserved
[6]	RW	phy0_txpreemphasistune	Pre-emphasis transmit enable signal of PHY0 in HS mode. The default value is 0. 0: disabled 1: enabled
[5]	RW	reserved	Reserved.
[4]	RW	phy0_txrisetune	High-speed signal up/down time tune of PHY0. 0: default value 1: –8%

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[3:0]	RW	phy0_txverftune	DC level tune signal in HS mode of PHY0. 0x0: –10% 0x1: –8.75% 0x2: –7.5% 0x3: –6.25% 0x4: –5% 0x5: –3.75% 0x6: –2.5% 0x7: –1.25% 0x8: default value 0x9: +1.25% 0xA: +2.5% 0xB: +3.7% 0xC: +5% 0xD: +6.25% 0xE: +7.5% 0xF: +8.75%

PERIPHCTRL22

PERIPHCTRL22 is USB PHY control register 1 (peripheral control register 22).

Offset Address	Register Name	Total Reset Value
0x0088	PERIPHCTRL22	0x701D_2188

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												phy1_txhsxvtune		phy1_sleepm		phy1_loopbackenb		phy1_compdistune		phy1_sqrxtune		phy1_txfslstune		phy1_txpreemphasistune		reserved		phy1_txrisetune		phy1_txvreftune	
Reset	0	1	1	1	0	0	0	0	0	0	0	1	1	1	0	1	0	0	1	0	0	0	0	1	1	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.

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[20:19]	RW	phy1_txhsxvtune	Crossover voltage tune signal of DP/DM. 00: reserved 01: –15 mV 10: +15 mV 11: default
[18]	RW	phy1_sleepm	Sleep mode of port 1. 0: sleep mode 1: normal mode
[17]	RW	phy1_loopbackenb	Loopback (from D+ to D-) test enable signal of PHY1. The default value is 0, and this bit must be set to 0.
[16:14]	RW	phy1_compdistune	HOSDISCONNECT threshold level tune signal of PHY1. 000: –6% 001: –4.5% 010: –3% 100: default value 101: +1.5% 110: +3% 111: +4.5% Other values: reserved
[13:11]	RW	phy1_sqrxtune	Squelch circuit tune signal of PHY1. 000: +20% 001: +15% 010: +10% 011: +5% 100: default value 101: –5% 110: –10% 111: –15%
[10:7]	RW	phy1_txfslstune	FS LS impedance tune signal of PHY1. 0x0: +5% 0x1: +2.5% 0x3: default value 0x7: –2.5% 0xF: –5% Other values: reserved
[6]	RW	phy1_txpreemphasistune	Pre-emphasis transmit enable signal of PHY1 in HS mode. The default value is 0. 0: disabled 1: enabled

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[5]	RO	reserved	Reserved.
[4]	RW	phy1_txrisetune	High-speed signal up/down time tune of PHY1. 0: default value 1: –8%
[3:0]	RW	phy1_txvreftune	DC level tune signal in HS mode of PHY1. 0x0: –10% 0x1: –8.75% 0x2: –7.5% 0x3: –6.25% 0x4: –5% 0x5: –3.75% 0x6: –2.5% 0x7: –1.25% 0x8: default value 0x9: +1.25% 0xA: +2.5% 0xB: +3.7% 0xC: +5% 0xD: +6.25% 0xE: +7.5% 0xF: +8.75%

SYSSTAT

SYSSTAT is a system status register (PLL_LOCK).

Offset Address	Register Name	Total Reset Value
0x008C	SYSSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bootrom_sel_in		nf_block_size		a9_l2_idle	a9_smp_namp	reserved						a9_standbywfe	a9_standbywfi	a9_pmupriv	a9_secure	reserved	nf_ecc_type			nf_addr_num		nf_page_size		jtag_sel		boot_mode		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	bootrom_sel_in	Whether the system boots from the bootrom. 0: no 1: yes
[30:29]	RO	nf_block_size	Block size of the NAND flash during booting. 00: 64 pages for the SLC component 01: 128 pages for the MLC component 10: 256 page 11: 512 page
[28]	RO	a9_l2_idle	L2 cache status. 0: non-idle 1: idle
[27]	RO	a9_smp_namp	Whether the Cortex-A9 processor is in equalization mode. 0: non-equalization mode 1: equalization mode
[26:20]	RO	reserved	Reserved.
[19]	RO	a9_standbywfe	Whether the Cortex-A9 processor is in wait for event (WFE) status. 0: non-WFE status 1: WFE status
[18]	RO	a9_standbywfi	Whether the Cortex-A9 processor is in wait for interrupt (WFI) status. 0: non-WFI status 1: WFI status
[17]	RO	a9_pmupriv	Mode of the Cortex-A9 processor. 0: user mode 1: privileged mode
[16]	RO	a9_secure	Secure status of the Cortex-A9 processor. 0: non-secure status 1: secure status
[15]	RO	reserved	Reserved.

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[14:12]	RO	nf_ecc_type	ECC mode of the NAND flash during booting. 000: non-ECC mode 001: 1-bit mode 010: 4-byte mode 011: 8-byte mode 100: 24-bit mode 101: 40-bit mode Other values: reserved
[11]	RO	nf_addr_num	Number of addresses sent to the NAND flash. Note: This bit is valid only during power-on. 0: four addresses 1: five addresses
[10:8]	RO	nf_page_size	Page size of the NAND flash during booting. 000: 512 bytes 001: 2 KB 010: 4 KB 011: 8 KB 100: 16 KB Other values: reserved
[7:6]	RO	jtag_sel	Selected debugging mode of the chip. 00: debug A9 01: reserved 10: debug SATA PHY 11: reserved
[5:4]	RO	boot_mode	Selected boot mode of the chip. 00: boot from the SPI flash 01: reserved 10: boot from the NAND flash 11: reserved
[3:0]	RO	reserved	Reserved.

PERIPHCTRL35

PERIPHCTRL35 is a software interrupt configuration register.

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Offset Address	Register Name	Total Reset Value
0x00C0	PERIPHCTRL35	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															software_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	software_int	Software interrupts. 0: No interrupt is generated. 1: An interrupt is generated.

PERIPHCTRL41

PERIPHCTRL41 is peripheral control register 41 (MDDRC out-of-order configuration register outtodr_ctrl).

Offset Address	Register Name	Total Reset Value
0x00D8	PERIPHCTRL41	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cpu_ctrl	reserved	toe_axi	sys_axi	bpd_ctrl	jpgd_ctrl	mdu_ctrl	vcmp_ctrl	vdh1_ctrl	venc1_ctrl	vpss1_ctrl	jpge_ctrl	voie_ctrl	vdh0_ctrl	venc0_ctrl	tde1_ctrl	tde0_ctrl	vpss0_ctrl	reserved	vicap_ctrl	vou_ctrl
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20]	RW	cpu_ctrl	Indicates whether out-of-order is allowed when the CPU accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[19]	RO	reserved	Reserved.

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[18]	RW	toe_ctrl	Indicates whether out-of-order is allowed when the TOE accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[17]	RW	ive_ctrl	Indicates whether out-of-order is allowed when the IVE subsystem accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[16]	RO	reserved	Reserved.
[15]	RW	ddrtest_ctrl	Indicates whether out-of-order is allowed when the DDRTEST accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[14]	RW	voie_ctrl	Indicates whether out-of-order is allowed when the VOIE accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[13]	RW	vcmp_ctrl	Indicates whether out-of-order is allowed when the VCMP accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[12]	RW	tde1_ctrl	Indicates whether out-of-order is allowed when TDE1 accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[11]	RW	tde0_ctrl	Indicates whether out-of-order is allowed when TDE0 accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[10]	RW	vpss_ctrl	Indicates whether out-of-order is allowed when VPSS accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[9:8]	RO	reserved	Reserved.
[7]	RW	mdu_ctrl	Indicates whether out-of-order is allowed when MDU accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.

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[6]	RW	jpgd_ctrl	Indicates whether out-of-order is allowed when JPGD accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[5]	RW	jpge_ctrl	Indicates whether out-of-order is allowed when JPGE accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[4]	RW	vdh_ctrl	Indicates whether out-of-order is allowed when VDH accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[3]	RW	vedu_ctrl	Indicates whether out-of-order is allowed when VEDU accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[2]	RO	reserved	Reserved.
[1]	RW	vicap_ctrl	Indicates whether out-of-order is allowed when the VICAP accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[0]	RW	vou_ctrl	Indicates whether out-of-order is allowed when the VOU accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.

PERIPHCTRL44

PERIPHCTRL44 is a TOE control register.

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Offset Address	Register Name	Total Reset Value
0x00E4	PERIPHCTRL44	0x0000_0011

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sbd_data_endianess	reserved					mac_emisc_pwr_down_ctrl	mac_emisc_pwr_clamp_ctrl	mac_pmt_intr_enable	mac_lpi_intr_enable	reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15]	RW	sbd_data_endianess	Endian mode for processing the TOE DMA data. 1: big endian 0: little endian
[14:10]	RO	reserved	Reserved.
[9]	RW	mac_emisc_pwr_down_ctrl	Power-off control signal of MAC, active high.
[8]	RW	mac_emisc_pwr_clamp_ctrl	VDD power control signal of the isolated cells of MAC, active high.
[7]	RW	mac_pmt_intr_enable	Network wakeup interrupt enable of MAC, active high.
[6]	RW	mac_lpi_intr_enable	LPI status exit interrupt enable of MAC, active high.
[5:0]	RO	reserved	Reserved.

PERIPHCTRL45

PERIPHCTRL45 is a TOE status register.

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Offset Address	Register Name	Total Reset Value
0x00E8	PERIPHCTRL45	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		mac0_speed		reserved										mac_pwr_down_ack	reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.
[13:12]	RO	mac_speed	Operating speed of MAC. 0x: 1000 Mbps 10: 10 Mbps 11: 100 Mbps
[11:2]	RO	reserved	Reserved.
[1]	RO	mac_pwr_down_ack	Indicates that MAC always-on block is actively programmed and the power management controller can start switching off the power.
[0]	RO	reserved	Reserved.

PERIPHCTRL46

PERIPHCTRL46 is peripheral control register 46.

Offset Address	Register Name	Total Reset Value
0x00EC	PERIPHCTRL46	0x0033_3333

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								timers_ram2								timers_ram1								timers_ram0							
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RW	timers_ram2	RAM2 timeout period (n x 3.3 ns).
[15:8]	RW	timers_ram1	RAM1 timeout period (n x 3.3 ns).
[7:0]	RW	timers_ram0	RAM0 timeout period (n x 3.3 ns).

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PERIPHCTRL47

PERIPHCTRL47 is peripheral control register 47.

Offset Address	Register Name	Total Reset Value
0x00F0	PERIPHCTRL47	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										sata_test_byp_mode	sata_test_burnin_mode	reserved																	sata_test_pddq	reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RW	sata_test_byp_mode	Indicates whether to enable all input interfaces of the SATA module in the ASIC to connect to the output end by using the combined logic, which increases the coverage rate of the interface test. 0: disabled 1: enabled
[20]	RW	sata_test_burnin_mode	SATA burn-in test mode enable. 0: disabled 1: enabled Note: You are advised to enable as much circuits as possible and use this bit with [sata_test_byp_mode] during the burn-in test.
[19:11]	RO	reserved	Reserved.
[10:3]	RO	reserved	Reserved.
[2]	RW	sata_test_pddq	SATA PHY power control. 0: not powered off 1: powered off
[1:0]	RO	reserved	Reserved.

PERIPHCTRL51

PERIPHCTRL51 is peripheral control register 51.

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Offset Address	Register Name	Total Reset Value
0x0100	PERIPHCTRL51	0xCFCF_CFCF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgmii_txckout_sl		rgmii_txckout_ctl						rgmii_txd_sl		rgmii_txd_ctl						rgmii_txen_sl		rgmii_txen_ctl						vo1120_clk_sl		vo1120_clk_ctl					
Reset	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1

Bits	Access	Name	Description
[31:30]	RW	rgmii_txckout_sl	Slew rate control for RGMII_TXCLKOUT I/O. 00: low slew rate 01: medium slew rate 10: high slew rate 11: very high slew rate
[29:24]	RW	rgmii_txckout_ctl	Drive capability of RGMII_TXCLKOUT I/O. 0x01: 3 mA 0x03: 6 mA 0x07: 9 mA 0x0F: 12 mA 0x1F: 15 mA 0x3F: 18 mA
[23:22]	RW	rgmii_txd_sl	Slew rate control for RGMII_TXD0/1/2/3 I/O. 00: low slew rate 01: medium slew rate 10: high slew rate 11: very high slew rate
[21:16]	RW	rgmii_txd_ctl	Drive capability of RGMII_TXD0/1/2/3 I/O. 0x01: 3 mA 0x03: 6 mA 0x07: 9 mA 0x0F: 12 mA 0x1F: 15 mA 0x3F: 18 mA

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[15:14]	RW	rgmii_txen_sl	Slew rate control for RGMII_TXEN I/O. 00: low slew rate 01: medium slew rate 10: high slew rate 11: very high slew rate
[13:8]	RW	rgmii_txen_ctl	Drive capability of RGMII_TXEN I/O. 0x01: 3 mA 0x03: 6 mA 0x07: 9 mA 0x0F: 12 mA 0x1F: 15 mA 0x3F: 18 mA
[7:6]	RW	vo1120_clk_sl	Slew rate control for VO1120_CLK I/O. 00: low slew rate 01: medium slew rate 10: high slew rate 11: very high slew rate
[5:0]	RW	vo1120_clk_ctl	Drive capability of VO1120_CLK I/O. 0x01: 3 mA 0x03: 6 mA 0x07: 9 mA 0x0F: 12 mA 0x1F: 15 mA 0x3F: 18 mA

PERIPHCTRL52

PERIPHCTRL52 is peripheral control register 52.

Offset Address	Register Name	Total Reset Value
0x0104	PERIPHCTRL52	0xCFCF_CFCF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	Reserved				mdio_txd_sl	mdio_txd_ctl	mdck_txen_sl	mdck_txen_ctl

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Reset	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:14]	RW	mdio_txd_sl	Slew rate control for MDIO I/O. 00: low slew rate 01: medium slew rate 10: high slew rate 11: very high slew rate
[13:8]	RW	mdio_txd_ctl	Drive capability of MDIO I/O. 0x01: 3 mA 0x03: 6 mA 0x07: 9 mA 0x0F: 12 mA 0x1F: 15 mA 0x3F: 18 mA
[7:6]	RW	mdck_txen_sl	Slew rate control for MDCK I/O. 00: low slew rate 01: medium slew rate 10: high slew rate 11: very high slew rate
[5:0]	RW	mdck_txen_ctl	Drive capability of MDCK I/O. 0x01: 3 mA 0x03: 6 mA 0x07: 9 mA 0x0F: 12 mA 0x1F: 15 mA 0x3F: 18 mA

SCSYSID0

SCSYSID0 is chip ID register 0.

Offset Address	Register Name	Total Reset Value
0xEE0	SCSYSID0	0x00

Bit	7	6	5	4	3	2	1	0
Name	sysid0							

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Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	sysid0	Reading this register returns 0x00.

SCSYSID1

SCSYSID1 is chip ID register 1.

Offset Address	Register Name	Total Reset Value
0xEE4	SCSYSID1	0x01

Bit	7	6	5	4	3	2	1	0
Name	sysid1							
Reset	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[7:0]	RO	sysid1	Reading this register returns 0x01.

SCSYSID2

SCSYSID2 is chip ID register 2.

Offset Address	Register Name	Total Reset Value
0xEE8	SCSYSID2	0x21

Bit	7	6	5	4	3	2	1	0
Name	sysid2							
Reset	0	0	1	0	0	0	0	1

Bits	Access	Name	Description
[7:0]	RO	sysid2	Reading this register returns 0x21.

SCSYSID3

SCSYSID3 is chip ID register 3.

Offset Address	Register Name	Total Reset Value
0xEEC	SCSYSID3	0x35

Bit	7	6	5	4	3	2	1	0
Name	sysid3							

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Reset	0	0	1	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RO	sysid3	Reading this register returns 0x35.

3.5 DMA Controller

3.5.1 Overview

DMA refers to an operating mode in which data is transferred by the hardware by means of input/output (I/O) exchange. In this mode, the DMAC directly transfers data between a memory and a peripheral, between peripherals, and between memories. This avoids the processor intervention and reduces the interrupt processing overhead of the processor. The DMA mode is usually used to transmit data blocks at high speed. After receiving a DMA request, the DMAC enables the master bus controller through the channel configured by the CPU and transmits the address and control signals to the memory and peripherals. The DMAC also counts the transmitted data and reports the status (that is, whether the data transfer is complete or an error occurs in the data transfer) of data transfer to the CPU as an interrupt.

3.5.2 Features

The DMAC has the following features:

- Transfers data in 8-bit, 16-bit, or 32-bit mode.
- Provides eight DMA channels. Each channel can be configured to support unidirectional transfer.
- Provides eight fixed DMA channel priorities. DMA channel 0 has the highest priority; whereas channel 7 has the lowest priority. When the DMA requests from two peripherals are valid simultaneously, the channel with the higher priority starts data transfer first.
- Provides one 4x32-bit FIFO in each of DMAC channels 0 to 5 and one 16 x 32-bit FIFO in each of DMAC channels 6 and 7.
- Provides two 32-bit master bus interfaces for data transfer.
- Supports two types of DMA requests: single transfer request and burst transfer request.
- Provides 16 groups of DMA request inputs. These requests can be configured as source requests or destination requests.
- Supports the DMA requests controlled through software.
- Programs the DMA burst size.
- Configures the source address and the destination address as automatic incremental or decremental addresses during DMA transfer.
- Supports four data transfer directions:
  - Memory to peripheral
  - Memory to memory
  - Peripheral to memory
  - Peripheral to peripheral

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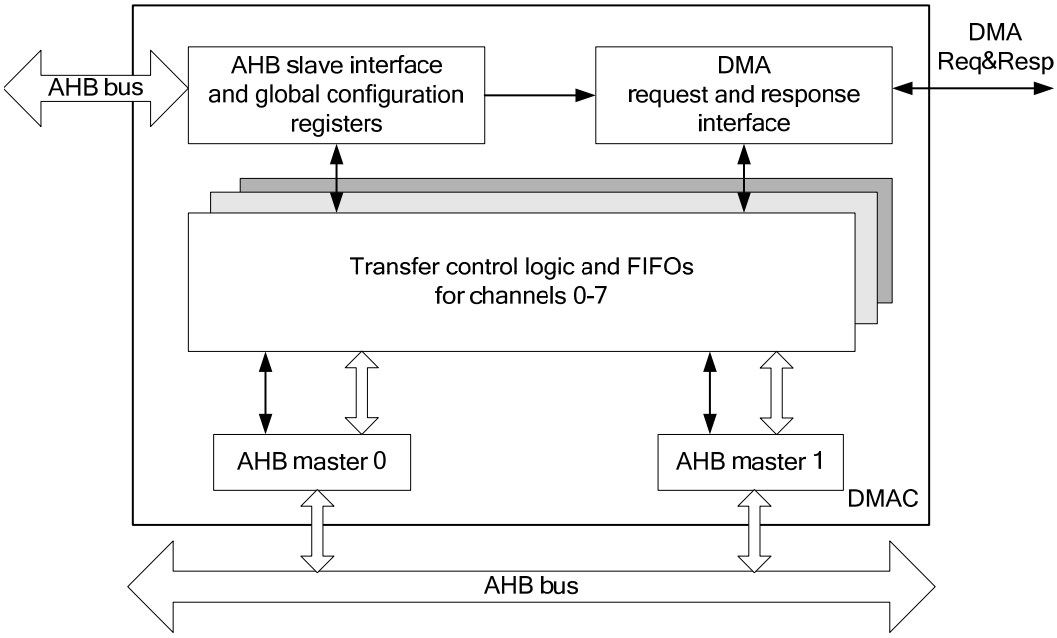
- Supports DMA transfer with the linked list.
- Supports the DMAC flow control.
- Provides a maskable interrupt output and supports the query of the statuses of the raw/masked DMA error interrupt and DMA terminal count interrupt and the status of the combination of the two interrupts.
- Controls the power consumption by disabling the DMAC and supports DMAC clock gating.

3.5.3 Function Description

Functional Block Diagram

Figure 3-5 shows the functional block diagram of the DMAC.

Figure 3-5 Functional block diagram of the DMAC



Each DMAC channel involves a group of transfer control logics and one FIFO. This group of transfer control logics perform the following operations automatically:

Step 1 Read data from the source address specified by the software.

Step 2 Buffer the data to the FIFO.

Step 3 Fetch data from the FIFO.

Step 4 Write the data to the destination address specified by the software.

---End

Workflow

The workflow of the DMAC is as follows:

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Step 1 The software selects one DMAC channel for DMA transfer, configures the following items, and enables the channel:

- Source address
- Destination address
- Head pointer of the linked list
- Amount of the transferred data
- Number of source and destination peripheral request signals
- Masters used at the source and destination ends of the channel.

After the channel is enabled, the DMAC starts to check the activities of the DMA request signals from the source peripheral and destination device connected to this channel.

Step 2 The source device transmits a DMA request to the DMAC. If the source device is a memory, the DMAC considers that the DMA request is always valid by default.

Step 3 The DMAC channel responds to the DMA request of the source device. Then, the DMAC reads data from the source device and stores it in the internal FIFO of the channel.

Step 4 The destination device transmits a DMA request to the DMAC. If the destination device is a memory, the DMAC considers that the DMA request is always valid by default.

Step 5 The DMAC channel responds to the DMA request of the destination device. Then, the DMAC fetches data from the internal FIFO of the channel and writes it to the destination device.

Step 6 The steps Step 2 and Step 3 and steps Step 4 and Step 5 may be performed concurrently, because the source and destination devices may transmit DMA requests to the DMAC at the same time. When the FIFO overrun or underrun occurs on the DMA channel, the DMAC blocks the DMA requests of the source device or destination device until the FIFO is full or empty. When the DMAC interacts with the source device and destination device for several times, Step 2 to Step 5 are performed repeatedly until the specified data is transferred and a maskable terminal count interrupt is sent. If the value of DMAC_CnLLI is not 0, read linked list item (LLI) nodes by considering the register value as an address, load the obtained values to DMAC_Cn_SRC_ADDR, DMAC_Cn_DEST_ADDR, DMAC_CnLLI, and DMAC_Cn_CONTROL in sequence (see Figure 3-6), and go to Step 2. If the value of DMAC_CnLLI is 0, the current DMA transfer is stopped. In this case, the channel is disabled automatically and the transfer ends.

---End

Figure 3-6 shows how to update channel registers by using LLIs.

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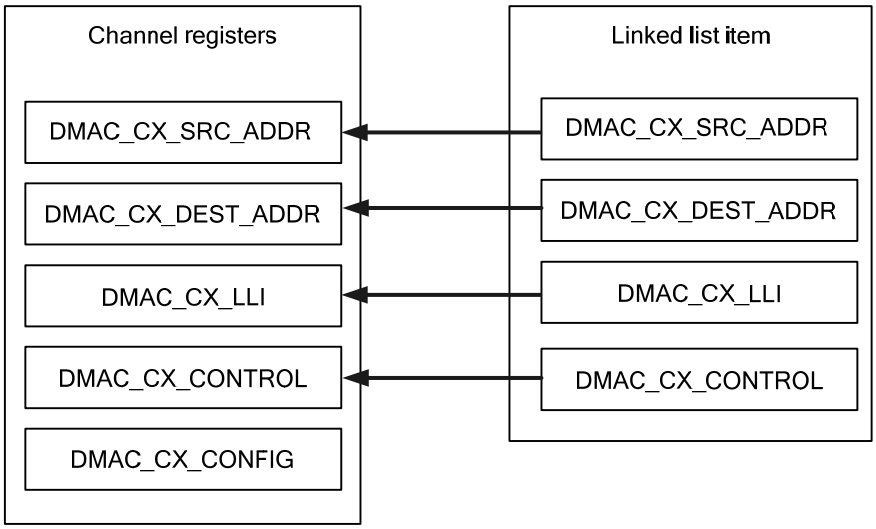
Figure 3-6 Updating channel registers by using the LLIs



Connections Between the DMAC and Peripherals

The peripherals initiate data transfer by transmitting DMA request signals to the DMAC.

The DMAC provides two types of DMA request signals for each peripheral:

- DMACBREQ

  Burst transfer request signal. It triggers a burst transfer and the burst size is preset.
- DMACSREQ

  Single transfer request signal. It triggers a single transfer. That is, the DMAC reads a data segment from a peripheral or writes a data segment to a peripheral.

The DMAC also provides a request clear signal DMACLR.

This signal is sent to each peripheral by the DMAC and is used to respond to the DMA request signal of each peripheral.

DMAC Request Signals

Table 3-28 describes the DMAC hardware request signals and corresponding peripheral requests.

Table 3-28 DMAC hardware request signals and corresponding peripheral requests

DMAC Hardware Request Signal No.	Peripheral Request
0	SIO0 receive (RX) channel
1	SIO1 receive (RX) channel
2	SIO2 receive (RX) channel
3	SIO2 transmit (TX) channel
4	SIO3 TX channel

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DMAC Hardware Request Signal No.	Peripheral Request
5	Reserved
6	DMA request of the UART0 RX channel
7	DMA request of the UART0 TX channel
8	DMA request of the UART1 RX channel
9	DMA request of the UART1 TX channel
10	DMA request of the UART2 RX channel
11	DMA request of the UART2 TX channel
12	DMA request of the UART3 RX channel
13	DMA request of the UART3 TX channel
14	DMA request of the SSP RX channel
15	DMA request of the SSP TX channel

The source and destination requests of each DMA channel are configured by using the software. For example, DMA request 0 is the request of the receive channel of SIO0. To transmit the received data of SIO0 using channel 3, you must configure DMA request 0 as the source request of channel 3.

As memories do not provide DMA request signals, when a memory is used for DMA transfer, the DMAC considers that the DMA request of the memory is always valid by default. In addition, an idle cycle is inserted after each bus operation during the DMAC transfer on channel 6 or channel 7. In this way, the Master with a higher priority channel can transfer data on the bus first. Therefore, to avoid other channels waiting for the bus for a long time, it is recommended to transmit data from memory to memory using channel 6 or channel 7.

The data structure of a DMAC LLI node is as follows:

- Channel register DMAC_Cn_SRC_ADDR, for setting the start address of the source device
- Channel register DMAC_Cn_DEST_ADDR, for setting the start address of the destination device
- Channel register DMAC_CnLLI, for setting the address of the next node
- Channel register DMAC_Cn_CONTROL, forsetting the master, data width, burst size, address increment, and transfer size of the source device and destination device

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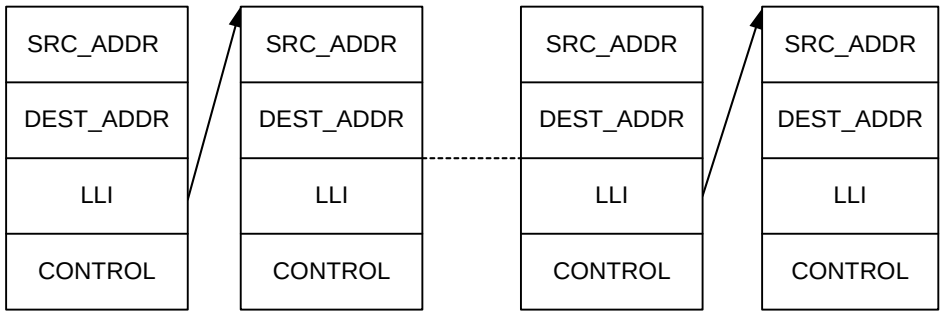
Figure 3-7 Structure of DMAC LLIs



CAUTION

The value of the LLI field must be less than or equal to 0xFFFF_FFF0. Otherwise, the address is wrapped around to 0x0000_0000 during a 4-word burst transfer. As a result, the data structure of LLI nodes cannot be stored in a continuous address area.

If the LLI field is set to 0, the current node is at the end of the linked list. In this case, the corresponding channel is disabled after the corresponding data blocks of the current node are transferred.

3.5.4 Operating Mode

Clock Gating

In the following cases, the DMAC and DMAC clock can be disabled using the software to reduce power consumption:

- All DMAC channels are idle and there is no DMA transfer request.\
- DMAC_Cn_CONFIG [e] is set to 0 and DMAC channels are disabled.

To disable the DMAC clock, perform the following steps:

Step 1 Write 0 to DMAC_Cn_CONFIG [e] to disable DMAC channels.

Step 2 Write 0 to DMAC_CONFIG[e] to disable the DMAC.

Step 3 Write 0 to PERI_CRG56[dma_cken] to disable the bus clock gating function of the DMAC and disable the DMAC clock.

Step 4 Enable the clock and the DMAC again when the DMAC is required for data transfer.

---End

Initializing the DMAC

To initialize the DMAC, perform the following steps:

Step 1 Write to DMAC_CONFIG to set the endian mode of DMAC master 1 and DMAC master 2, and write 1 to DMAC_CONFIG[e] to enable the DMAC.

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Step 2 Write 1 to all the bits of DMAC_INT_ERR_CLR and DMAC_INT_TC_CLR to clear all interrupt statuses.

Step 3 Write 0 to the corresponding bits of DMAC_SYNC to set the DMA request signal groups to be synchronized.

Step 4 Configure and disable each channel in sequence. You can disable all the channels by writing 0 to DMAC_Cn_CONFIG [e] of each channel.

---End

Enabling a Channel

After the DMAC is initialized, the DMAC can transfer data only when a DMAC channel is configured and enabled. To enable a DMA channel, perform the following steps:

Step 1 Read DMAC_ENBLD_CHNS to search for free channels and select one.

Step 2 Write 1 to the corresponding bits of DMAC_INT_ERR_CLR and DMAC_INT_TC_CLR to clear the interrupt status of the selected channel.

Step 3 Configure and enable the selected channel as follows:

1. Write to DMAC_Cn_SRC_ADDR to set the access start address of the source device.
2. Write to DMAC_Cn_DEST_ADDR to set the access start address of the destination device.
3. For single-block data transfer, write 0 to DMAC_CnLLI.
4. For LLI data transfer, configure DMAC_CnLLI as the LLI header pointer.
5. Write to DMAC_Cn_CONTROL to set the master, data width, burst size, address increment, and transfer size of the source device and destination device.
6. Write to DMAC_Cn_CONFIG to set the DMA request signal, flow control mode, and interrupt mask of this channel. At this time, write 0 to DMAC_CX_CONFIG[e]. Then this channel is not enabled currently.
7. Write to DMAC_Cn_CONFIG to enable this channel. **Note:** Set the Channel Enable bit to 1 and keep other bits unchanged.

---End

Using DMAC_Cn_CONTROL

This register contains the control information about the DMA channels, such as the transfer size, burst size, and transfer bit width.

Before a channel is enabled, its corresponding register must be programmed using software. After the channel is enabled, the value of the register is updated when being loaded from the LLI node after a complete data block is transferred.

When a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. After the channel stops data transfer, the register can be read.

Table 3-29 describes the mapping between the value of DBSize or SBSize of DMAC_Cn_CONTROL and burst length.

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Table 3-29 Mapping between the value of DBSize or SBSize and burst length

DBSize or SBSize	Burst Length
000	1
001	4
010	8
011	16
100	32
101	64
110	128
111	256

Table 3-30 describes the value of DWidth or SWidth of DMAC_Cn_CONTROL and transfer data width.

Table 3-30 Mapping between the value of DWidth or SWidth and transfer bit width

SWidth or DWidth	Transfer Bit Width
000	Byte (8 bits)
001	Half word (16 bits)
010	Word (32 bits)
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Reserved

Note the following points when configuring DMAC_Cn_CONTROL:

- When the transfer bit width of the source device is smaller than that of the destination device, the product of the transfer bit width and transfer size of the source device must be an integral multiple of the transfer bit width of the destination device. Otherwise, data retention and data loss occur in the FIFO.
- SWidth and DWidth fields cannot be set to undefined bit widths.
- If the transfer size field is set to 0 and the DMAC is a flow controller, the DMAC does not transfer data. In this case, the programmer needs to disable the DMA channel and reprogram it.
- Do not perform common write/read tests on the DMAC_Cn_CONTROL register, because the transfer size field is different from the common register field whose written value and read value may be the same. During writes, this field serves as a control

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register, because it determines the number of data segments transferred by the DMAC. During reads, this field serves as a status register, because it returns the number (in the unit of the bit width of the source device) of the remaining data segments to be transferred.

- When the transfer size field is set to a value greater than the depth of the FIFO (peripheral FIFO rather than the DMAC FIFO) of the source device or destination device, the mode of DMAC source address or destination address must be set to non-increment mode. Otherwise, the peripheral FIFO may overflow.

The bus access information is provided for the source device or destination device over the master interface signals during data transfer. Such information is related to the bits DMAC_Cn_CONTROL[prot] and DMAC_Cn_CONFIG[Lock] set by programming channel registers. Table 3-31 describes the three protection bits of the prot field of DMAC_Cn_CONTROL.

Table 3-31 Definitions of the prot field of DMAC_Cn_CONTROL

Bits	Description	Purpose
[2]	Cacheable or noncacheable	Indicates whether the access is cacheable. 0: noncacheable 1: cacheable For example, this bit can notify an advanced microcontroller bus architecture (AMBA) bridge of the following information: When finding the first burst read operation with eight digits, this bridge can initiate one 8-digit burst read operation on the destination bus directly without transmitting the read operations on the source bus to the destination bus one by one. This bit controls the output of the bus signal HPROT[3].
[1]	Bufferable or nonbufferable	Indicates whether the access is bufferable. 0: nonbufferable 1: bufferable For example, this bit is used to notify an AMBA bridge that the write operation on the source bus can be complete without waiting. That is, the operation can be performed even when the bridge does not arbitrate the operation to the destination bus and the slave device does not receive data completely. This bit controls the output of the bus signal HPROT[2].
[0]	Privileged or user	Access mode. 0: user mode 1: privileged mode This bit controls the output of the bus signal HPROT[1].

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Using DMAC_Cn_CONFIG

Table 3-32 describes the flow controllers and transfer types corresponding to the flow_cntrl field of DMAC_Cn_CONFIG.

Table 3-32 Flow controllers and transfer types corresponding to the flow_cntrl field

Bit Value	Transfer Mode	Controller
000	Memory to memory	DMAC
001	Memory to peripheral	DMAC
010	Peripheral to memory	DMAC
011	Source device to destination device	DMAC
100	Source device to destination device	Destination device
101	Memory to peripheral	Destination device
110	Peripheral to memory	Source device
111	Source device to destination device	Source device

Processing an Interrupt

When data transfer is complete or an error occurs during data transfer, interrupts are reported to the interrupt controller. An interrupt is processed as follows:

Step 1 Read DMAC_INT_STAT to find the channel that transmits an interrupt request. When multiple channels transmit interrupt requests at the same time, the interrupt request with the highest priority is processed first.

Step 2 Read DMAC_INT_TC_STAT to query the value of the selected bit to check whether the interrupt sent by the corresponding channel is a terminal count interrupt. If the value is 1, the interrupt is a terminal count interrupt. In this case, go to Step 4; otherwise, go to Step 3.

Step 3 Read DMAC_INT_ERR_STAT to query the value of the selected bit to check whether the interrupt sent by the corresponding channel is an error interrupt. If the selected bit is 1, the interrupt is an error interrupt. In this case, go to Step 5; otherwise, end the operation.

Step 4 Process the terminal count interrupt as follows:

1. Write 1 to the selected bit of DMAC_INT_TC_CLR to clear the interrupt status of the corresponding channel.
2. Fetch or use up the data buffered in the memory. If necessary (such as creating a buffer in the memory), configure and enable the channel again.
3. End the operation.

Step 5 Process the error interrupt as follows:

1. Write 1 to the selected bit of DMAC_INT_ERR_CLR to clear the interrupt status of the corresponding channel.

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2. Provide the error information. If necessary, configure and enable the channel again.
3. End the operation.

---End

3.5.5 Register Summary

Table 3-33 describes DMAC registers.

Table 3-33 Summary of the DMAC registers (base address: 0x100D_0000)

Offset Address	Register	Function Description	Page
0x000	DMAC_INT_STAT	DMAC interrupt status register	3-131
0x004	DMAC_INT_TC_STAT	DMAC terminal count interrupt status register	3-131
0x008	DMAC_INT_TC_CLR	DMAC terminal count interrupt clear register	3-132
0x00C	DMAC_INT_ERR_STAT	DMAC error interrupt status register	3-132
0x010	DMAC_INT_ERR_CLR	DMAC error interrupt clear register	3-133
0x014	DMAC_RAW_INT_TC_STAT	DMAC raw terminal count interrupt status register	3-133
0x018	DMAC_RAW_INT_ERR_STAT	DMAC raw error interrupt status register	3-134
0x01C	DMAC_ENBLD_CHNS	DMAC channel enable status register	3-134
0x020	DMAC_SOFT_BREQ	DMA burst request register for software	3-135
0x024	DMAC_SOFT_SREQ	DMA single request register for software	3-135
0x028	DMAC_SOFT_LBREQ	DMA last burst request register for software	3-136
0x02C	DMAC_SOFT_LSREQ	DMA last single request register for software	3-137
0x030	DMAC_CONFIG	DMAC configuration register	3-137
0x034	DMAC_SYNC	DMAC request synchronization register	3-138
0x100+n x 0x20	DMAC_Cn_SRC_ADDR	DMAC source address register	3-138

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Offset Address	Register	Function Description	Page
0x104+n x 0x20	DMAC_Cn_DEST_ADDR	DMAC destination address register	3-139
0x108+n x 0x20	DMAC_Cn_LLI	DMAC LLI register	3-140
0x10C+n x 0x20	DMAC_Cn_CONTROL	DMAC control register	3-140
0x110+n x 0x20	DMAC_Cn_CONFIG	DMAC configuration register	3-143

3.5.6 Register Description

DMAC_INT_STAT

DMAC_INT_STAT is an interrupt status register. It shows the status of the masked interrupts. If certain bits of DMAC_INT_TC_STAT and DMAC_INT_ERR_STAT are masked at the same time, the corresponding bit of DMAC_INT_STAT1 is also masked. Each bit of DMAC_INT_STAT maps to one DMAC channel. When a bit is 1, an interrupt request is generated in the corresponding channel and the interrupt request may be an error interrupt or a terminal count interrupt.

Offset Address	Register Name	Total Reset Value
0x000	DMAC_INT_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								int_stat							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	RO	int_stat	Statuses of the masked interrupts of each DMA channel. Bit[7:0] map to channels 7–0. 0: No interrupt is generated. 1: An interrupt is generated. The interrupt request may be an error interrupt or a terminal count interrupt.

DMAC_INT_TC_STAT

DMAC_INT_TC_STAT is an terminal count interrupt status register. It shows the status of the masked terminal count interrupts. The corresponding mask bit is DMAC_Cn_CONFIG[itc], where n is the channel number ranging from 0 to 7. This register must work with DMAC_INT_STAT.

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Offset Address	Register Name	Total Reset Value
0x004	DMAC_INT_TC_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								int_tc_stat							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	RO	int_tc_stat	Statuses of the masked terminal count interrupts. Bit[7:0] map to channels 7–0. 0: No terminal count interrupt is generated. 1: A terminal count interrupt is generated.

DMAC_INT_TC_CLR

DMAC_INT_TC_CLR is a terminal count interrupt clear register. It is used to clear terminal count interrupts.

Offset Address	Register Name	Total Reset Value
0x008	DMAC_INT_TC_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								int_tc_clr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	WO	int_tc_clr	Terminal count interrupt clear. Bit[7:0] map to channels 7–0. 0: do not clear 1: clear

DMAC_INT_ERR_STAT

DMAC_INT_ERR_STAT is an error interrupt status register. It shows the status of the masked error interrupts. The corresponding mask bit is DMAC_Cn_CONFIG [ie]. The register must work with DMAC_INT_STAT.

Offset Address	Register Name	Total Reset Value
0x00C	DMAC_INT_ERR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								int_err_stat							

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	RO	int_err_stat	Statuses of masked error interrupts. Bit[7:0] map to channels 7–0. 0: No error interrupt is generated. 1: An error interrupt is generated.

DMAC_INT_ERR_CLR

DMAC_INT_ERR_CLR is an error interrupt clear register. It is used to clear error interrupts.

Offset Address	Register Name	Total Reset Value
0x010	DMAC_INT_ERR_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								int_err_clr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	WO	int_err_clr	Error interrupt clear. Bit[7:0] map to channels 7–0. 0: do not clear 1: clear

DMAC_RAW_INT_TC_STATUS

DMAC_RAW_INT_TC_STATUS is a raw terminal count interrupt status register. It shows the status of the raw terminal count interrupt of each channel.

Offset Address	Register Name	Total Reset Value
0x014	DMAC_RAW_INT_TC_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								raw_int_tc_stat							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.

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[7:0]	RO	raw_int_tc_stat	Statuses of the raw terminal count interrupt of each channel. Bit[7:0] map to channels 7–0. 0: No terminal count interrupt is generated. 1: A terminal count interrupt is generated.

DMAC_RAW_INT_ERR_STATUS

DMAC_RAW_INT_ERR_STATUS is a raw error interrupt status register. It shows the status of the raw error interrupt of each channel.

Offset Address	Register Name	Total Reset Value
0x018	DMAC_RAW_INT_ERR_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								raw_int_err_stat							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	RO	raw_int_err_stat	Statuses of the raw error interrupt of each channel. Bit[7:0] map to channels 7–0. 0: No error interrupt is generated. 1: An error interrupt is generated.

DMAC_ENBLD_CHNS

DMAC_ENBLD_CHNS is a DMAC channel enable status register. It shows the enabled channels.

For example, if a bit of DMAC_ENBLD_CHNS is 1, the corresponding channel is enabled. The enable bit of DMAC_Cn_CONFIG of each channel determines whether the corresponding channel is enabled. When the DMA transfer over a channel is complete, the bit of DMAC_ENBLD_CHNS corresponding to the channel is cleared.

Offset Address	Register Name	Total Reset Value
0x01C	DMAC_ENBLD_CHNS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								enabled_channels							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.

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[7:0]	RO	enabled_channels	Channel enable. Bit[7:0] map to channels 7–0. 0: disabled 1: enabled

DMAC_SOFT_BREQ

DMAC_SOFT_BREQ is a DMA burst request register for software. It is used to control whether to generate a DMA burst request using software.

When this register is read, the device that is requesting the DMA burst transfer can be queried. This register and any peripheral each can generate a DAM request.

NOTE

It is not recommended to generate a software DMA request and a hardware DMA request at the same time.

Offset Address	Register Name	Total Reset Value
0x020	DMAC_SOFT_BREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_breq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	soft_breq	Controls whether to generate a DMA burst transfer request. For details about the request corresponding to each bit, see Table 3-28. When this register is written: 0: no effect 1: A DMA burst transfer request is generated. When the transfer is complete, the corresponding bit is cleared. When this register is read: 0: The peripheral corresponding to the request signal DMACBREQ[15:0] does not transmit a DMA burst request. 1: The peripheral corresponding to the request signal DMACBREQ[15:0] is requesting a DMA burst transfer.

DMAC_SOFT_SREQ

DMAC_SOFT_SREQ is a DMA single request register for software. It is used to control whether to generate a DMA single transfer request using software.

When this register is read, the device that is requesting the DMA single transfer can be queried. This register and any of the 16 DMA request input signals of the DMAC each can generate a DMA request.

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NOTE

It is not recommended to generate a software DMA request and a hardware DMA request at the same time.

Offset Address	Register Name	Total Reset Value
0x024	DMAC_SOFT_SREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_sreq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	soft_sreq	Controls whether to generate a DMA burst transfer request. For details about the request corresponding to each bit, see Table 3-28. When this register is written: 0: no effect 1: A DMA single transfer request is generated. When the transfer is complete, the corresponding bit is cleared. When this register is read: 0: The peripheral corresponding to the request signal DMACBREQ[15:0] does not transmit a DMA single request. 1: The peripheral corresponding to the request signal DMACBREQ[15:0] is requesting a DMA single transfer.

DMAC_SOFT_LBREQ

DMAC_SOFT_LBREQ is a DMA last burst request register for software. It is used to control whether to generate a DMA last burst transfer request using software.

Offset Address	Register Name	Total Reset Value
0x028	DMAC_SOFT_LBREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_lbreq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	WO	soft_lbreq	Last burst request issued by the software. 0: no effect 1: A DMA last burst transfer request is generated. When the transfer is complete, the corresponding bit is cleared.

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DMAC_SOFT_LSREQ

DMAC_SOFT_LSREQ is a DMA last single request register for software. It is used to control whether to generate a DMA last single transfer request.

Offset Address	Register Name	Total Reset Value
0x02C	DMAC_SOFT_LSREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_lsreq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	WO	soft_lsreq	Last single transfer request issued by the software. 0: no effect 1: A DMA last single transfer request is generated. When the transfer is complete, the corresponding bit is cleared.

DMAC_CONFIG

DMAC_CONFIG is a DMAC configuration register. It is used to configure DMAC operations. You can change the endian modes of the two master interfaces of the DMAC by writing to m1 (bit[1]) and m2 (bit[2]) of this register. After reset, the modes of the two master interfaces are set to little endian.

NOTE
Both Masters work in little endian mode.

Offset Address	Register Name	Total Reset Value
0x030	DMAC_CONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													m2	m1	e
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved.
[2]	RW	m2	Endian mode of Master 2. 0: little endian mode 1: big endian mode
[1]	RW	m1	Endian mode of Master 1. 0: little endian mode 1: big endian mode

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[0]	RW	e	DMAC enable. 0: disabled 1: enabled

DMAC_SYNC

DMAC_SYNC is a DMAC synchronization register. It is used to enable or disable the synchronization logic provided for DMA request signals.

Offset Address	Register Name	Total Reset Value
0x034	DMAC_SYNC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dmac_sync															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	dmac_sync	Controls whether to synchronize the request signals. For details about the request corresponding to each bit, see Table 3-28. 0: enable the synchronization logic provided for the DMA request signals of the corresponding peripheral. 1: disable the synchronization logic provided for the DMA request signals of the corresponding peripheral.

NOTE

It is recommended that you disable the synchronization logics for all request signals.

DMAC_Cn_SRC_ADDR

DMAC_Cn_SRC_ADDR is a DMAC source address register. It shows the source addresses (sorted by byte) of the data to be transferred.

The offset address of the register is 0x100+n x 0x20. The value of n ranges from 0 to 7. The values 0–7 map to DMA channels 0–7.

Before a channel is enabled, its corresponding register must be programmed using software. After the channel is enabled, the register is updated in the following cases:

- The source address is incremented.
- A complete data block is transferred and then loaded from LLI nodes.

When a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel stops data transfer. At this time, the read value is the last source address read by the DMAC.

The source and destination addresses must be aligned with the transfer widths of the source and destination devices.

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Offset Address	Register Name	Total Reset Value
0x100 + n x 0x20	DMAC_Cn_SRC_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	src_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	src_addr	DMA source address.

The DMAC provides eight channels. Each channel has the following five channel registers:

- DMAC_Cn_SRC_ADDR
- DMAC_Cn_DEST_ADDR
- DMAC_CnLLI
- DMAC_Cn_CONTROL
- DMAC_Cn_CONFIG

When the DMA loads LLI nodes from a memory, the DMAC updates the preceding registers except DMAC_CX_CONFIG automatically.

CAUTION

During DMA transfer, the DMAC may perform unexpected operations when the preceding channel registers are updated. Before changing the settings of a channel, you must disable the channel and then configure its relevant registers.

DMAC_Cn_DEST_ADDR

DMAC_Cn_DEST_ADDR is a destination address register. Its offset address is 0x104 + n x 0x20. The value of X ranges from 0 to 7. The values 0–7 map to DMA channels 0–7.

This register contains the destination address (sorted by byte) of the data to be transferred. Before a channel is enabled, its corresponding register must be programmed using software. After the channel is enabled, the register is updated in the following cases:

- Destination address increment.
- A complete data block is transferred and then loaded from LLI nodes.

When a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel stops data transfer. At this time, the read value is the last destination address written by the DMAC.

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Offset Address	Register Name	Total Reset Value
0x104 + n x 0x20	DMAC_Cn_DEST_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dest_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dest_addr	DMA destination address.

DMAC_CnLLI

DMAC_CnLLI is a DMAC LLI register. Its offset address is 0x108 + n x 0x20. The value of X ranges from 0 to 7. The values 0–7 map to DMA channels 0–7.

Offset Address	Register Name	Total Reset Value
0x108 + n x 0x20	DMAC_CnLLI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lli																														r	lm
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RW	lli	LLI. The bit[31:2] of the next LLI node address and the address bit[1:0] are both set to 0. A linked list address must be 4-byte aligned.
[1]	RW	r	Reserved. This bit must be 0 during writes and must be masked during reads.
[0]	RW	lm	Master for loading the next LLI node. 0: Master1 1: Master2

DMAC_Cn_CONTROL

DMAC_Cn_CONTROL is a DMAC channel control register. Its offset address is 0x10C + n x 0x20. The value of X ranges from 0 to 7. The values 0–7 map to DMA channels 0–7.

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Offset Address	Register Name	Total Reset Value
0x10C + n x 0x20	DMAC_Cn_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	i	prot			di	si	d	s	dwidth				swidth				dbsize				sbsize				transfersize							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	i	Terminal count interrupt enable. This bit determines whether the current LLI node triggers a terminal count interrupt. 0: not trigger 1: trigger
[30:28]	RW	prot	HPROT[2:0] access protection signal transmitted by the Master.
[27]	RW	di	Destination address increment. 0: The destination address is not incremented 1: The destination address is incremented once after a data segment is transferred If the destination device is a peripheral, the destination address is not incremented. If the destination device is a memory, the destination address is incremented.
[26]	RW	si	Source address increment. 0: The source address is not incremented 1: The source address is incremented once after a data segment is transferred If the source device is a peripheral, the source address is not incremented. If the source device is a memory, the source address is incremented.
[25]	RW	d	Master for accessing the destination device. 0: The SPDIF, SIO0, SIO1, UART0, UART1, and SCI access the destination device using Master1. 1: The SPI flash, NAND flash, NOR flash, and DDRC access the destination device using Master 2.
[24]	RW	s	Master for accessing the source device. 0: The SPDIF, SIO0, SIO1, UART0, UART1, and SCI access the source device using Master1. 1: The SPI flash, NAND flash, NOR flash, and DDRC access the source device using Master2.

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[23:21]	RW	dwidth	Transfer bit width of the destination device. The transfer bit width is invalid if it is greater than the bit width of the Master. The data widths of the destination and source devices can be different. The hardware automatically packs and unpacks the data. For details about the mapping between the value of DWidth and the bit width, see Table 3-30.
[20:18]	RW	swidth	Transfer bit width of the source device. The transfer bit width is invalid if it is greater than the bit width of the Master. The data widths of the destination and source devices can be different. The hardware automatically packs and unpacks the data. For details about the mapping between the value of SWidth and the bit width, see Table 3-30.
[17:15]	RW	dbsize	Burst size of the destination device. Indicates the number of data segments to be transferred by the destination device in a burst transfer, that is, the number of transferred data segments when DMACCnBREQ is valid. This value must be set to a burst size supported by the destination device. If the destination device is a memory, the value is set to the storage area size beyond the storage address boundary. For details about the mapping between the value of DBSize and the transfer size, see Table 3-29.
[14:12]	RW	sbsize	Burst size of the source device. Indicates the number of data segments to be transferred by the source device in a burst transfer, that is, the number of transferred data segments when DMACCnBREQ is valid. The value must be set to a burst size supported by the source device. If the source device is a memory, the value is set to the storage area size beyond the storage address boundary. For details about the mapping between the value of SBSize and the transfer length, see Table 3-29.
[11:0]	RW	transfersize	The DMA transfer size can be configured by writing to DMAC_Cn_CONTROL only when the DMAC is a flow controller. The transfer size indicates the number of the data segments to be transferred by the source device. When DMAC_Cn_CONTROL is read, the number of data segments transferred through the bus connected to the destination device is obtained. When a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel is enabled and data transfer is stopped.

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DMAC_Cn_CONFIG

DMAC_Cn_CONFIG is a DMAC channel configuration register. Its offset address is 0x110 + n x 0x20. The value of X ranges from 0 to 7. The values 0–7 map to DMA channels 0–7.

This register is not updated when a new LLI node is loaded.

Offset Address	Register Name	Total Reset Value
0x110 + n x 0x20	DMAC_Cn_CONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													h	a	l	itc	ie	flow_cntrl		reserved		dest_peripheral				reserved		src_peripheral			e
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	-	reserved	Reserved. This bit must be 0 during writes and must be masked during reads.
[18]	RW	h	Halt bit. 0: The DMA request is allowed. 1: The subsequent DMA requests are ignored and the contents in the channel FIFO are completely transferred. This bit can disable a DMA channel without data loss by working with the Active bit and the Channel Enable bit.
[17]	RO	a	Active bit. 0: There is no data in the channel FIFO. 1: There is data in the channel FIFO. This bit can disable a DMA channel without data loss by working with the Halt bit and Channel Enable bit.
[16]	RW	l	Lock bit. 0: Disable lock transfer on the bus. 1: Enable lock transfer on the bus.
[15]	RW	itc	Terminal count interrupt mask bit. 0: Mask the terminal count interrupts of the channel. 1: Do not mask the terminal count interrupts of the channel.
[14]	RW	ie	Error interrupt mask bit. 0: Mask the error interrupts of the channel. 1: Do not mask the error interrupts of the channel.

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[13:11]	RW	flow_cntrl	Flow control and transfer type field. This field is used to specify the flow controller and transfer type. The flow controller can be the DMAC, source device, or destination device. The transfer type can be memory to peripheral, peripheral to memory, peripheral to peripheral, or memory to memory. For details, see Table 3-32.
[10]	-	reserved	Reserved. This bit must be 0 during writes and must be masked during reads.
[9:6]	RW	dest_peripheral	Destination device. This field is used to select a peripheral request signal as the request signal of the DMA destination device of the channel. If the destination device for DMA transfer is a memory, this field is ignored.
[5]	-	reserved	Reserved. This bit must be 0 during writes and must be masked during reads.
[4:1]	RW	src_peripheral	Source device. This field is used to select a peripheral request signal as the request signal of the DMA source device of the channel. If the source device for DMA transfer is a memory, this field is ignored.
[0]	RW	e	Channel enable bit. The current status of a channel can be queried by reading this register or DMAC_ENBLD_CHNS. 0: disabled 1: enabled Clearing this bit can disable a channel. When this bit is cleared, the current bus transfer continues until the data transfer is complete. Then, the channel is disabled and the remaining data in the FIFO is lost. When the last LLI is transferred or an error occurs during transfer, the channel is also disabled and this bit is cleared. If you want to disable a channel without data loss, the Halt bit must be set to 1 so the subsequent DMA requests are ignored by the channel. After this, the Active bit must be polled until its value becomes 0. This indicates that there is no data in the channel FIFO. At this time, the Enable bit can be cleared. To enable a channel by setting this bit to 1, you must reinitialize the channel. If a channel is enabled by setting this bit to 1 only, unexpected results may occur. When a channel is disabled by writing to the Channel Enable bit, this bit can be set to 1 again only after the corresponding bit of DMAC_ENBLD_CHNS is polled to be 0. This is because the channel is not disabled immediately after the Channel Enable bit is cleared. The running delay during a bus burst operation also needs to be considered

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3.6 CIPHER

3.6.1 Overview

The CIPHER module supports data encryption and decryption by following the data encryption standard (DES), 3DES, or advanced encryption standard (AES) algorithm. The DES, 3DES, and AES algorithms are implemented according to FIPS46-3 and FIPS 197 standards. The DES/3DES and AES operating modes comply with FIPS-81 and NIST special 800-38a standards.

The CIPHER module can encrypt or decrypt a large amount of data effectively. In addition, it encrypts and decrypts one or more blocks at one time.

3.6.2 Features

The CIPHER module has the following features:

- Supports the AES key length of 128 bits, 192 bit, or 256 bits. If keys are configured by the key management module, the key length can be set only to 128 bits.
- Supports the DES key length of 64 bits. The values for bit 0, bit 8, bit 16, bit 24, bit 32, bit 40, bit 48, and bit 56 represent the parity check values for eight bytes repectively. The parity check values are not used during encryption or decryption.
- Supports 3-key and 2-key modes for the 3DES algorithm. If keys are configured by the key management module, only the 2-key mode is supported.
- Supports the operating modes of electronic codebook (ECB), cipher block chaining (CBC), 1-/8-/128-cipher feedback (CFB), 128-output feedback (OFB), and counter (CTR) for the AES algorithm. These operating modes comply with the NIST special 800-38a standard.
- Supports the operating modes of ECB, CBC, 1-/8-/64-CFB, and 1-/8-/64-OFB for the DES or 3DES algorithm. These operating modes comply with the FIPS-81 standard.
- Encrypts and decrypts one or more blocks at one time in ECB, CBC, CFB, OFB or CTR operating mode.
- Encrypts and decrypts one or more blocks at one time in CTR operating mode using the AES algorithm.
- Provides eight encryption/decryption keys (64 bits, 128 bits, 192 bits, or 256 bits) configured by the CPU.
- Provides eight keys (fixed at 128 bits) configured by the key management module. The master CPU cannot be read and written.
- Provides a single-block encryption/decryption channel and seven multi-block encryption/decryption channels. The single-block encryption/decryption channel can encrypt or decrypt a single block only at one time. In this case, the CPU writes data to the channel register and reads the results. For the multi-block encryption/decryption channel, the logic reads data from the DDR, and writes the encrypted or decrypted data to the DDR automatically.
- Supports weighted round robin policy for each channel. For a single-block channel, the weighted value is 1 by default; for a multi-block channel, the weighted value is configurable.
- Supports the same set of keys or different sets of keys for any channel.
- Keeps the data in the last incomplete block unprocessed when the data of the multi-block channels is not an integral multiple of encryption/decryption blocks.

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- Supports data combination for multi-block channels. To be specific, if the remaining data in a linked list data block is insufficient to form an encryption/decryption block and the data block is not the last one to be processed, the remaining data is combined with the data in the next data block for encryption or decryption. This avoids data stuffing.
- Supports byte address for the multi-block encryption/decryption channel.
- Supports the multi-linked-list structure for the multi-block encryption/decryption channel and supports the combination of data from multiple linked lists. The linked list length is 20 bits. That is, the maximum data amount is 1 MB minus 1.
- Queries the interrupt status and masks and clears interrupts.
- Separately processes and controls interrupts for each channel.
- Supports multi-packet interrupts and aging interrupts.

3.6.3 Function Description

The operating modes of the DES, 3DES, and AES algorithms comply with the FIPS-81 and NIST special 800-38a standards. In the DES, 3DES, and AES algorithms, the ECB, CBC, and CFB operating modes are identical; however, the CTR (for the AES algorithm only) and OFB operating modes are slightly different.

3DES Algorithm

The 3DES algorithm supports both 3-key and 2-key operations. A 2-key operation can be regarded as a simplified 3-key operation. To be specific, key 3 is represented by key 1 in a 2-key operation.

Figure 3-8 shows the 3DES encryption of a 3-key operation and a 2-key operation.

Figure 3-8 3DES encryption of a 3-key operation and a 2-key operation

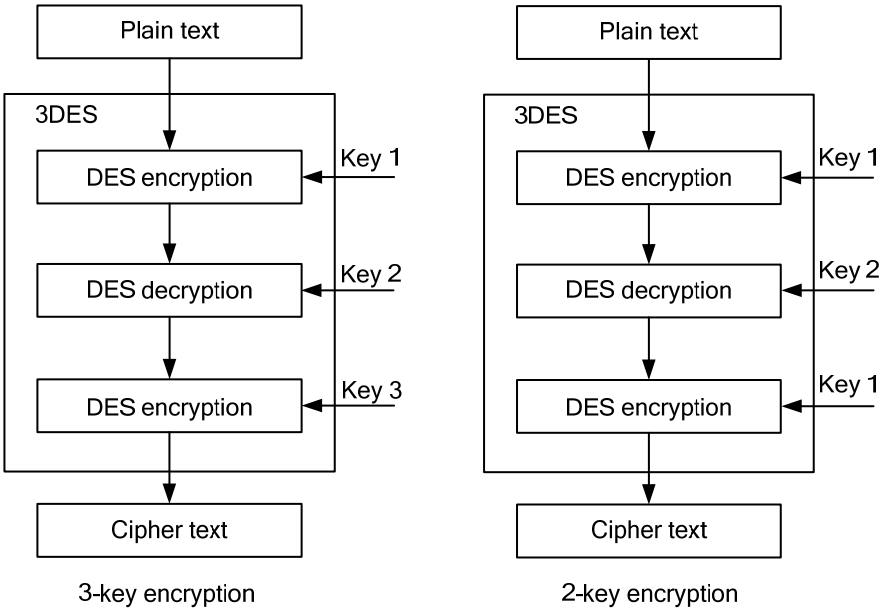

Figure 3-9 shows the 3DES decryption of a 3-key operation and a 2-key operation.

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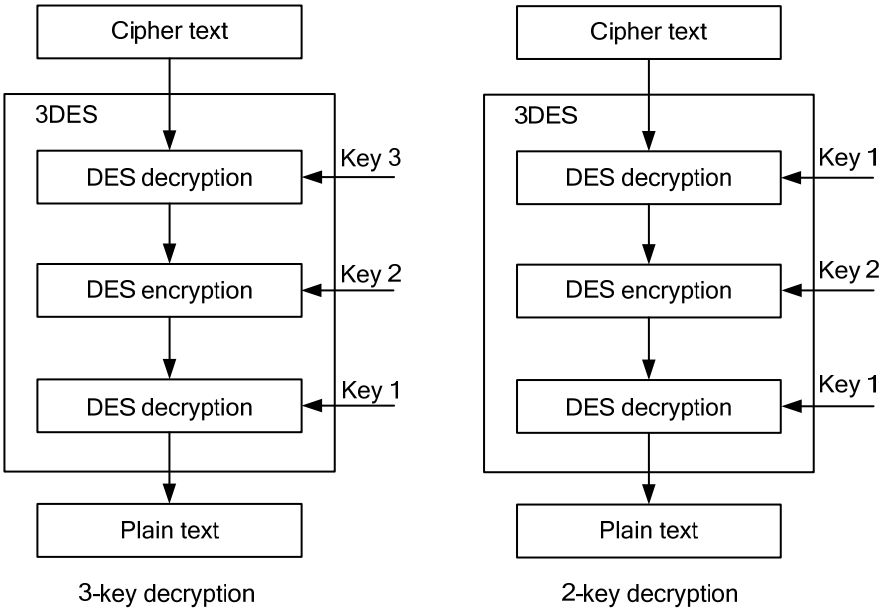
Figure 3-9 3DES decryption of a 3-key operation and a 2-key operation



ECB Mode

In ECB mode, encryption and decryption algorithms are directly applied to the block data. The operation of each block is independent. With this feature, the plain text encryption and cipher text decryption can be performed concurrently. Figure 3-10 shows the ECB mode of the AES and DES algorithms, and Figure 3-11 shows the ECB mode of the 3DES algorithm.

Figure 3-10 ECB mode of the AES and DES algorithms

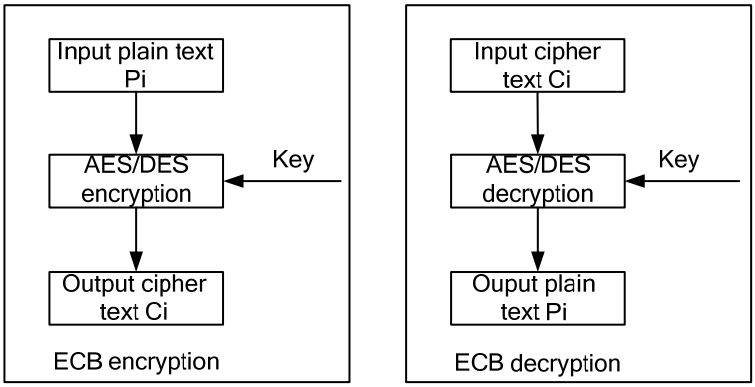


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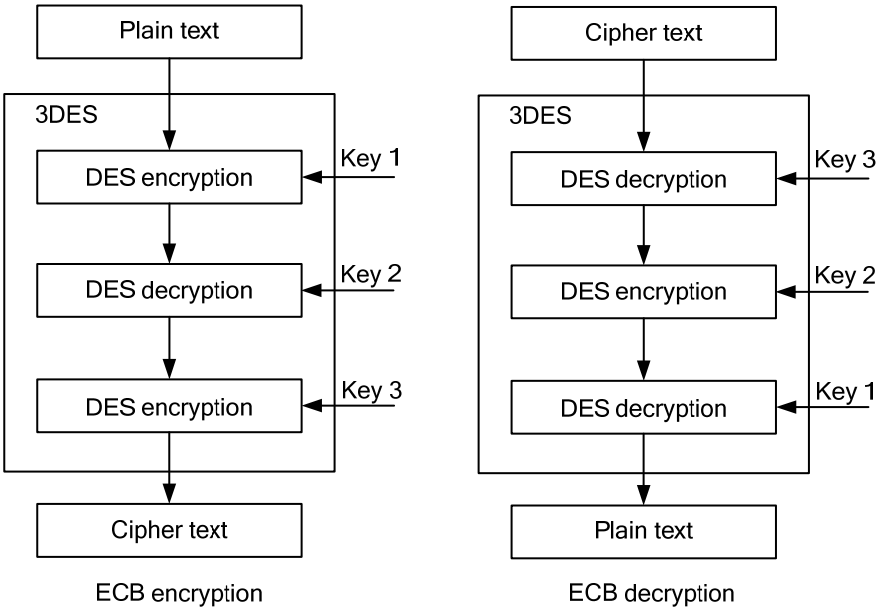
Figure 3-11 ECB mode of the 3DES algorithm



CBC Mode

In CBC mode, the encrypted input plain text block must be exclusive-ORed with the input initialization vector (IV) before being encrypted. The encryption processing of each plain text block is related to the block processing result (cipher text) of the previous plain text. Therefore, encryption operations cannot be concurrently performed in CBC mode. The decryption operation, however, is independent of output plain text of the previous block. Therefore, decryption operations can be performed concurrently. Figure 3-12 shows the CBC mode of the AES and DES algorithms, and Figure 3-13 shows the CBC mode of the 3DES algorithm.

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Figure 3-12 CBC mode of the AES and DES algorithms

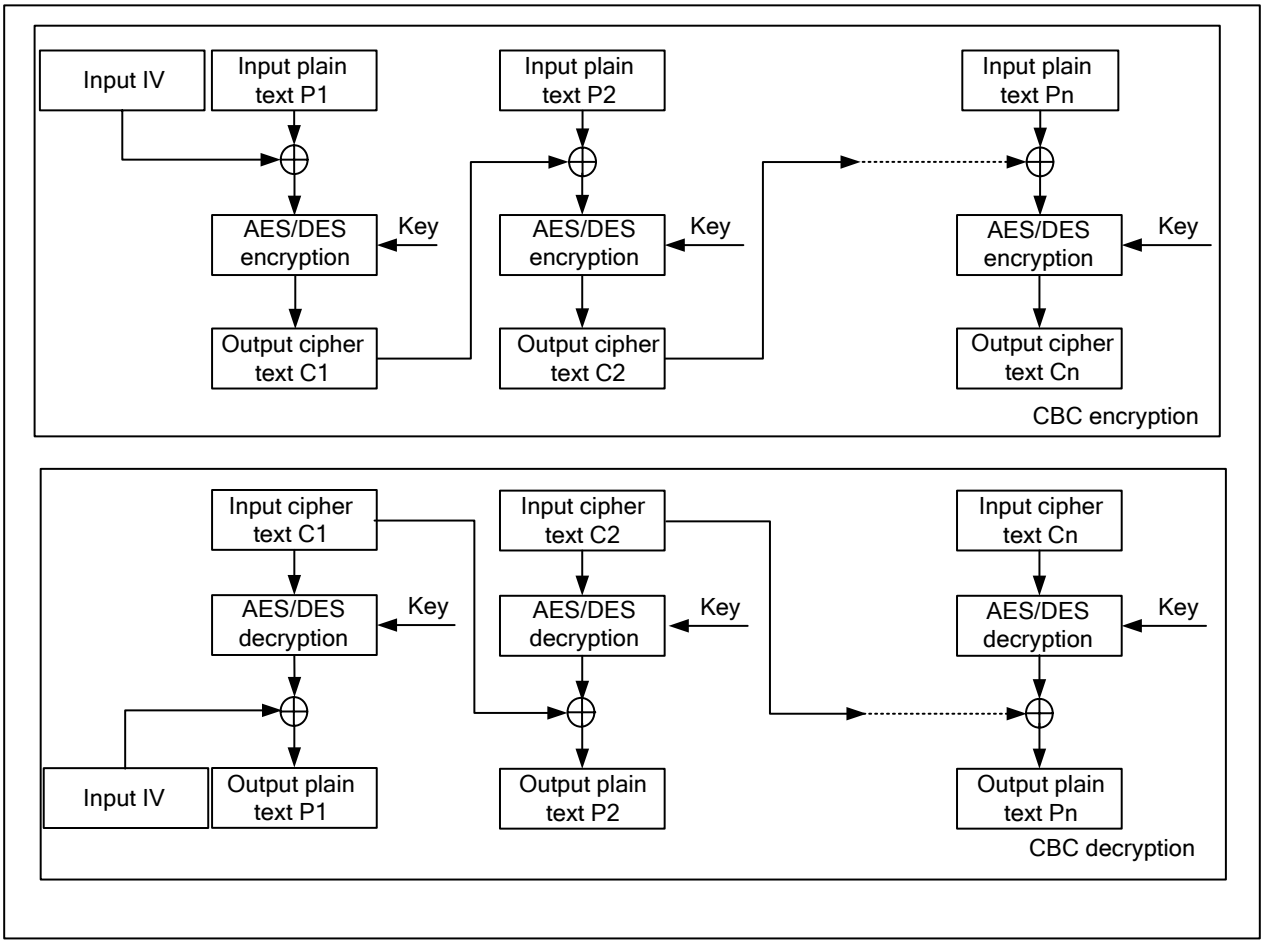

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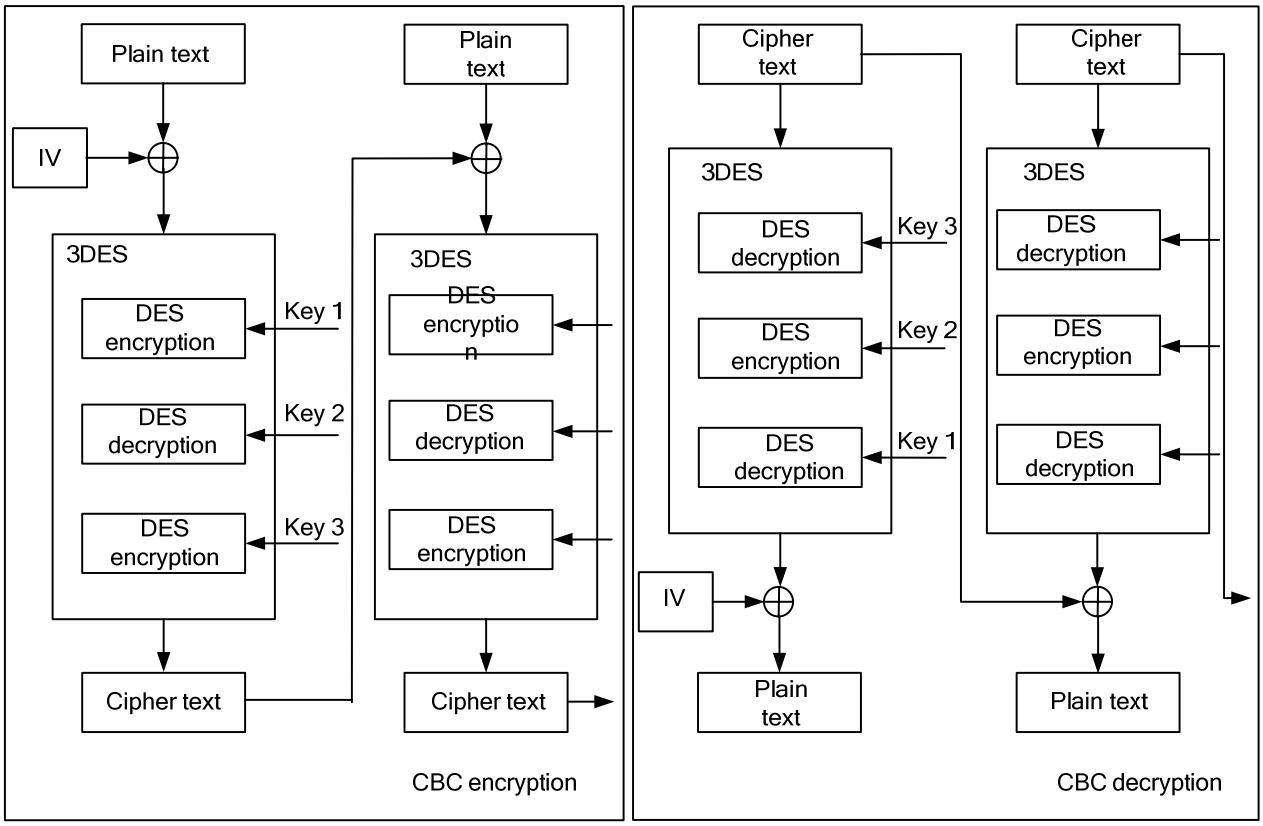
Figure 3-13 CBC mode of the 3DES algorithm



CFB Mode

The CFB mode is used to convert a block cipher into a stream cipher. This mode is implemented by selecting the operation bits of the CFB. The shift operation bits are represented by the letter s. The value of s is as follows:

- 1 bit, 8 bits, or 64 bits for the DES or 3DES algorithm
- 1 bit, 8 bits, or 128 bits for the AES algorithm

Figure 3-14 shows the s-bit CFB mode of the AES and DES algorithms, and Figure 3-15 shows the s-bit CFB mode of the 3DES algorithm.

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Figure 3-14 S-bit CFB mode of the AES and DES algorithms

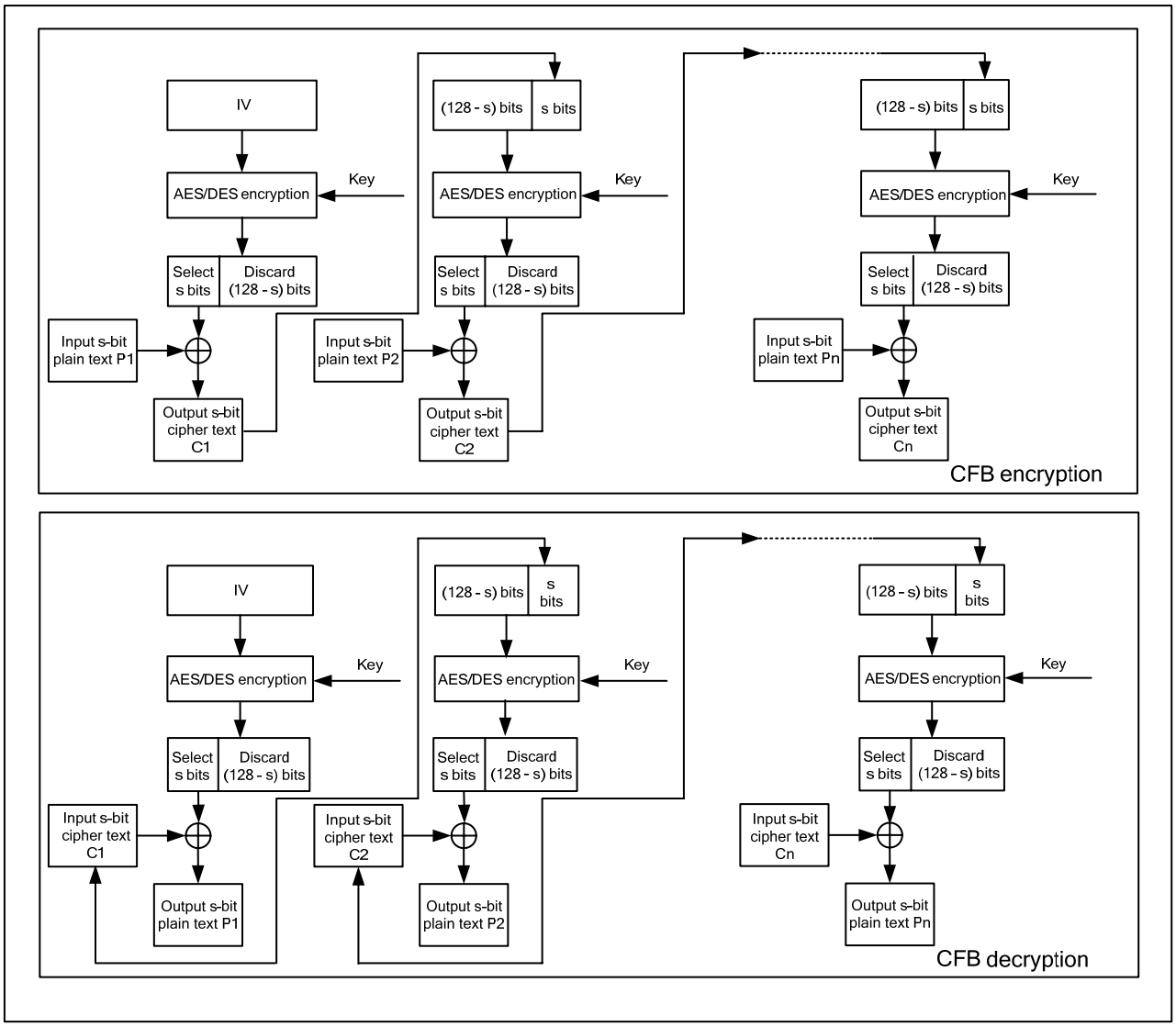

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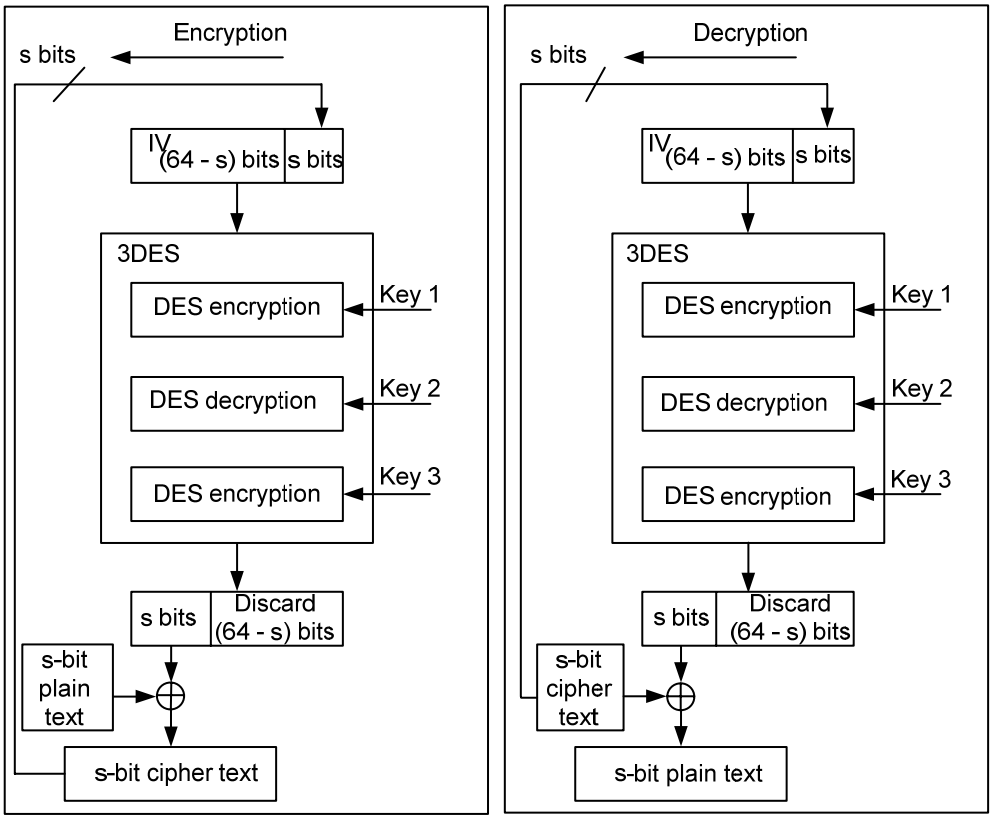
Figure 3-15 S-bit CFB mode of the 3DES algorithm



OFB Mode

In OFB mode, IVs serve as the inputs during encryption. If a same key is used, different IVs must be used to ensure operation security. The value of the s bit is as follows:

- 1 bit, 8 bits, or 64 bits for the DES or 3DES algorithm
- 128 bits for the AES algorithm

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Figure 3-16 shows the OFB mode of the AES algorithm.

Figure 3-16 OFB mode of the AES algorithm

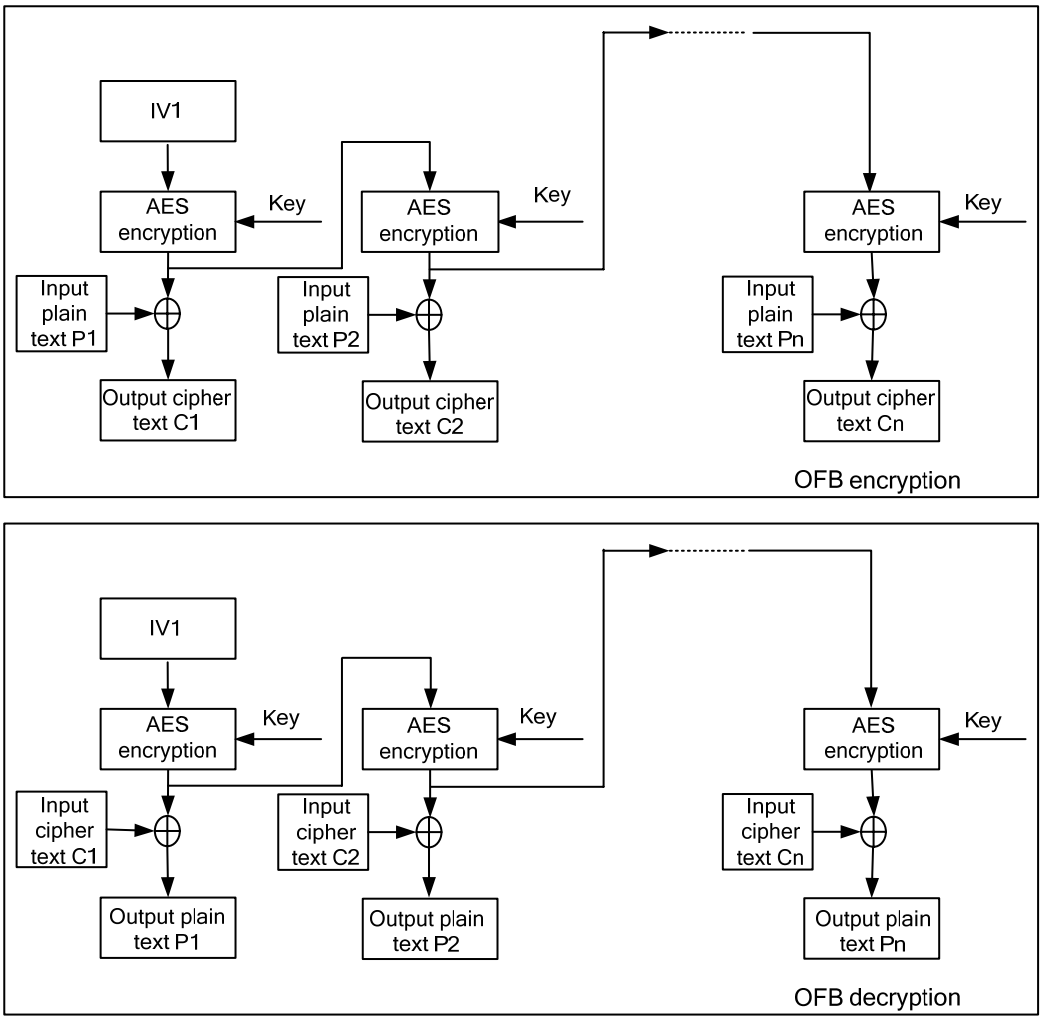

Figure 3-17 shows the s-bit OFB mode of the DES algorithm.

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Figure 3-17 S-bit OFB mode of the DES algorithm

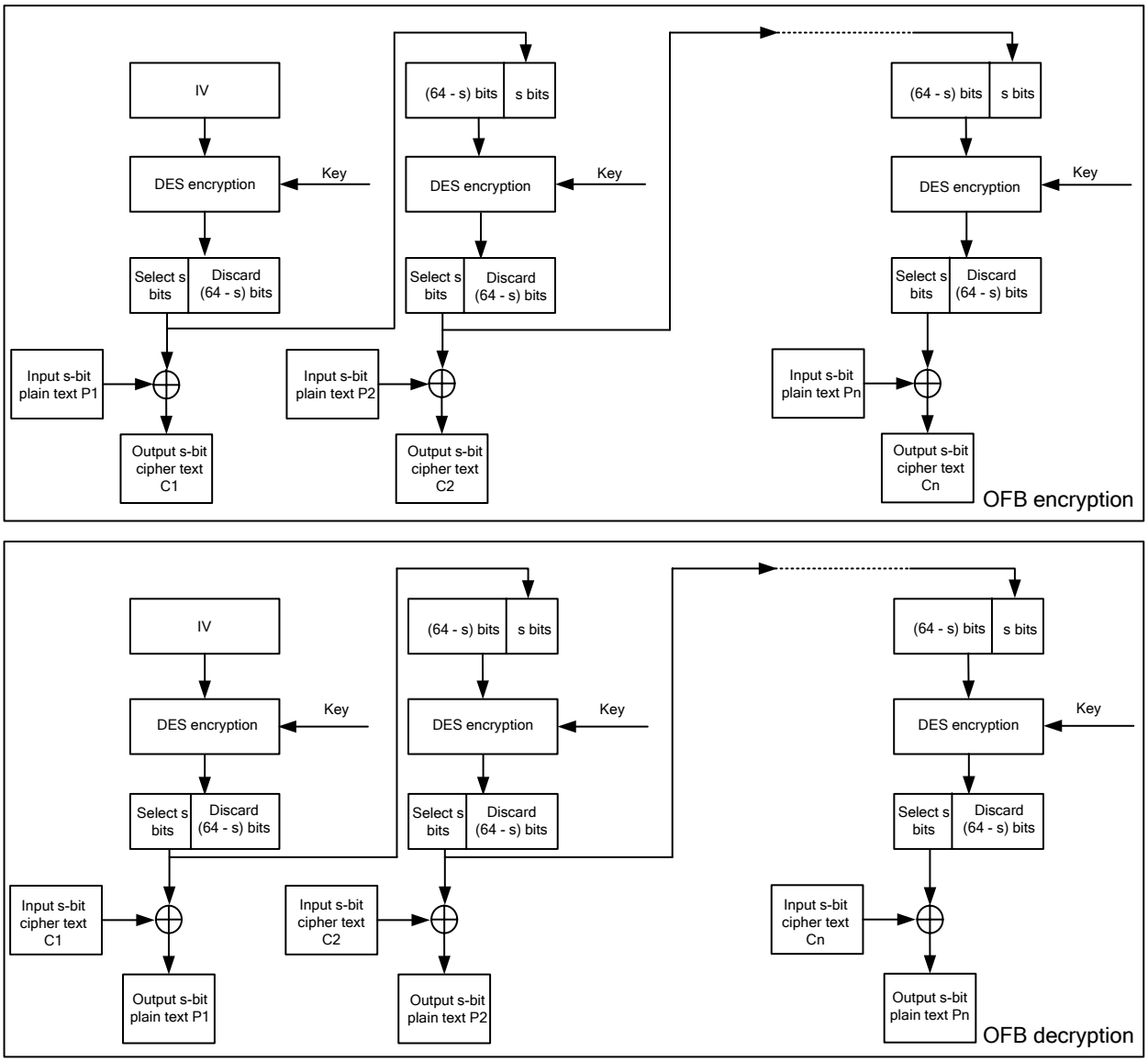

Figure 3-18 shows the s-bit OFB mode of the 3DES algorithm.

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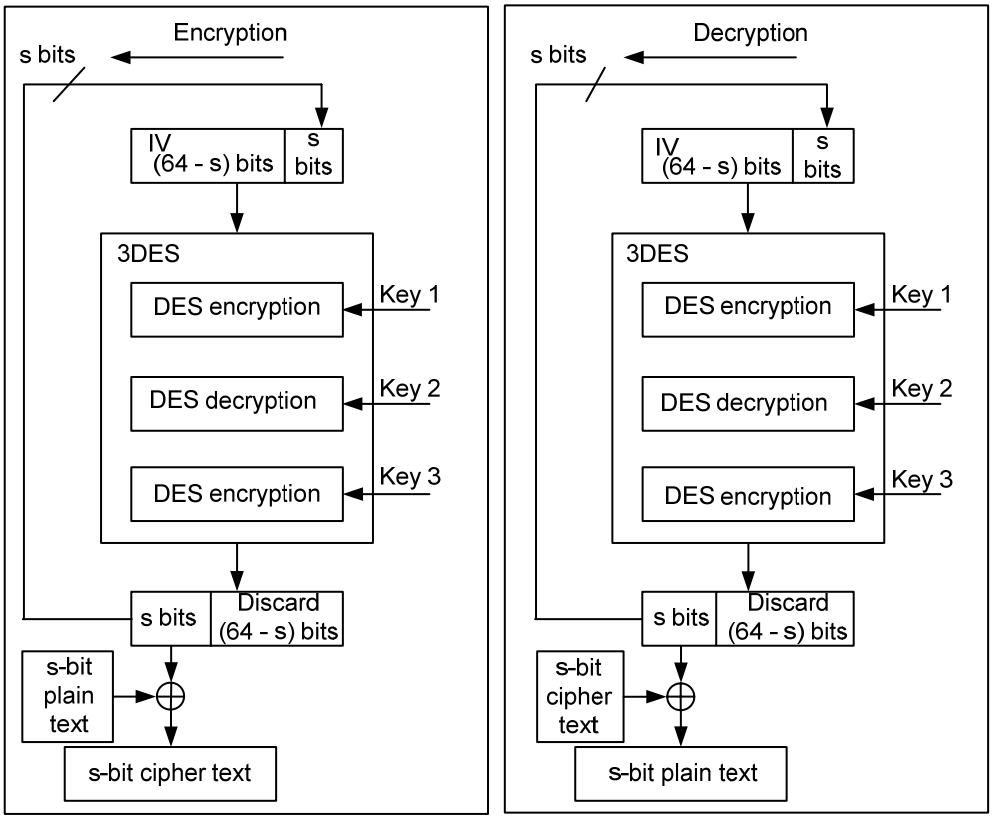
Figure 3-18 S-bit OFB mode of the 3DES algorithm



CTR Mode

In CTR mode, different data segments are input to the CIPHER module by using the AES algorithm to ensure data security. Such data can be the count value CTRn. Therefore, CTRn determines the security of the CTR mode.

NOTE

CTRn is obtained by using the accumulation count mode.

Figure 3-19 shows the CTR mode of the AES algorithm.

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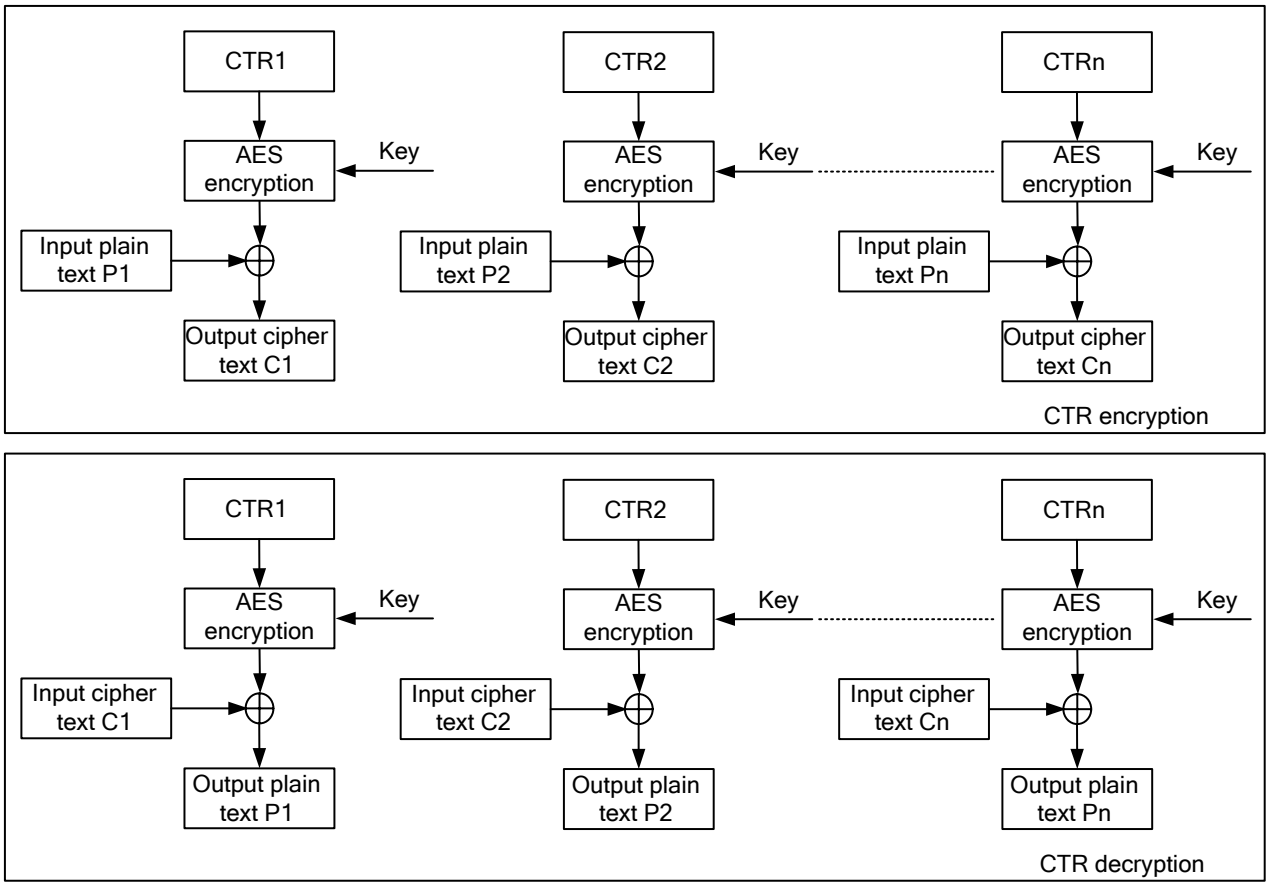
Figure 3-19 CTR mode of the AES algorithm



3.6.4 Operating Mode

Single-Block Operation Process of the CIPHER Module

The CIPHER module provides channel 0 as the single-block encryption/decryption channel. A single-block operation is performed as follows:

Step 1 Check whether channel 0 is busy by querying the ch0_busy field of the configuration register CHAN0_CFG of channel 0. If channel 0 is not busy, configure data inputs and write related configuration information to the registers of channel 0.

Step 2 Write to the ch0_start field of CHAN0_CFG to enable channel 0 to start encryption or decryption.

Step 3 Check whether encryption and decryption of channel 0 are complete in either of following ways:

- Query the ch0_busy field. If ch0_busy indicates that channel 0 is not busy, encryption and decryption are complete.
- Check whether the interrupt of channel 0 is generated. If the interrupt is generated, encryption and decryption are complete.

Step 4 Read the registers CHAN0_CIPHER_DOUT and CHAN0_CIPHER_IVOUT of channel 0.

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---End

Multi-Block Operation Process of the CIPHER Module

The CIPHER module provides seven multi-block encryption/decryption channels. The weighted value of each channel can be set using software based on its rate. These channels automatically read data from the DDR, and write the encrypted or decrypted data to the DDR.

A multi-block operation is performed as follows:

Step 1 Initialize the channels, including setting the depth, start address, number of multi-packet interrupts, aging interrupt time of the input and output queues of each channel, and setting the control register of each channel.

Step 2 When data needs to be encrypted or decrypted, query CHANn_IBUF_CNT. If the value of this register is smaller than the value of CHANn_IBUF_NUM, add the header of the data linked list corresponding to the data to be encrypted or decrypted to the input queue, and go to Step 4; otherwise, go to step 3.

Step 3 Enable the interrupt corresponding to the input queue channel, wait for the generation of the interrupt, read CHANn_IEMPTY_CNT, write to this register to clear the interrupt, and add new data to the input queue.

Step 4 Add the linked list header of the output buffer to the output queue.

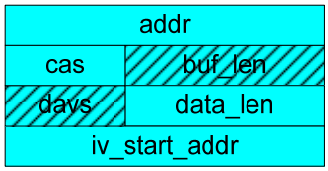
Step 5 Enable the interrupt corresponding to the output queue.

Step 6 Fetch data from the output queue, and write the number of currently received packets to CHANn_OFULL_CNT to clear the interrupt.

---End

Figure 3-20 shows the structure of the linked list header of a multi-block encryption/decryption channel.

Figure 3-20 Structure of the linked list header of a multi-block encryption/decryption channel



The field definitions are as follows:

- addr is the start address of the buffer pointer by the linked list header. The start address can be byte address.
- data_len is the length of the valid data pointed by the linked list header.
- cas is CIPHER control information.

Figure 3-21 shows the bits of cas.

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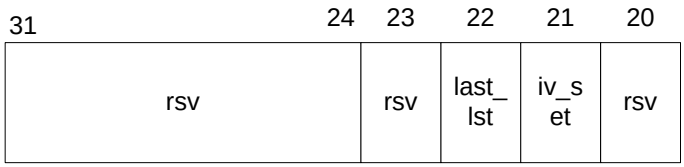
Figure 3-21 Bits of cas



- iv_set indicates that the IV of the data pointed by the current linked list header must be replaced. iv_start_addr indicates the start address of the IV in the DDR. This address must be aligned by word.
- last_lst indicates that the data pointed by the current linked list header is the last linked list of a data block. If the logic encounters an incomplete encryption/decryption block after processing the linked list, the logic writes the incomplete block to the output buffer without performing encryption and decryption.

Clock Gating

When no encryption is required and the CIPHER module is idle, the CIPHER clock can be disabled by configuring the registers of the system controller, which reduces power consumption.

Soft Reset

The CIPHER module can be soft-reset by configuring the registers of the system controller.

3.6.5 Register Summary

Table 3-34 describes CIPHER registers.

Table 3-34 Summary of CIPHER registers (base address: 0x100C_0000)

Offset Address	Register	Description	Page
0x0000–0x000C	CHAN0_CIPHER_DOUT	CIPHER output register for channel 0 (for single-block encryption/decryption)	3-160
0x0010–0x001C	CHAN0_CIPHER_IVOUT	Operation complete IV output register of the CIPHER module	3-161
0x0020–0x008C	CHAN_CIPHER_IVOUT	IV output register for channels 1–7	3-161
0x0090–0x018C	CIPHER_KEY	CPU configuration key register of the CIPHER module	3-162
0x1000	CHAN0_CIPHER_CTRL	Encryption/decryption control register for channel 0	3-163
0x1004–0x1010	CHAN0_CIPHER_IVIN	CIPHER VI block input register for channel 0	3-166

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Offset Address	Register	Description	Page
0x1014–0x1020	CHAN0_CIPHER_DIN	128-bit block input register of the CIPHER module	3-167
0x1000+n*128	CHANn_IBUF_NUM	Input queue total depth register for channel n (n = 1–7) (linked list header count register)	3-167
0x1000+n*128+0x4	CHANn_IBUF_CNT	Pending data buffer count register for channel n in the input queue	3-168
0x1000+n*128+0x8	CHANn_IEMPTY_CNT	Processed data buffer count register for channel n in the input queue	3-168
0x1000+n*128+0xC	CHANn_INT_ICNTCFG	Input queue multi-packet interrupt threshold register for channel n	3-169
0x1000+n*128+0x10	CHANn_CIPHER_CTRL	Encryption/decryption control register for channel n	3-169
0x1000+n*128+0x14	CHANn_SRC_LST_SADDR	Input queue start address register for channel n	3-171
0x1000+n*128+0x18	CHANn_IAGE_TIMER	Input queue interrupt aging time configuration register for channel n	3-171
0x1000+n*128+0x3C	CHANn_OBUF_NUM	Output queue total depth register for channel n (linked list header count register)	3-172
0x1000+n*128+0x40	CHANn_OBUF_CNT	Pending data buffer count register for channel n in the output queue	3-172
0x1000+n*128+0x44	CHANn_OFULL_CNT	Processed data buffer count register for channel n in the output queue	3-173
0x1000+n*128+0x48	CHANn_INT_OCNTCFG	Output queue multi-packet interrupt threshold register for channel n	3-173
0x1000+n*128+0x4C	CHANn_DEST_LST_SADDR	Output queue start address register for channel n	3-173
0x1000+n*128+0x50	CHANn_OAGE_TIMER	Output queue interrupt aging time configuration register for channel n	3-174
0x1400	INT_STATUS	Interrupt status register	3-174
0x1404	INT_EN	Interrupt enable register	3-175
0x1408	INT_RAW	Raw interrupt status register	3-176
0x140C	RST_STATUS	Reset status indicator register	3-177
0x1410	CHAN0_CFG	Channel 0 configuration register	3-177

Table 3-35 describes the value range and definition of the variable in the offset addresses of CIPHER registers.

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Table 3-35 Variable in the offset addresses of CIPHER registers

Variable	Value Range	Description
n	1–7	Channels 1–7 of the CIPHER module

3.6.6 Register Description

CHAN0_CIPHER_DOUT

CHAN0_CIPHER_DOUT is the CIPHER output register for channel 0 (for single-block encryption/decryption).

The data read from this register is the results of a single-block operation. The results of the AES algorithm are different from those of the DES or 3DES algorithm. The details are as follows:

- For the AES algorithm
  - If the 1-CFB mode is selected, the least significant bit (LSB) is valid, that is, CIPHER_DOUT bit[0] is valid.
  - If the 8-CFB mode is selected, lower eight bits are valid, that is, CIPHER_DOUT bit[7:0] is valid.
  - If the 128-CFB mode is selected, 128 bits are valid.
  - In other modes, 128 bits are valid.
- For the DES or 3DES algorithm
  - If the 1-CFB or 1-OFB mode is selected, the LSB is valid, that is, CIPHER_DOUT bit[0] is valid.
  - If the 8-CFB or 8-OFB mode is selected, lower eight bits are valid, that is, CIPHER_DOUT bit[7:0] is valid.
  - If the 64-CFB or 64-OFB mode is selected, lower 64 bits are valid, that is, CIPHER_DOUT bit[63:0] is valid.
  - In other modes, lower 64 bits are valid, that is, CIPHER_DOUT bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x0000–0x000C	CHAN0_CIPHER_DOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_dout																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan0_cipher_dout	128-bit block output of the CIPHER module. Each address maps to a 32-bit data segment. CIPHER_DOUT[31:0]: address 0x0000 CIPHER_DOUT[63:32]: address 0x0004 CIPHER_DOUT[95:64]: address 0x0008 CIPHER_DOUT[127:96]: address 0x000C

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CHAN0_CIPHER_IVOUT

CHAN0_CIPHER_IVOUT is an operation complete IV output register of the CIPHER module.

Note the following points when reading this register:

- This register can be ignored in ECB or CTR mode.
- If a single-block operation is performed, the data of this register is the vector output of the block. The data can be used as the vector input in the next block operation for the same data packet.
  - If the AES algorithm is selected, 128 bits are valid.
  - If the DES or 3DES algorithm is selected (CIPHER_CTRL[cipher_mode] = 0b00, 0b01, or 0b11), lower 64 bits are valid, that is, CIPHER_IVOUT bit[63:0] is valid.
- If a multi-block operation is performed, the data read from this register is the output vector of the last block operation.
  - If the AES algorithm is selected, 128 bits are valid.
  - If the DES or 3DES algorithm is selected, lower 64 bits are valid, that is, CIPHER_IVOUT bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x0010–0x001C	CHAN0_CIPHER_IVOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_ivout																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan0_cipher_ivout	Vector output after the operation of the CIPHER module is complete. It can be ignored in ECB or CTR mode. Each address maps to a 32-bit data segment. CIPHER_DOUT[31:0]: address 0x0010 CIPHER_IVOUT[63:32]: address 0x0014 CIPHER_IVOUT[95:64]: address 0x0018 CIPHER_IVOUT[127:96]: address 0x001C

CHAN_CIPHER_IVOUT

CHAN_CIPHER_IVOUT is the IV output register for channels 1–7.

Offset Address	Register Name	Total Reset Value
0x0020–0x008C	CHAN_CIPHER_IVOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan_cipher_ivout																															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan_cipher_ivout	0x0020–0x002C: channel 1 0x0030–0x003C: channel 2 0x0040–0x004C: channel 3 0x0050–0x005C: channel 4 0x0060–0x006C: channel 5 0x0070–0x007C: channel 6 0x0080–0x008C: channel 7

CIPHER_KEY

CIPHER_KEY is a CPU configuration key register of the CIPHER module. The key is the configured value of the CPU, and the CPU can be read or written.

Note the following points when configuring this register:

- If the DES algorithm is selected, lower 64 bits are valid, that is, CIPHER_KEY[63:0] is valid.
- For the 3DES algorithm

  If a 3-key operation is performed (CIPHER_CTRL[key_length] = 0b00, 0b01, or 0b10), low 192 bits are valid.

  where

  - CIPHER_KEY bit[63:0] indicates key 1.
  - CIPHER_KEY bit[127:64] indicates key 2.
  - CIPHER_KEY bit[191:128] indicates key 3.

  If a 2-key operation is selected (CIPHER_CTRL[key_length] = 0b11), lower 128 bits are valid.

  where

  - CIPHER_KEY bit[63:0] indicates key 1.
  - CIPHER_KEY bit[127:64] indicates key 2.
- For the AES algorithm
  - If a 128-bit key operation is performed, lower 128 bits are valid, that is, CIPHER_KEY bit[127:0] is valid.
  - If a 192-bit key operation is performed, lower 192 bits are valid, that is, CIPHER_KEY bit[191:0] is valid.
  - If a 256-bit key operation is performed, 256 bits are valid.

The CIPHER module allows you to configure eight keys. Each channel can use one key, and multiple channels can share one key.

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Offset Address	Register Name	Total Reset Value
0x0090–0x018C	CIPHER_KEY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cipher_key																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cipher_key	Key input of the CIPHER module. Each address maps to a 32-bit data segment. CIPHER_KEY[31:0]: address 0x0090 CIPHER_KEY[63:32]: address 0x0094 CIPHER_KEY[95:64]: address 0x0098 CIPHER_KEY[127:96]: address 0x009C CIPHER_KEY[159: 128]: address 0x00A0 CIPHER_KEY[191:160]: address 0x00A4 CIPHER_KEY[223:192]: address 0x00A8 CIPHER_KEY[255:224]: address 0x00AC 0x0090–0x00AC: host_key0 0x00B0–0x00CC: host_key1 0x00D0–0x00EC: host_key2 0x00F0–0x010C: host_key3 0x0110–0x012C: host_key4 0x0130–0x014C: host_key5 0x0150–0x016C: host_key6 0x0170–0x018C: host_key7

CHAN0_CIPHER_CTRL

CHAN0_CIPHER_CTRL is the encryption/decryption control register for channel 0. Channel 0 is a single-block encryption/decryption channel.

Note the following points when configuring this register:

- Configure this register before configuring others registers of the CIPHER module.
- In the modes except the CFB mode of the AES algorithm, the CIPHER_CTRL[width] cannot be set to 01 or 10.
- In the modes except the CFB and OFB modes of the DES and 3DES algorithms, CIPHER_CTRL[width] cannot be set to 01 or 10.

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Offset Address	Register Name	Total Reset Value
0x1000	CHAN0_CIPHER_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																key_adder				key_sel		byte_seq	reserved				key_length		ivin_sel	width			alg_sel		mode			decrypt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16:14]	RW	key_adder	ID of the key used by the current channel. 000: host_key0 001: host_key1 010: host_key2 011: host_key3 100: host_key4 101: host_key5 110: host_key6 111: host_key7
[13]	RW	key_sel	Key select. 0: keys configured by the CPU 1: keys generated by the key management module
[12]	-	reserved	Reserved.
[11]	-	reserved	Reserved.
[10:9]	RW	key_length	Key length select. For the AES algorithm: 00: 128 bits 01: 192 bits 10: 256 bits 11: 128 bits For the DES algorithm: 00: 3 keys 01: 3 keys 10: 3 keys 11: 2 keys
[8]	RW	ivin_sel	Input select of CIPHER_IVIN. 0: do not configure CIPHER_IVIN 1: configure CIPHER_IVIN

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Offset Address	Register Name	Total Reset Value
0x1000	CHAN0_CIPHER_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																key_adder		key_sel	byte_seq	reserved		key_length		ivin_sel	width		alg_sel		mode		decrypt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RW	width	Bit width control. For the DES or 3DES algorithm: 00: 64 bits 01: 8 bits 10: 1 bit 11: 64 bits For the AES algorithm: 00: 128 bits 01: 8 bits 10: 1 bit 11: 128 bits
[5:4]	RW	alg_sel	Algorithm select. 00: DES algorithm 01: 3DES algorithm 10: AES algorithm 11: DES algorithm
[3:1]	RW	mode	Operating mode select. For the AES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode 100: CTR mode Other values: ECB mode For the DES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode Other values: ECB mode

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Offset Address	Register Name	Total Reset Value
0x1000	CHAN0_CIPHER_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																key_adder		key_sel	byte_seq	reserved		key_length		ivin_sel	width		alg_sel		mode		decrypt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	decrypt	Encryption/decryption select. 0: encryption 1: decryption

CHAN0_CIPHER_IVIN

CHAN0_CIPHER_IVIN is the CIPHER VI block input register for channel 0.

Assume that channel 0 is selected for the single-block encryption/decryption and the selected mode is not ECB mode (CIPHER_CTRL[mode] = 0b001, 0b010, 0b011, or 0b100).

- If you do not want to configure the input vector (CIPHER_CTRL[ivin_sel] = 0b0), CIPHER_IVIN can be ignored.
- If you want to configure the input vector (CIPHER_CTRL[ivin_sel] = 0b1), CIPHER_IVIN needs to be configured. If the AES algorithm is selected (CIPHER_CTRL [alg_sel] = 0b10), CIPHER_IVIN bit[127:0] is valid. If the DES or 3DES algorithm is selected (CIPHER_CTRL[alg_sel] = 0b00, 0b01, or 0b11), lower 64 bits are valid, that is, CIPHER_IVIN bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x1004–0x1010	CHAN0_CIPHER_IVIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_ivin																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_cipher_ivin	128-bit IV of the CIPHER module for channel 0 or the data input from the counter. Each address maps to a 32-bit data segment. CIPHER_IVIN[31:0]: address 0x1004 CIPHER_IVIN[63:32]: address 0x1008 CIPHER_IVIN[95:64]: address 0x100C CIPHER_IVIN[127:96]: address 0x1010

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CHAN0_CIPHER_DIN

CHAN0_CIPHER_DIN is a 128-bit block input register of the CIPHER module.

Note the following points when configuring this register:

If channel 0 is selected for the single-block operation, this register needs to be configured.

- Assume that the AES algorithm (CIPHER_CTRL[alg_sel] = 0b10) is selected.
  - If the 1-CFB mode is selected, the LSB is valid, that is, CIPHER_DIN bit[0] is valid.
  - If the 8-CFB mode is selected, lower eight bits are valid, that is, CIPHER_DIN bit[7:0] is valid.
  - If the 128-CFB mode is selected, 128 bits are valid.
  - In other modes, 128 bits are valid.
- Assume that the DES or the 3DES algorithm (CIPHER_CTRL[alg_sel] = 0b00, 0b01, or 0b11) is selected.
  - If the 1-CFB or 1-OFB mode is selected, the LSB is valid, that is, CIPHER_DIN bit[0] is valid.
  - If the 8-CFB or 8-OFB mode is selected, lower eight bits are valid, that is, CIPHER_DIN bit[7:0] is valid.
  - If the 64-CFB or 64-OFB mode is selected, lower 64 bits are valid, that is, CIPHER_DIN bit[63:0] is valid.
  - In other modes, lower 64 bits are valid, that is, CIPHER_DIN bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x1014–0x1020	CHAN0_CIPHER_DIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_din																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_cipher_din	128-bit block input of the CIPHER module for channel 0. Each address maps to a 32-bit data segment. CIPHER_DIN[31:0]: address 0x1014 CIPHER_DIN[63:32]: address 0x1018 CIPHER_DIN[95:64]: address 0x101c CIPHER_DIN[127:96]: address 0x1020

CHANn_IBUF_NUM

CHANn_IBUF_NUM is the input queue total depth register for channel n (n = 1–7). This register can be used to configure the count of linked list headers.

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Offset Address	Register Name	Total Reset Value
0x1000+n*128	CHANn_IBUF_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ibuf_num															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	ibuf_num	Input queue depth, that is, count of linked list headers configured for each channel.

CHANn_IBUF_CNT

CHANn_IBUF_CNT is the pending data buffer count register for channel n in the input queue. When this register is written by using software, the logic adds the original value of the register and the written value. After the logic processes a buffer, the value of this register is decreased by 1.

Offset Address	Register Name	Total Reset Value
0x1000+n*128+0x4	CHANn_IBUF_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ibuf_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	ibuf_cnt	Count of buffers to be processed in the input queue.

CHANn_IEMPTY_CNT

CHANn_IEMPTY_CNT is the processed buffer count register for channel n in the input queue. When this register is written by software, the logic subtracts the written value from the original value of this register. After the logic processes a buffer, the value of this register is increased by 1.

Offset Address	Register Name	Total Reset Value
0x1000+n*128+0x8	CHANn_IEMPTY_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																iempty_cnt															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	iempty_cnt	Count of processed buffers in the input queue.

CHANn_INT_ICNTCFG

CHANn_INT_ICNTCFG is the input queue multi-packet interrupt threshold register for channel n. When the count of buffers in the input queue processed by the logic is above the threshold, an input queue interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000+n*128+0xC	CHANn_INT_ICNTCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_icnt_cfg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	int_icnt_cfg	Input queue multi-packet interrupt threshold.

CHANn_CIPHER_CTRL

CHANn_CIPHER_CTRL is the encryption/decryption control register for channel n.

Note the following points when configuring this register:

- You must configure this register before performing encryption or decryption using the channel.
- In the modes other than the CFB mode of the AES algorithm, CIPHER_CTRL[width] cannot be set to 01 or 10.
- In the modes other than the CFB and OFB modes of the DES or 3DES algorithm, CIPHER_CTRL[width] cannot be set to 01 or 10.

Offset Address	Register Name	Total Reset Value
0x1000+n*128+0x10	CHANn_CIPHER_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	weight												reserved				key_adder			key_sel	byte_seq	ts_vld	key_length		reserved	width		alg_sel		mode		decrypt

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	-	weight	Weighted value of the current channel, in the unit of 64 bytes.
[21:17]	-	reserved	Reserved.
[16:14]	RW	key_adder	ID of the key used by the current channel. The key can be any one in the addresses 0–7.
[13]	RW	key_sel	Key select 0: keys configured by the CPU 1: keys generated by the key management module
[12:11]	-	reserved	Reserved.
[10:9]	RW	key_length	Key length select. For the AES algorithm: 00: 128 bits 01: 192 bits 10: 256 bits 11: 128 bits For the DES algorithm: 00: 3 keys 01: 3 keys 10: 3 keys 11: 2 keys
[8]	-	reserved	Reserved.
[7:6]	RW	width	Bit width control. For the DES or 3DES algorithm: 00: 64 bits 01: 8 bits 10: 1 bit 11: 64 bits For the AES algorithm: 00: 128 bits 01: 8 bits 10: 1 bit 11: 128 bits
[5:4]	RW	alg_sel	Algorithm select. 00: DES algorithm 01: 3DES algorithm 10: AES algorithm 11: DES algorithm

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[3:1]	RW	mode	Operating mode select. For the AES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode 100: CTR mode Other values: ECB mode For the DES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode Other values: ECB mode
[0]	RW	decrypt	Encryption/decryption select. 0: encryption 1: decryption

CHANn_SRC_LST_SADDR

CHANn_SRC_LST_SADDR is the input queue start address register for channel n. The address must be aligned by word.

Offset Address	Register Name	Total Reset Value
0x1000+n*128+0x14	CHANn_SRC_LST_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	src_lst_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	src_lst_saddr	Start address of the input queue.

CHANn_IAGE_TIMER

CHANn_IAGE_TIMER is the input queue interrupt aging time configuration register for channel n. If an overflow occurs in the aging time counter and the count of processed buffers in the input queue is greater than 0, an input queue processing complete interrupt is reported.

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Offset Address	Register Name	Total Reset Value
0x1000+n*128+0x18	CHANn_IAGE_TIMER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																iage_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	iage_timer	Aging interrupt timer.

CHANn_OBUF_NUM

CHANn_OBUF_NUM is the output queue total depth register for channel n. This register can be used to configure the count of linked list headers.

Offset Address	Register Name	Total Reset Value
0x1000+n*128+0x3C	CHANn_OBUF_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																obuf_num															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	obuf_num	Total depth of the output queue.

CHANn_OBUF_CNT

CHANn_OBUF_CNT is the pending data buffer count register for channel n in the output queue. When this register is written by using software, the logic adds the original value of the register and the written value. After the logic processes a buffer, the value of this register is decreased by 1.

Offset Address	Register Name	Total Reset Value
0x1000+n*128+0x40	CHANn_OBUF_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																obuf_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.

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[15:0]	RW	obuf_cnt	Count of buffers to be processed in the output queue.

CHANn_OFULL_CNT

CHANn_OFULL_CNT is the processed buffer count register for channel n in the output queue. When this register is written by software, the logic subtracts the written value from the original value of this register. After the logic processes a buffer, the value of this register is increased by 1.

Offset Address	Register Name	Total Reset Value
0x1000+n*128+0x44	CHANn_OFULL_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ofull_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	ofull_cnt	Count of processed buffers in the output queue.

CHANn_INT_OCNTCFG

CHANn_INT_OCNTCFG is the output queue multi-packet interrupt threshold register for channel n. When the count of buffers in the output queue processed by the logic is above the threshold, an output queue interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000+n*128+0x48	CHANn_INT_OCNTCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_ocnt_cfg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	int_ocnt_cfg	Output queue multi-packet interrupt threshold.

CHANn_DEST_LST_SADDR

CHANn_DEST_LST_SADDR is the output queue start address register for channel n. The address must be aligned by word.

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Offset Address	Register Name	Total Reset Value
0x1000+n*128+0x4C	CHANn_DEST_LST_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dest_lst_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dest_lst_saddr	Start address of the output queue.

CHANn_OAGE_TIMER

CHANn_OAGE_TIMER is the output queue interrupt aging time configuration register for channel n. If an overflow occurs in the aging time counter and the count of processed buffers in the output queue is greater than 0, an output queue processing complete interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000+n*128+0x50	CHANn_OAGE_TIMER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																oage_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	oage_timer	Aging interrupt timer.

INT_STATUS

INT_STATUS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1400	INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ch7_ibuf_int	ch6_ibuf_int	ch5_ibuf_int	ch4_ibuf_int	ch3_ibuf_int	ch2_ibuf_int	ch1_ibuf_int	ch0_ibuf_int	ch7_obuf_int	ch6_obuf_int	ch5_obuf_int	ch4_obuf_int	ch3_obuf_int	ch2_obuf_int	ch1_obuf_int	reserved

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15]	RO	ch7_ibuf_int	Input queue data interrupt for channel 7.
[14]	RO	ch6_ibuf_int	Input queue data interrupt for channel 6.
[13]	RO	ch5_ibuf_int	Input queue data interrupt for channel 5.
[12]	RO	ch4_ibuf_int	Input queue data interrupt for channel 4.
[11]	RO	ch3_ibuf_int	Input queue data interrupt for channel 3.
[10]	RO	ch2_ibuf_int	Input queue data interrupt for channel 2.
[9]	RO	ch1_ibuf_int	Input queue data interrupt for channel 1.
[8]	RO	ch0_ibuf_int	Data processing complete interrupt for channel 0.
[7]	RO	ch7_obuf_int	Output queue data interrupt for channel 7.
[6]	RO	ch6_obuf_int	Output queue data interrupt for channel 6.
[5]	RO	ch5_obuf_int	Output queue data interrupt for channel 5.
[4]	RO	ch4_obuf_int	Output queue data interrupt for channel 4.
[3]	RO	ch3_obuf_int	Output queue data interrupt for channel 3.
[2]	RO	ch2_obuf_int	Output queue data interrupt for channel 2.
[1]	RO	ch1_obuf_int	Output queue data interrupt for channel 1.
[0]	-	reserved	Reserved.

INT_EN

INT_EN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x1404	INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_en	reserved															ch7_ibuf_en	ch6_ibuf_en	ch5_ibuf_en	ch4_ibuf_en	ch3_ibuf_en	ch2_ibuf_en	ch1_ibuf_en	ch0_ibuf_en	ch7_obuf_en	ch6_obuf_en	ch5_obuf_en	ch4_obuf_en	ch3_obuf_en	ch2_obuf_en	ch1_obuf_en	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	int_en	Total interrupt enable for the CIPHER module.

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[30:16]	-	reserved	Reserved.
[15]	RW	ch7_ibuf_en	Input queue data interrupt enable for channel 7.
[14]	RW	ch6_ibuf_en	Input queue data interrupt enable for channel 6.
[13]	RW	ch5_ibuf_en	Input queue data interrupt enable for channel 5.
[12]	RW	ch4_ibuf_en	Input queue data interrupt enable for channel 4.
[11]	RW	ch3_ibuf_en	Input queue data interrupt enable for channel 3.
[10]	RW	ch2_ibuf_en	Input queue data interrupt enable for channel 2.
[9]	RW	ch1_ibuf_en	Input queue data interrupt enable for channel 1.
[8]	RW	ch0_ibuf_en	Data processing complete interrupt enable for channel 0.
[7]	RW	ch7_obuf_en	Output queue data interrupt enable for channel 7.
[6]	RW	ch6_obuf_en	Output queue data interrupt enable for channel 6.
[5]	RW	ch5_obuf_en	Output queue data interrupt enable for channel 5.
[4]	RW	ch4_obuf_en	Output queue data interrupt enable for channel 4.
[3]	RW	ch3_obuf_en	Output queue data interrupt enable for channel 3.
[2]	RW	ch2_obuf_en	Output queue data interrupt enable for channel 2.
[1]	RW	ch1_obuf_en	Output queue data interrupt enable for channel 1.
[0]	-	reserved	Reserved.

INT_RAW

INT_RAW is a raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1408	INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ch7_ibuf_raw	ch6_ibuf_raw	ch5_ibuf_raw	ch4_ibuf_raw	ch3_ibuf_raw	ch2_ibuf_raw	ch1_ibuf_raw	ch0_ibuf_raw	ch7_obuf_raw	ch6_obuf_raw	ch5_obuf_raw	ch4_obuf_raw	ch3_obuf_raw	ch2_obuf_raw	ch1_obuf_raw	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15]	RWC	ch7_ibuf_raw	Raw input queue data interrupt for channel 7.
[14]	RWC	ch6_ibuf_raw	Raw input queue data interrupt for channel 6.

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[13]	RWC	ch5_ibuf_raw	Raw input queue data interrupt for channel 5.
[12]	RWC	ch4_ibuf_raw	Raw input queue data interrupt for channel 4.
[11]	RWC	ch3_ibuf_raw	Raw input queue data interrupt for channel 3.
[10]	RWC	ch2_ibuf_raw	Raw input queue data interrupt for channel 2.
[9]	RWC	ch1_ibuf_raw	Raw input queue data interrupt for channel 1.
[8]	RWC	ch0_ibuf_raw	Raw data processing complete interrupt for channel 0.
[7]	RWC	ch7_obuf_raw	Raw output queue data interrupt for channel 7.
[6]	RWC	ch6_obuf_raw	Raw output queue data interrupt for channel 6.
[5]	RWC	ch5_obuf_raw	Raw output queue data interrupt for channel 5.
[4]	RWC	ch4_obuf_raw	Raw output queue data interrupt for channel 4.
[3]	RWC	ch3_obuf_raw	Raw output queue data interrupt for channel 3.
[2]	RWC	ch2_obuf_raw	Raw output queue data interrupt for channel 2.
[1]	RWC	ch1_obuf_raw	Raw output queue data interrupt for channel 1.
[0]	-	reserved	Reserved.

RST_STATUS

RST_STATUS is a reset status indicator register.

Offset Address	Register Name	Total Reset Value
0x140C	RST_STATUS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								rst_status
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	rst_status	Reset status indicator of the CIPHER module. 0: The CIPHER module is being reset. 1: The CIPHER module is working properly.

CHAN0_CFG

CHAN0_CFG is channel 0 configuration register.

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Offset Address	Register Name	Total Reset Value
0x1410	CHAN0_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														ch0_busy	ch0_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved.
[1]	RO	ch0_busy	Status signal of channel 0.
[0]	RW	ch0_start	Encryption/decryption start signal of channel 0.

3.7 Timer

3.7.1 Overview

The timer module implements the timing and counting functions. It not only serves as the system clock of the operating system, but also can be used by applications for timing and counting. The timer module has four dual-timer modules: dual-timer0, dual-timer1, dual-timer2, and dual-timer3.Besides the different base addresses, the four dual-timer modules provide different functions in the system applications. The details about the four dual-timer modules are as follows:

- Dual-timer0 consists of timer0 and timer1 that share a base address and an interrupt signal.
- Dual-timer1 consists of timer2 and timer3 that share a base address and an interrupt signal.
- Dual-timer2 consists of timer4 and timer5 that share a base address and an interrupt signal.
- Dual-timer3 consists of timer6 and timer7 that share a base address and an interrupt signal.

Each dual-timer module consists of two timers with the same functions.

3.7.2 Features

Each dual-timer module has the following features:

- Provides two 16-bit or 32-bit down counters. Each counter has a programmable 8-bit prescaler.
- Provides a configurable count clock, that is, the clock can serve as the clock of the advanced peripheral bus (APB) or 3 MHz crystal oscillator clockSupports three count modes: free-running mode, periodic mode, and one-shot mode.

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- Loads the initial value through either of the following registers: TIMERx_LOAD and TIMERx_BGLOAD
- Reads the current count value at any time
- Generates an interrupt when the count value is decreased to 0

3.7.3 Function Description

Function Principle

The timer is a 32-bit or 16-bit configurable down counter. The counter value is decremented by 1 on each rising edge of the count clock. When the count value reaches 0, the timer generates an interrupt.

The timer supports three count modes:

- Free-running mode

  The timer counts continuously. When the count value reaches 0, the timer wraps its value around to the maximum value automatically and then continues to count. When the count length is 32 bits, the maximum value is 0xFFFF_FFFF.When the count length is 16 bits, the maximum value is 0xFFFF.In free-running mode, the count value is decremented immediately from the loaded value. When the value reaches 0, the value is wrapped around to the maximum value.
- Periodic mode

  The timer counts continuously. When the count value reaches 0, the timer loads an initial value from TIMERx_BGLOAD again and then continues to count.
- One-shot mode

  The initial value is loaded to the timer. When the count value of the timer reaches 0, the timer stops counting. The timer starts to count again only when a new value is loaded and the timer is enabled.

Each timer has a prescaler that divides the frequency of the working clock of each timer by 1, 16, or 256.In this way, flexible frequencies of the count clock are provided. An initial value is loaded to the timer as follows:

- An initial value can be loaded by writing TIMERx_LOAD. When the timer works, if a value is written to TIMERx_LOAD, the timer recounts starting from this value immediately. This method is applicable to all count modes.
- The count cycle in periodic mode can be set by writing TIMERx_BGLOAD. The current count value of the timer is not affected immediately when TIMERx_BGLOAD is written. Instead, the timer continues to count until the count value reaches 0. Then the timer loads the new value of TIMERx_BGLOAD and starts to count.

3.7.4 Operating Mode

Initialization

The timer must be initialized when the system is initialized. To initialize timerX (X ranges from 0 to 7), do as follows:

Step 1 Write to TIMERx_LOAD to load an initial value to the timer.

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Step 2 When the timer is required to work in periodic mode and the count cycle is different from the initial value loaded to the timer, write to TIMERx_BGLOAD to set the count cycle of the timer.

Step 3 Configure the SC_CTRL register of the system controller to set the reference clock of the clock enable signal of the timer.

Step 4 Write to TIMERx_CONTROL to set the count mode, counter length, prescaling factor, and interrupt mask of the timer, and then enable the timer to count.

----End

Interrupt Processing

The timer is used to generate interrupts periodically. Therefore, interrupt processing is a process of activating and waiting the timing interrupt. To process an interrupt, do as follows:

Step 1 Configure TIMERx_INTCLR to clear the interrupt of the timer.

Step 2 Activate the processes of waiting for the interrupt and execute the process.

Step 3 When all the processes of waiting for the interrupt are complete or the wait interrupt is in hibernate state, resume the interrupt and continue to execute the interrupted program.

----End

Clock Selection

Each timer has two optional count clocks. The following sections describe how to select a clock by taking timer0 as an example.

To select the APB clock as the count clock, do as follows:

Step 1 Set SC_CTRL[timeren0ov] to 1.

Step 2 Initialize the timer and start to count.

----End

To select the 3 MHz crystal oscillator clock as the count clock, do as follows:

Step 1 Set SC_CTRL[timeren0ov] to 0.

Step 2 Set SC_CTRL[timeren0sel] to 0.

Step 3 Initialize the timer and start to count.

----End

3.7.5 Register Summary

The timer module consists of eight timers and each timer involves a group of registers. The eight groups of registers have the same features except that their base addresses and offset addresses are different. The details about their base addresses are as follows:

- The base address of timer 0: 0x2000_0000.
- The base address of timer 1: 0x2000_0020.

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- The base address of timer 2: 0x2001_0000.
- The base address of timer 3: 0x2001_0020.
- The base address of timer 4: 0x2013_0000.
- The base address of timer 5: 0x2013_0020.
- The base address of timer 6: 0x2014_0000.
- The base address of timer 7: 0x2014_0020.

NOTE

The value of X in timerX ranges from 0 to 7. The registers for timer 0 to timer 7 are the same. In this section, timer 0 registers are described as an example.

Table 3-36 Summary of timer registers

Offset Address	Register	Description	Page
0x000	TIMERx_LOAD	Initial count value register	3-181
0x004	TIMERx_VALUE	Current count value register	3-182
0x008	TIMERx_CONTROL	Control register	3-182
0x00C	TIMERx_INTCLR	Interrupt clear register	3-184
0x010	TIMERx_RIS	Raw interrupt status register	3-184
0x014	TIMERx_MIS	Masked interrupt status register	3-185
0x018	TIMERx_BGLOAD	Initial count value register in periodic mode	3-185

3.7.6 Register Description

TIMERx_LOAD

TIMERx_LOAD is the initial count value register. It is used to set the initial count value of each timer. Each timer (timer0–timer7) has one such register.

NOTE

- The minimum valid value written to TIMERx_LOAD is 1.
- When the value 0 is written to TIMERx_LOAD, the dual-timer module generates an interrupt immediately.

If values are written to TIMERx_BGLOAD and TIMERx_LOADbefore the rising edge of TIMCLK enabled by TIMCLKENx reaches, the count value of the next rising edge of TIMCLK is changed to the value written to TIMERx_LOAD. As the value of TIMERx_BGLOAD changes when data is written to TIMERx_LOAD, the value returned after TIMERx_BGLOAD is read is the latest value that is written to TIMERx_LOAD and TTIMERx_BGLOAD. When the timer works in periodic mode and the count value decreases to 0, the initial value is loaded from TIMERx_BGLOAD to continue counting.

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Offset Address	Register Name	Total Reset Value
0x000	TIMER0_LOAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_load																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	timer0_load	Initial count value of timer0

TIMERx_VALUE

TIMERx_VALUE is the current count value register. It shows the current value of the counter that is decremented. Each timer (timer0–timer7) has one such register.

After a value is written to TIMERx_LOAD, TIMERx_VALUE immediately shows the newly loaded value of the counter in the PCLK domain without waiting for the clock edge of TIMCLK enabled by TIMCLKENx.

NOTE

When a timer is in 16-bit mode, the 16 upper bits of the 32-bit TIMERx_VALUE are not set to 0 automatically. If the timer is switched from 32-bit mode to 16-bit mode and no data is written to TIMERx_LOAD, the upper 16 bits of TIMERx_VALUE may be non-zero.

Offset Address	Register Name	Total Reset Value
0x004	TIMER0_VALUE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_value																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	timer0_value	Current count value of timer0 that is decremented.

TIMERx_CONTROL

TIMERx_CONTROL is the control register. Each timer (timer0–timer7) has one such register.

NOTE

When the periodic mode is selected, TIMERx_CONTROL[timermode] must be set to 1 and TIMERx_CONTROL[oneshot] must be set to 0.

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Offset Address	Register Name	Total Reset Value
0x008	TIMER0_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								timeren	timermode	intenable	reserved	timerpre		timersize	oneshot
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7]	RW	timeren	Timer enable. 0: disabled 1: enabled
[6]	RW	timermode	Timer count mode. 0: free-running mode 1: periodic mode
[5]	RW	intenable	Raw interrupt mask. 0: masked 1: not masked
[4]	-	reserved	Reserved.
[3:2]	RW	timerpre	Prescaling factor configuration. 00: no prescaling. That is, the clock frequency of the timer is divided by 1 01: 4-level prescaling. That is, the clock frequency of the timer is divided by 16 10: 8-level prescaling. That is, the clock frequency of the timer is divided by 256 11: undefined. If the bits are set to 11, 8-level prescaling is considered. That is, the clock frequency of the timer is divided by 256.
[1]	RW	timersize	Counter select. 0: 16-bit counter 1: 32-bit counter
[0]	RW	oneshot	Count mode select. 0: periodic mode or free-running mode 1: one-shot mode

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TIMERx_INTCLR

TIMERx_INTCLR is the interrupt clear register. The interrupt status of a counter is cleared after any operation is performed on this register. Each timer (timer0–timer7) has one such register.

CAUTION

This register is a write-only register. The timer clears interrupts when any value is written to this register. In addition, no value is recorded in this register and no default reset value is defined.

Offset Address	Register Name	Total Reset Value
0x00C	TIMER0_INTCLR	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_intclr																															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Access	Name	Description
[31:0]	WO	timer0_intclr	Writing this register clears the output interrupt of timer0.

TIMERx_RIS

TIMERx_RIS is the raw interrupt status register. Each timer (timer0–timer7) has one such register.

Offset Address	Register Name	Total Reset Value
0x010	TIMER0_RIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															timer0ris
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved. Writing this register has no effect and reading this register returns 0.
[0]	RO	timer0ris	Raw interrupt status of timer0. 0: No interrupt is generated. 1: An interrupt is generated.

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TIMERx_MIS

TIMERx_MIS is the masked interrupt status register. Each timer (timer0–timer7) has one such register.

Offset Address	Register Name	Total Reset Value
0x014	TIMER0_MIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															timer0mis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	timer0mis	Masked interrupt status of timer0. 0: The interrupt is invalid. 1: The interrupt is valid.

TIMERx_BGLOAD

TIMERx_BGLOAD is the initial count value register in periodic mode. Each timer (timer0–timer7) has one such register.

The TIMERx_BGLOAD register contains the initial count value of the timer. This register is used to reload an initial count value when the count value of the timer reaches 0 in periodic mode.

In addition, this register provides another method of accessing TIMERx_LOAD. The difference is that after a value is written to TIMERx_BGLOAD, the timer does not count starting from the input value immediately.

Offset Address	Register Name	Total Reset Value
0x018	TIMER0_BGLOAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0bgload																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	timer0bgload	Initial count value of timer0. Note: This register differs from TIMERx_LOAD. For details, see the descriptions of TIMERx_LOAD.

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3.8 Watchdog

3.8.1 Overview

The watchdog is used to transmit a reset signal to reset the entire system within a period after an exception occurs in the system.

3.8.2 Features

The watchdog has the following features:

- Provides a 32-bit internal down counter. The count clock source is configurable.
- Supports the configurable timeout interval, namely, initial count value.
- Locks registers to avoid any modification to them.
- Supports the generation of timeout interrupts.
- Supports the generation of reset signals.
- Supports the debugging mode.

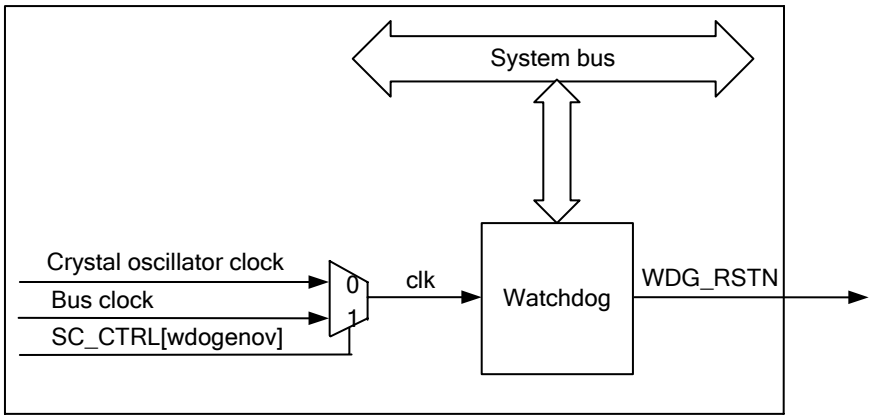
3.8.3 Function Description

Application Block Diagram

The system selects clocks for the watchdog by configuring SC_CTRL[wdogenov] and configures the parameter values of watchdog registers by using the system bus. The watchdog transmits interrupt requests to the system periodically. When the system does not respond to the interrupt requests (such as the suspend case), the watchdog transmits the WDG_RSTN reset signal to reset the system. In this way, the system running status is monitored.

Figure 3-22 shows the application block diagram of the watchdog.

Figure 3-22 Application block diagram of the watchdog



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Function Principle

The watchdog works based on a 32-bit down counter. The initial value is loaded by WDG_LOAD. When the watchdog clock is enabled, the count value is decremented by 1 on the rising edge of each count clock. When the count value reaches 0, the watchdog generates an interrupt. On the next rising edge of the count clock, the counter reloads the initial value from WDG_LOAD and continues to count in decremental mode.

If the count value of the counter reaches 0 for the second time but the CPU does not clear the watchdog interrupt, the watchdog transmits the reset signal WDG_RSTN and the counter stops counting.

You can enable or disable the watchdog by configuring WDG_CONTROL as required. That is, you can control the watchdog whether to generate interrupts and reset signals.

- When the interrupt generation function is disabled, the watchdog counter stops counting.
- When the interrupt generation function is enabled again, the watchdog counter counts starting from the preset value of WDG_LOAD instead of the last count value. Before an interrupt is generated, the initial value can be reloaded.

The count clock of the watchdog can be a crystal oscillator clock or a bus clock so different count time ranges are available.

By configuring WDG_LOCK, you can disable the operation of writing to the internal registers of the watchdog.

- Writing 0x1ACC_E551 to WDG_LOCK to enable the write permission for all the registers of the watchdog.
- Writing any other values to WDG_LOCK to disable the write permission for all the registers of the watchdog except WDG_LOCK.

This feature avoids modifications to the watchdog registers by software. Therefore, the watchdog operation is not terminated by mistake by software when an exception occurs.

In debugging mode, the watchdog is disabled automatically to avoid the intervention to the normal debugging.

3.8.4 Operating Mode

Configuring the Frequency of the Count Clock

The system supports two types of watchdog count clocks: 3 MHz crystal oscillator clock and bus clock. The two clocks are selected by configuring SC_CTRL[wdogenov].

The count time T_{WDG} of the watchdog is calculated as follows:

$$T_{WDG} = Value_{WDG_LOAD} \times \left(\frac{1}{f_{clk}} \right)$$

NOTE

The definition of each parameter in the preceding formula is as follows:

- T_{WDG} indicates the count time of the watchdog.
- $Value_{WDG_LOAD}$ indicates the initial count value of the watchdog.
- f_{clk} indicates the frequency of the watchdog count clock.

The ranges of the count time of the watchdog under different clocks are as follows:

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- When a 3 MHz crystal oscillator clock is selected, the count time ranges from 0s to 1400s.
- When a bus clock (such as a 100 MHz clock) is selected, the count time ranges from 0s to 42s.

Initializing the System

The watchdog counter stops counting after the system power-on reset. Before the system is initialized, the watchdog must be initialized and enabled. To initialize the watchdog, perform the following steps:

Step 1 Write to WDG_LOAD to set the initial count value.

Step 2 Write to WDG_CONTROL to enable the interrupt mask function and start the watchdog counter.

Step 3 Write to WDG_LOCK to lock the watchdog to avoid the watchdog settings being modified by the software by mistake.

---End

Processing an Interrupt

After an interrupt is received from the watchdog, the interrupt must be cleared in time and the initial count value must be reloaded to the watchdog to restart counting. A watchdog interrupt is processed as follows:

Step 1 Write 0x1ACC_E551 to WDG_LOCK to unlock the watchdog.

Step 2 Write to WDG_INTCLR to clear the watchdog interrupt and load the initial count value to the watchdog to restart counting.

Step 3 Write any other values rather than 0x1ACC_E551 to WDG_LOCK to lock the watchdog.

---End

Disabling the Watchdog

You can control the status of the watchdog by writing 0 or 1 to WDG_CONTROL[inten].

- 0: disabled
- 1: enabled

3.8.5 WatchDogRegister Summary

Table 3-37 describes watchdog registers.

Table 3-37 Summary of watchdog registers (base address: 0x2004_0000)

Offset Address	Register	Description	Page
0x0000	WDG_LOAD	Initial count value register	3-189
0x0004	WDG_VALUE	Current count value register	3-189
0x0008	WDG_CONTROL	Control register	3-190

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Offset Address	Register	Description	Page
0x000C	WDG_INTCLR	Interrupt clear register	3-190
0x0010	WDG_RIS	Raw interrupt register	3-191
0x0014	WDG_MIS	Masked interrupt status register	3-191
0x0018–0x0BFC	RESERVED	Reserved	-
0x0C00	WDG_LOCK	Lock register	3-191

3.8.6 Register Description

WDG_LOAD

WDG_LOAD is an initial count value register. It is used to configure the initial count value of the internal counter of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0000	WDG_LOAD	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_load																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	wdg_load	Initial count value of the watchdog counter.

WDG_VALUE

WDG_VALUE is a current count value register It is used to read the current count value of the internal counter of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0004	WDG_VALUE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdogvalue																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	wdogvalue	Current count value of the watchdog counter.

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WDG_CONTROL

WDG_CONTROL is a control register. It is used to enable or disable the watchdog and control the interrupt and reset functions of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0008	WDG_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														resen	inten
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved.
[1]	RW	resen	Output enable of the watchdog reset signal. 0: disabled 1: enabled
[0]	RW	inten	Output enable of the watchdog interrupt signal. 0: The counter stops counting, the current count value remains unchanged, and the watchdog is disabled. 1: The counter, interrupt and watchdog are enabled.

WDG_INTCLR

WDG_INTCLR is an interrupt clear register. It is used to clear watchdog interrupts so the watchdog can reload an initial value for counting. This register is write-only. When a value is written to this register, the watchdog interrupts are cleared. No written value is recorded in this register and no default reset value is defined.

Offset Address	Register Name	Total Reset Value
0x000C	WDG_INTCLR	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_intclr																															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Access	Name	Description
[31:0]	WO	wdg_intclr	Writing any value to this register clears the watchdog interrupts and enables the watchdog to reload an initial count value from WDG_LOAD to restart counting.

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WDG_RIS

WDG_RIS is a raw interrupt status register. It shows the raw interrupt status of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0010	WDG_RIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wdogris
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	wdogris	Status of the raw interrupts of the watchdog. When the count value reaches 0, this bit is set to 1. 0: No interrupt is generated. 1: An interrupt is generated.

WDG_MIS

WDG_MIS is a masked interrupt status register. It shows the masked interrupt status of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0014	WDG_MIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wdogmis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	wdogmis	Status of the masked interrupts of the watchdog. 0: No interrupt is generated or the interrupt is masked. 1: An interrupt is generated.

WDG_LOCK

WDG_LOCK is a lock register. It is used to control the write and read permissions for the watchdog registers.

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Offset Address	Register Name	Total Reset Value
0x0C00	WDG_LOCK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_lock																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdg_lock	Writing 0x1ACC_E551 to this register enables the write permission for all the registers. Writing other values disables the write permission for all the registers. When this register is read, the lock status rather than the written value of this register is returned. 0x0000_0000: The write permission is available (unlocked). 0x0000_0001: The write permission is unavailable (locked).

3.9 RTC

3.9.1 Overview

The RTC is used to display the time in real time and generate timing alarms.

3.9.2 Features

The RTC has the following features:

- Provides an internal 32-bit up counter
- Provides a 1 Hz count clock
- Supports the configurable initial count value
- Supports the configurable match value
- Supports the timeout interrupt
- Supports soft reset

3.9.3 Function Description

The RTC works based on a 32-bit up counter. The initial count value is loaded from RTC_LR. The count value is increased by 1 on the rising edge of each count clock. When the count value of RTC_LR is equal to that of RTC_MR, the RTC generates an interrupt. Then the counter continues to count incrementally on the rising edge of the next count clock.

By configuring RTC_IMSC, you can enable or disable the RTC to determine whether to generate interrupts as required. Note the following two cases:

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- When the function of generating interrupts is disabled, the RTC counter continues to count in incremental mode and no interrupts are generated. RTC_MIS shows the status of masked interrupt and RTC_RIS shows the status of raw interrupts.
- When the function of generating interrupts is enabled again, the RTC counter continues to count incrementally. When the count value of RTC_LR is equal to that of RTC_MR, the RTC generates an interrupt

The count clock of the RTC is a 1 Hz clock that is used to convert the count time into a value in the format of year, month, day, hour, minute, and second.

3.9.4 Operating Mode

3.9.4.1 Count Clock Frequency

The RTC uses a 1 Hz count clock. The maximum count time is calculated as follows:

$T_{RTC} = (2^{32} – 1) \times (1/f_{rtcclk}) = 4294967295$ seconds ≈ 49710 days

NOTE

T_{RTC} indicates the count time of the RTC, $2^{32} - 1$ indicates the maximum count value of the RTC, and f_{rtcclk} indicates the frequency of the count clock (1 Hz).

3.9.4.2 Soft Reset

You can separately soft-reset the RTC by configuring PERI_CEG57[rtc_srst_req]. After soft reset, the value of each RTC configuration register is restored to its default value. Therefore, these registers must be initialized again.

To execute soft reset, perform the following steps:

Step 1 Write 1 to PERI_CEG57[rtc_srst_req] to soft-reset the RTC.

Step 2 Write 0 to PERI_CEG57[rtc_srst_req] to clear the soft reset on the RTC.

---End

3.9.4.3 Initializing the System

The RTC counter stops counting after the system is reset during power-on. When the system is initialized, the RTC must be initialized and enabled. To initialize the RTC, perform the following steps:

Step 1 Set PERI_CRG57 [rtc_srst_req] to 0 to deassert the soft reset of the RTC.

Step 2 Set RTC_LOCK to 0x1ACCE551 to unlock the RTC.

Step 3 Set RTC_CR[rtc_start] to 1 to start the RTC counter.

Step 4 Configure RTC_MR to set the match value of the RTC.

Step 5 Configure RTC_LR to set the initial count value of the RTC.

Step 6 The RTC counts starting from the value of RTC_LR based on the 1 Hz count clock. When the count value is equal to the value of RTC_MR, the RTC determines whether to generate interrupts based on the settings of RTC_IMSC.

---End

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3.9.4.4 Processing an Interrupt

If the system receives an interrupt from the RTC, the timing time is reached. Then, the operations such as timing startup and timing shutdown are performed. The RTC counter, however, still counts in incremental mode. An RTC interrupt is processed as follows:

Step 1 Set RTC_ICR[rtc_icr] to 0b1 to clear the RTC interrupt.

Step 2 If you want to continue to set a timing time, write a new match value to RTC_MR.

---End

3.9.4.5 Disabling the RTC

After RTC_CR is configured and the RTC is enabled for counting, the RTC keeps on counting. The RTC can be disabled only when it is reset. For details about how to soft-reset the RTC, see section 3.9.4.2 "Soft Reset."

3.9.5 Register Summary

Table 3-38 describes RTC registers.

Table 3-38 Summary of RTC registers (base address: 0x2006_0000)

Offset Address	Register	Description	Page
0x000	RTC_DR	Current count value register	3-194
0x004	RTC_MR	RTC match register	3-195
0x008	RTC_LR	RTC load register	3-195
0x00C	RTC_CR	RTC enable register	3-196
0x010	RTC_IMSC	Interrupt mask register	3-196
0x014	RTC_RIS	Raw interrupt register	3-197
0x018	RTC_MIS	Masked interrupt status register	3-197
0x01C	RTC_ICR	Interrupt clear register	3-197
0x020	RTC_LOCK	RTC unlock register	3-158

3.9.6 Register Description

RTC_DR

RTC_DR is a current count value register. It is used to read the current count value of the internal counter of the RTC.

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Offset Address	Register Name	Total Reset Value
0x000	RTC_DR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rtc_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rtc_data	Current count value of the RTC counter.

RTC_MR

RTC_MR is an RTC match register. It is used to set the match value of the RTC.

Offset Address	Register Name	Total Reset Value
0x004	RTC_MR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rtc_match																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rtc_match	Match value of the RTC.

RTC_LR

RTC_LR is an RTC load register. It is used to set the initial count value of the RTC.

Offset Address	Register Name	Total Reset Value
0x008	RTC_LR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rtc_load																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rtc_load	Initial count value of the RTC.

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RTC_CR

RTC_CR is a control register. It is used to enable the RTC. If the RTC is enabled, this register can be cleared only when the system is reset. Writing this register has no effect and reading this register returns the current value.

Offset Address	Register Name	Total Reset Value
0x00C	RTC_CR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															rtc_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	rtc_start	RTC enable. 0: disabled 1: enabled

RTC_IMSC

RTC_IMSC is an interrupt mask register. It is used to show the interrupt mask status of the RTC.

Offset Address	Register Name	Total Reset Value
0x010	RTC_IMSC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															rtc_imsc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	rtc_imsc	RTC interrupt mask control. 0: masked 1: not masked

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RTC_RIS

RTC_RIS is a raw interrupt status register. It is used to show the status of the raw interrupts of the RTC.

Offset Address	Register Name	Total Reset Value
0x014	RTC_RIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															rtc_ris
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	rtc_ris	Status of raw interrupts of the RTC. 0: No interrupt is generated. 1: An interrupt is generated.

RTC_MIS

RTC_MIS is a masked interrupt status register. It is used to show the status of the masked interrupts of the RTC.

Offset Address	Register Name	Total Reset Value
0x018	RTC_MIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															rtc_mis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	rtc_mis	Status of the masked interrupts of the RTC. 0: No interrupt is generated or the interrupt is masked. 1: An interrupt is generated.

RTC_ICR

RTC_ICR is an RTC interrupt clear register. It is used to clear RTC interrupts.

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Offset Address	Register Name	Total Reset Value
0x01C	RTC_ICR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															rtc_icr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	WO	rtc_icr	RTC interrupt clear. 0: no effect 1: cleared

RTC_LOCK

RTC_LOCK is an RTC lock register. It is used to unlock the RTC.

Offset Address	Register Name	Total Reset Value
0x020	RTC_LOCK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															rtc_icr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rtc_lock	RTC unlock. 1ACCE551: The RTC is unlocked and is available. Other values: The RTC is locked and is unavailable.

3.10 Power Management and Low-Power Mode Control

3.10.1 Overview

In low-power mode, the power consumption of the chip is reduced effectively. The Hi3521 reduces its power consumption in the following low-power control modes:

- System operating mode control

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In all operating modes except the normal mode, the power consumption is reduced to some extent. You can select different operating modes according to the actual power consumption and function requirements.

- Clock gating and clock frequency adjustment

  The clock disabling function is used to disable unnecessary clocks to reduce the power consumption of the chip. In addition, the frequency of the system working clock can be adjusted. That is, when the function requirement is met, you can adjust the clock frequency to reduce the power consumption of the chip.

- Module low-power control

  When a module is idle, it can be disabled or switched to low-power mode to reduce the power consumption.

- DDR low-power control

  The power consumption of the DDRC and related pins can be controlled dynamically. You can enable this function to reduce the power consumption of the chip. You can also enable the self-refresh function of the DDR to reduce the power consumption of the entire product.

3.10.2 Operating Modes of the System

The system provides two operating modes.

- Normal operating mode: This mode maps to the normal running mode of the system.

  When the system works in normal mode, you can control the clock frequency and set the modules and DDR to low-power mode to reduce the power consumption.

- Standby operating mode: This mode maps to the slow and doze running modes of the system.
  - In standby mode, the system works at the clock with low frequency, and the clocks of most idle modules are disabled. Therefore, the power consumption is low.
  - When the system works in slow or doze mode, you can power off the power supplies of idle modules to reduce the power consumption.

  The mode can be switched by configuring the system controller. For details, see section 3.4 "System Controller."

3.10.3 Clock Gating and Clock Frequency Adjustment

The system supports clock gating of each module. When a module is idle, its clock can be disabled to reduce the power consumption of the chip. For details about the process, see the description in the section of "clock gating" of each module.

In normal mode, the system can adjust its working frequency to reduce the power consumption of the chip. To adjust the system working frequency, perform the following steps:

- Disable the service module to prevent it from accessing the DDR.
- Enable the system to run in the off-chip memory.

When DDRC_SREFCTRL[sr_seq] is set to a valid value, the DDRC forces the DDRn SDRAM to enter the self-refresh mode.

Step 1 Set the value of SC_PLLCTRL[27:3] to the stable time of the PLL.

Step 2 Configure PERI_CRG0 and PERI_CRG1 to control the clock divider of the PLL

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Step 3 Wait a moment and configure DDRC_SREFCTRL to enable the DDRC to exit the self-refresh mode based on the configuration requirements of the DDRC.

Step 4 The program starts to run in the DDR.

---End

The working frequencies of some modules can also be adjusted separately. This reduces the power consumption of the system further. For details about the clock source of each module, see section 3.2.3 "Clock Configuration."

3.10.4 Module Low-Power Control

Most modules including USB 2.0 host, SATA, Video DAC, and PLL modules support low-power operating modes. For details, see the descriptions of the system controller, VDP, and clocks.

- Low-power control for the USB host module:
  - Disable the USB 2.0 host clock by setting PERI_CRG46 bit[7] to 0.
  - Powered off the USB PHY by setting PERIPHCTRL21 bit[22] to 1.
- Low-power control for the SATA module
  - Disable the clock of SATA port 0 or port 1 by setting PERI_CRG45 bit[9] or PERI_CRG45 bit[8] to 0 respectively.
  - Power off the SATA PHY by setting PERIPHCTRL47 bit[2] to 1.
- When the video DAC is not used, you can:
  - Power off the VOU SD DAC by setting PERI_CRG13 bit[7] to 1.
  - Power off the VOU HD DAC by setting PERI_CRG13 bit[6] to 1.
- The PLL also supports the low-power mode. If the PLL is not used, it can be disabled to switch the system to low-power mode.
  - If the APLL is not used, you can set PERI_CRG1[apll_pd] to 0 to disable it. Then the APLL enters the low-power mode.
  - If VPLL0 is not used, you can set PERI_CRG3[vpll0_pd] to 0 to disable it. Then VPLL0 enters the low-power mode.
  - If VPLL2 is not used, you can set PERI_CRG7[vpll2_pd] to 0 to disable it. Then VPLL2 enters the low-power mode.
  - If the EPLL is not used, you can set PERI_CRG9[epll_pd] to 0 to disable it. Then the EPLL enters the low-power mode.

The modules such as the slave VICAP, VENC, and VDH can be separately powered off and woken up. For details, see the descriptions of system controller registers.

- Low-power control for the VICAP
  - Disable the clock of the VICAP by setting PERI_CRG11 bit[31:28] to 0 and PERI_CRG11 bit[23:20] to 0.
  - Power off the VICAP by setting PERIPHCTRL2 bit[9] to 1 and PERIPHCTRL2 bit[8] to 0; query the power status of the VICAP by reading PERISTAT bit[4].
- Low-power control for the VENC (VEDU) module
  - Disable the clock of VEDU by setting PERI_CRG16 bit[1].

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  - Power off VENC or VEDU by setting PERIPHCTRL2 bit[11] to 1 and PERIPHCTRL2 bit[10] to 0; query the power status of VENC0 or VEDU0 by reading PERISTAT bit[5].
- Low-power control for the VDH module
  - Disable the clocks of VDH by setting PERI_CRG20 bit[1].
  - Power off VDH by setting PERIPHCTRL2 bit[19] to 1 and PERIPHCTRL2 bit[18] to 0; query the power status of VDH by reading PERISTAT bit[9].
- Low-power control for the TOE module
  - Disable the TOE clock by setting PERI_CRG51 bit[1] to 0.
  - Power off MAC by setting PERIPHCTRL44 bit[9] and PERIPHCTRL44 bit[8] to 1; query the power status of the MAC by reading PERIPHCTRL45 bit[1].

The BOOTROM module provides internal RAM/ROM power-off mechanisms. For details, see the descriptions of system controller registers.

Low-power control for the BOOTROM module

- Power off the internal ROM of the BOOTROM module by setting PERIPHCTRL2 bit[0] to 1.
- Power off the first RAM of the BOOTROM module by setting PERIPHCTRL2 bit[2] to 1.
- Power off the second RAM of the BOOTROM module by setting PERIPHCTRL2 bit[4] to 1.
- Power off the third RAM of the BOOTROM module by setting PERIPHCTRL2 bit[6] to 1.

3.10.5 DDR Low-Power Control

For details about the low-power control mode of the DDRC, see the description of "Configuring the Low-Power Mode" in section 4.1.4 "Operating Mode."

3.11 Processor Subsystem

3.11.1 ARM Cortex-A9 Processor

The Hi3521 uses the ARM CortexA-9 processor with a core. This processor has the following features:

- Supports a maximum of 930 MHz working frequency.
- Supports L1 cache including 32 KB I-cache and 32 KB D-cache.
- Supports 256 KB L2 cache. The frequencies of the L2 cache and processor are the same, and the ratio of the frequency of the L2 cache to the frequency of the AXI bus is configurable. Table 3-39 describes the ratio of the frequency of the CPU to the frequency of the AXI bus.

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Table 3-39 Ratio of the frequency of the CPU to the frequency of the AXI bus

Ratio of the Frequency of the L2 Cache to the Frequency of the AXI Bus		Description
310MHz for the AXI bus	3:1	930 MHz for the L2 cache, and 310 MHz for the AXI bus
	2:1	620 MHz for the L2 cache, and 310 MHz for the AXI bus
	1:1	310 MHz for the L2 cache, and 310 MHz for the AXI bus

- Integrates with a GIC supporting 128 interrupt sources.
- Uses scrambling dual-issue structure based on a single thread and 2.5 DMIPS.
- Uses 8-stage pipelines.
- Provides a memory management unit (MMU).
- Supports Vxworks or Linux operating system.
- Supports the branch prediction with up to 95% precision based on the global history buffer (GHB).
- Supports the JTAG debugging interface.

3.11.2 L2 Cache

The L2 cache has the following features:

- Supports the size of 256 KB.
- Works based on the physical address and physical tag.
- Supports cache lockdown in C format. The instruction and data operations are classified based on the lockdown status. The locked RAM space can serve as the tightly coupled memory (TCM) of the processor.
- Provides fixed cache line (32 bytes, 8 words, or 256 bits) and supports the write operation by byte.
- Supports write-back, write-through, read-allocate, and write-allocate operations. The actual mode depends on the page table.
- Supports the access to the tag RAM and data RAM using pipeline. A tag RAM query and a data RAM read/write can be performed within a clock cycle.
- Provides three line fill buffers (LFBs). Each buffer caches the data allocated from the memory and submits the data to the L2 memory when a cache line is filled with data.
- Provides two line read buffers (LRBs) for each slave interface. After the cache is hit, an L1 cache line is provided.
- Provides three eviction buffers (EBs). Each buffer caches the data that is replaced from L2 cache and will be written to the primary memory.
- Provides three write buffers (WBs). Each buffer caches the data that is written from the L1 cache to the memory and L2 cache. Such buffer includes an address space and a 256-bit data space and allows the data in a line to be written to a data slot.
- Supports forcible write-allocate function that enables data to be allocated forcibly in each cacheable write operation.

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- Supports shared mode. By default, the shared operation is cacheable but cannot be allocated.
- Supports keyword priority.
- Supports atomicity synchronization.
- Supports pseudo random replacement algorithm that is relevant to the actual lockdown status. That is, the algorithm is invalid in the case of direct connection.
- Provides the exclusive cache function that can be enabled using software. When the function is enabled, you can disable the presence of data in L1 and L2 at the same time.
- Supports clean and invalidate operations by way, way+index, or address.
- Supports cache memory ECC check. Both tag RAM and data RAM support 1-bit correction.
- Supports cache disabling. If this function is enabled, the cache is bypassed, and all the operations on L1 are transferred to the memory transparently.
- Supports L2 cache performance statistics. The cache provides the statistics on the cache access events, write-back events, loss events, and loss and wait events.
- Collects statistics on the internal events of the cluster and configures the internal special signals of the cluster.

NOTE

For the principles of the lockdown function in C format, see the *ARM Architecture Reference Manual*.

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Contents

4 Memory Interfaces 4-1
4.1 DDRC 4-1
4.1.1 Overview 4-1
4.1.2 Features 4-1
4.1.3 Function Description 4-1
4.1.4 Operating Mode 4-10
4.1.5 Register Summary 4-15
4.1.6 Register Description 4-18
4.2 NAND Flash Controller 4-61
4.2.1 Overview 4-61
4.2.2 Features 4-61
4.2.3 Function Description 4-62
4.2.4 Operating Mode 4-65
4.2.5 Precautions 4-74
4.2.6 NANDCRegister Summary 4-75
4.2.7 Register Description 4-76
4.3 SPI Flash Controller 4-100
4.3.1 Overview 4-100
4.3.2 Features 4-101
4.3.3 Function Description 4-101
4.3.4 Working Flowchart 4-107
4.3.5 Register Summary 4-110
4.3.6 Register Description 4-112

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Figures

Figure 4-1 Diagram of connecting a DDRC to two DDRn SDRAMs in 32-bit mode 4-4

Figure 4-2 Diagram of connecting a DDRC to one DDRn SDRAM in 16-bit mode 4-5

Figure 4-3 Diagram of connecting the reference resistors to the DDR IOs 4-14

Figure 4-4 Block diagram of NANDC interfaces 4-63

Figure 4-5 Typical timing when the NANDC reads the data of a page size from the NAND flash 4-64

Figure 4-6 Timing when the NANDC starts programming 4-64

Figure 4-7 Data storage structure of the NAND flash with the page size of 2 KB (2048 + 64 bytes) in 1-bit ECC mode 4-71

Figure 4-8 (4096 + 56)-byte data structure of the driver in 1-bit ECC mode 4-71

Figure 4-9 Data structure of the NAND flash in 1-bit ECC mode 4-71

Figure 4-10 (4096 + 48)-byte data structure of the driver in 4-bit ECC mode 4-72

Figure 4-11 (4096 + 128)-byte data structure of the NAND flash in 4-bit ECC mode 4-72

Figure 4-12 (4096 + 32)-byte data structure of the driver in 24-bit ECC mode 4-72

Figure 4-13 (4096 + 200)-byte data structure of the NAND flash in 24-bit ECC mode (n = 8) 4-72

Figure 4-14 (8192 + 32)-byte data structure of the driver in 24-bit ECC mode 4-73

Figure 4-15 (8192 + 368)-byte data structure of the NAND flash in 24-bit ECC mode (n = 4) 4-73

Figure 4-16 Timing of the standard SPI (write) 4-101

Figure 4-17 Timing of the standard SPI (read) 4-102

Figure 4-18 Timing of the dual input/output SPI 4-102

Figure 4-19 Timing in dual I/O SPI mode 4-103

Figure 4-20 Timing in dual I/O SPI mode 4-103

Figure 4-21 Timing of the quad input/output SPI 4-104

Figure 4-22 Timing in quad I/O SPI mode 4-104

Figure 4-23 Timing of the full quad I/OSPI 4-105

Figure 4-24 SPI output timing 4-107

Figure 4-25 SPI write protection timing 4-107

Figure 4-26 Process of reading the flash memory by configuring registers in query mode 4-108

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Figure 4-27 Process of writing to the flash memory by configuring registers in interrupt mode.....4-109

Figure 4-28 Process of reading and writing to the flash memory directly by using the bus.....4-110

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Tables

Table 4-1 DDR2 SDRAMs supported by the DDRC 4-2
Table 4-2 DDR3 SDRAMs supported by the DDRC 4-3
Table 4-3 Command truth values of the DDRC 4-6
Table 4-4 DDRC address mapping in 32–bit mode 4-8
Table 4-5 DDRC address mapping in 16–bit mode 4-9
Table 4-6 Transmit impedance 4-14
Table 4-7 Receive impedance 4-14
Table 4-8 Variables in the offset addresses of registers 4-15
Table 4-9 Summary of the DDRC registers (base address: 0x2011_0000) 4-15
Table 4-10 Mapping modes of pins 4-65
Table 4-11 Boot configuration pins 4-68
Table 4-12 Addresses of the K9F2G08U0M 4-69
Table 4-13 Addresses of the K9GAG08X0M 4-70
Table 4-14 Common commands for operating the NAND flash 4-70
Table 4-15 Summary of NANDC registers (base address; 0x1000_0000) 4-75
Table 4-16 Summary of the SFC registers (base address: 0x1001_0000) 4-110
Table 4-17 Mode of accessing the flash memory based on the register configurations 4-111

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4 Memory Interfaces

4.1 DDRC

4.1.1 Overview

The DDR2/DDR3 SDRAM controller (DDRC) controls the access to the DDR2 SDRAM or DDR3 SDRAM. In the following sections, DDR2/DDR3 SDRAM is expressed as DDRn SDRAM.

NOTE

The Hi3521 provides a DDRC that supports 32-bit or 16-bit DDRs.

4.1.2 Features

The DDRC has the following features:

- Provides one DDRn SDRAM CS space. The data bus width for the DDRn SDRAM can be configured to the 32-bit or 16-bit mode. The address bus width for the DDRn SDRAM can be configured to a maximum of 15 bits.
- Supports a maximum of 1 GB storage space in 32-bit mode and 512MB in 16-bit mode.
- Supports the 620 MHz DDRn SDRAM bus.
- Supports various low-power modes for the DDRn SDRAM including power down and self refresh.
- Supports burst4 and burst8 transfer modes for the DDR2 SDRAM and burst8 transfer mode for the DDR3 SDRAM.

4.1.3 Function Description

4.1.3.1 Application Block Diagram

By using the DDRC, the master devices such as the CPU of the system-on-chip (SoC) can access the external DDRn SDRAM. After the timing parameter registers of the DDRC are configured by using the CPU, the DDRC supports the DDR2 SDRAM and DDR3 SDRAM complying with the JEDEC (JESD79) standard. Table 4-1 lists the mainstream DDR2 SDRAMs supported by the DDRC. The descriptions in Table 4-1 are based on the working frequencies of DDR2 SDRAMs. The restrictions such as the capacity are not taken into account.

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Table 4-1 DDR2 SDRAMs supported by the DDRC

Vendor	200 MHz	333 MHz	400 MHz
JESD79 (DDR2 Standard)	DDR2-400 DDR2-533 DDR2-667 DDR2-800	DDR2-667 DDR2-800	DDR2-800
Micron	-5E DDR2-400 -37E DDR2-533 -3 DDR2-667 -3E DDR2-667 -25 DDR2-800 -25E DDR2-800	-3 DDR2-667 -3E DDR2-667 -25 DDR2-800 -25E DDR2-800	-25 DDR2-800 -25E DDR2-800
ELPIDA	-4A DDR2-400 -5C DDR2-533 -6E DDR2-667 -6C DDR2-667 -8E DDR2-800	-6E DDR2-667 -6C DDR2-667 -8E DDR2-800	-8E DDR2-800
Hynix	-E3 DDR2-400 -C4 DDR2-533 -Y4 DDR2-667 -Y5 DDR2-667 -S5 DDR2-800 -S6 DDR2-800	-Y4 DDR2-667 -Y5 DDR2-667 -S5 DDR2-800 -S6 DDR2-800	-S5 DDR2-800 -S6 DDR2-800
Samsung	-CC DDR2-400 -D5 DDR2-533 -E6 DDR2-667 -E7 DDR2-800	-E6 DDR2-667 -E7 DDR2-800	-E7 DDR2-800

NOTE

- The DDRC supports the SDRAMs complying with the JESD79 standard. In different operating modes, the DDRC supports only the SDRAMs whose frequencies are higher than or equal to its working frequency. You can refer to this feature to select the SDRAMs provided by other vendors.
- You need to select DDR2 SDRAMs provided by each vendor according to their working frequencies. In practice, the DDR2 SDRAMs with the same working frequency may differ from each other in capacity or bit width. A DDR2 SDRAM is supported by the DDRC as long as its working frequency is listed in Table 4-1. The capacity and bit width of a DDR2 SDRAM are selected based on the actual application scenario of the chip.

Table 4-2 lists the DDR3 SDRAMs supported by the DDRC.

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Table 4-2 DDR3 SDRAMs supported by the DDRC

Vendor	400 MHz	533 MHz	800 MHz
JESD79 (DDR3 Standard)	DDR3-800 DDR3-1066 DDR3-1333	DDR3-800 DDR3-1066 DDR3-1333	None

NOTE

If the working frequency of the DDRC is 400 MHz, the frequencies of all the DDR3s can be decreased to 400 MHz.

The supported memory types are based on the JEDEC standard.

The DDRC supports two interconnection modes: 32-bit mode and 16-bit mode. In 32-bit mode, the DDRC connects to two 16-bit or four 8-bit DDRn SDRAMs. The following is an example using two 16-bit DDRn SDRAMs. Figure 4-1 shows the diagram of connecting a DDRC to two 16-bit DDRn SDRAMs.

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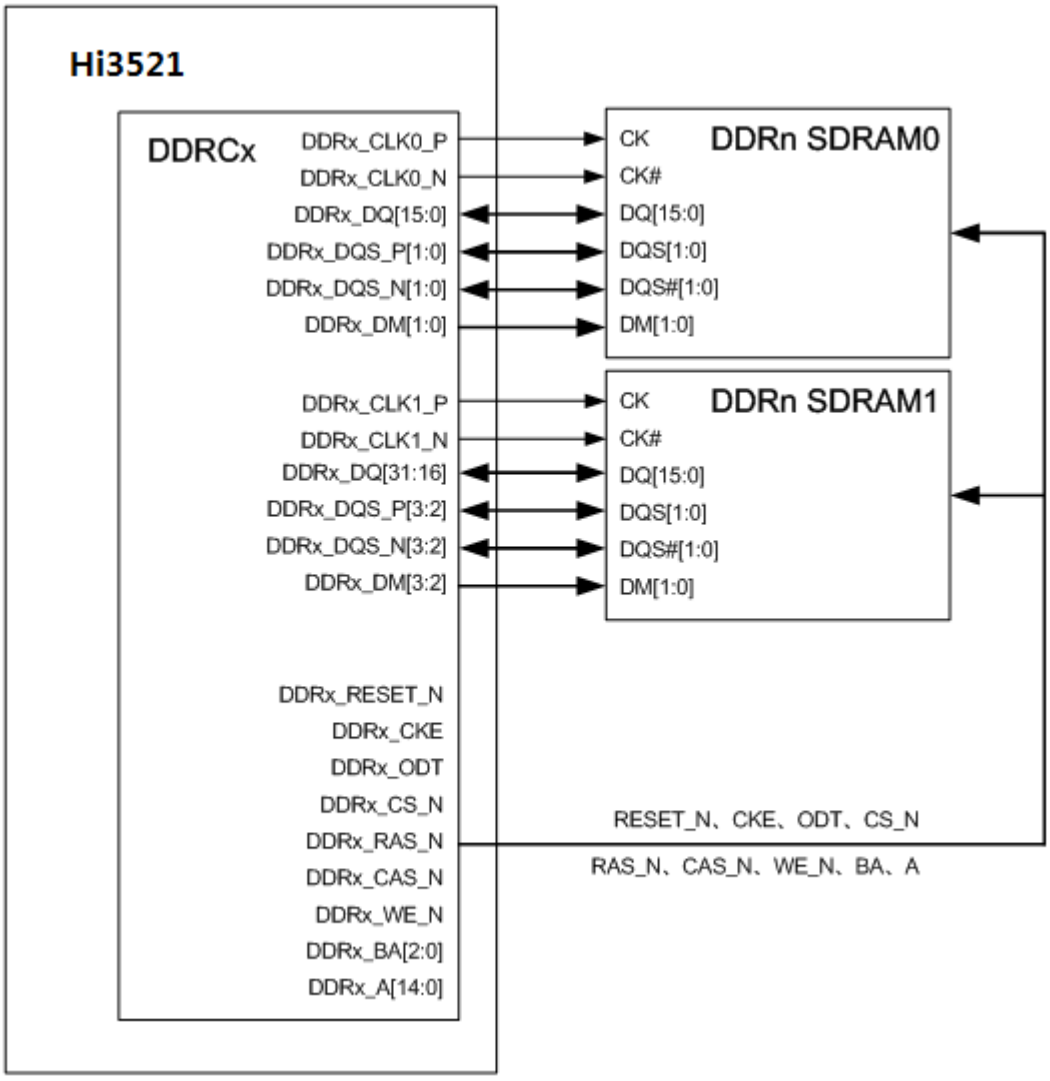
Figure 4-1 Diagram of connecting a DDRC to two DDRn SDRAMs in 32-bit mode



Description:
The letter *x* in DDRCx or DDRx indicates the DDR controller ID and its value is 0 or 1.
DDRn SDRAMx is a 16-bit memory.
The command control signals of the DDRC include DDRx_CKE, DDRx_RESET_N, DDRx_ODT, DDRx_CS_N, DDRx_RAS_N, DDRx_CAS_N, DDRx_WE_N, DDRx_BA[2:0] and DDRx_A[14:0]. These signals connect to the command control signals of the DDRn SDRAMx. That is, the command control bus of the DDRC is connected in one-driven-two mode.
If the capacity of a DDR2 SDRAM is smaller than 1 Gbit, the output address signal DDRx_BA[2] of the DDRC is floated.
DDRx_RESET_N is floated in DDR2 mode.

In 16-bit mode, the DDRC connects to one 16-bit or two 8-bit DDRn SDRAMs. The following is an example using one 16-bit DDRn SDRAM. Figure 4-2 shows the diagram of connecting a DDRC to one 16-bit DDDRn SDRAM.

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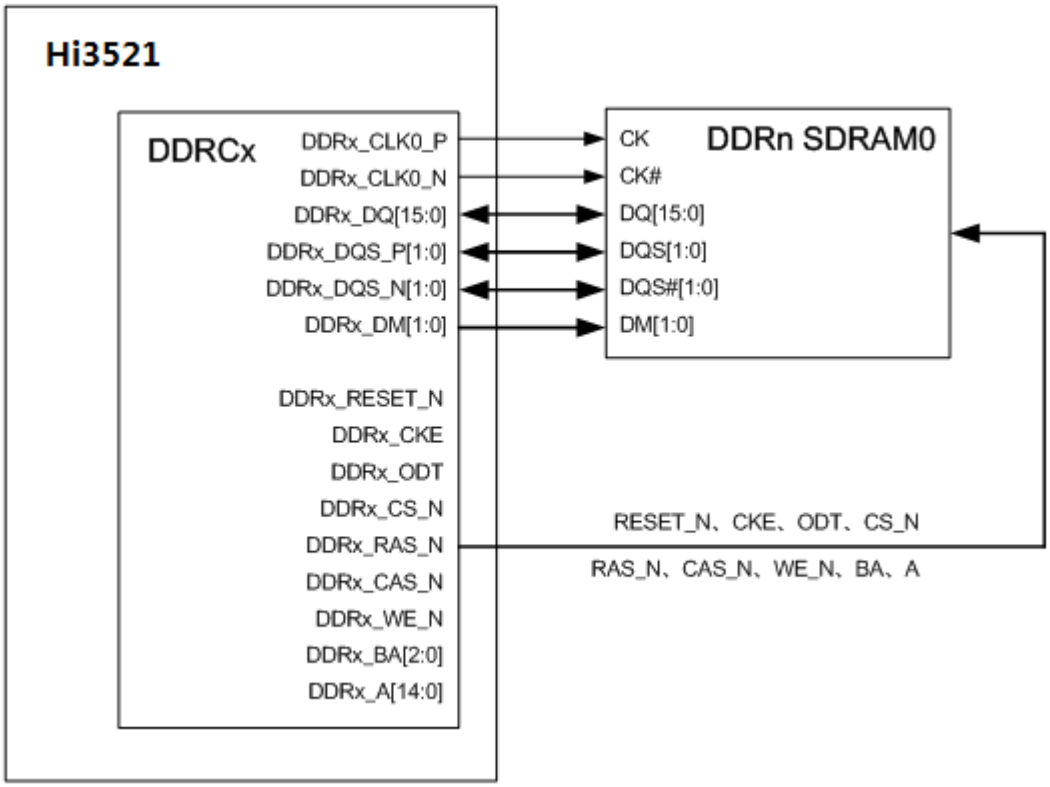
Figure 4-2 Diagram of connecting a DDRC to one DDRn SDRAM in 16-bit mode



Description:
The letter *x* in DDRCx or DDRx is the DDR controller ID and its value is 0 or 1.
DDRn SDRAMx is a 16-bit memory.
The command control signals of the DDRC include DDRx_CKE, DDRx_RESET_N, DDRx_ODT, DDRx_CS_N, DDRx_RAS_N, DDRx_CAS_N, DDRx_WE_N, DDRx_BA[2:0] and DDRx_A[14:0]. These signals connect to the command control signals of the DDRn SDRAM. That is, the command control bus of the DDRC is connected in one-driven-one mode.
If the capacity of a DDR2 SDRAM is smaller than 1 Gbit, the output address signal DDRx_BA[2] of the DDRC is floated.
In 16-bit mode, the signals DDRx_DQS_P[3:2], DDRx_DQS_N[3:2], DDRx_DQ[31:16], and DDRx_DM[3:2] are floated.
DDRx_RESET_N is floated in DDR2 mode.

4.1.3.2 Function Principle

As the timings of the DDRC interface comply with the JESD79 standard, the DDRC can access the data of the DDRn SDRAM and control the status of the DDRn SDRAM by transmitting the command words of the DDRn SDRAM. The DDRC can also read and write the DDRn SDRAM, automatically refresh the DDRn SDRAM, and control the power consumption of the DDRn SDRAM.

Command Truth Value Table

The DDRC can read, write, and control the command words of the DDRn SDRAM. Table 4-3 lists the command truth values of the DDRC.

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Table 4-3 Command truth values of the DDRC

FUNCTION	DDRn_CKE	DDRn_CSN	DDRn_RASN	DDRn_CASN	DDRn_WEN	DDRn_ADR			DDRn_BA
						11	AP(10)	9:0	
DESELECT	H	H	X	X	X	X	X	X	X
ACTIVE	H	L	L	H	H	V	V	V	V
READ	H	L	H	L	H	V	V	V	V
WRITE	H	L	H	L	L	V	V	V	V
PRECHARGE	H	L	L	H	L	X	L	X	V
PRECHARGE ALL	H	L	L	H	L	X	H	X	X
AUTO REFRESH	H	L	L	L	H	X	X	X	X
SELF REFRESH	L	L	L	L	H	X	X	X	X
MODE REGISTER SET	H	L	L	L	L	V	V	V	V
ZQCL	H	L	H	H	L	X	H	X	X
ZQCS	H	L	H	H	L	X	L	X	X

H: high level; L: low level; V: valid; X: ignored.

ZQ calibration long (ZQCL): start a ZQ calibration on the DDR3 SDRAM when it is initialized during power on.

ZQ calibration short (ZQCS): start a calibration on the DDR3 SDRAM when its ambient environment is changed.

Auto Refresh

When DDRC_TIMING2[taref] is set to a non-zero value, the DDRC refreshes the DDRn SDRAM by generating a periodic auto refresh command automatically At normal temperature, the DDR2 SDRAM must be auto-refreshed for 8192 times within 64 ms. That is, the auto-refresh cycle is 7.8 µs. The relationship between the configured value (Taref) of DDRC_TIMING2 [taref] and the auto-refresh cycle T (T = 7.8 µs or 3.9 µs) is as follows:

Taref ≤ T/(16 x DDR clock cycle)

When DDRC_TIMING2[taref] is configured, the internal counter of the DDRC loads the taref value automatically and then counts in decremental mode. When the count value reaches 0, the DDRC initiates an auto-refresh operation and the counter reloads the taref value to count.

Low-Power Management

The DDRC supports two types of low-power management: common low-power mode and auto-refresh low-power mode.

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When the system is idle (the DDR is not read or written over the DDRC bus interface for a period), the DDRn SDRAM enters the common low-power mode automatically.

When the system needs to be switched to the standby mode, you can force the DDRn SDRAM to enter the self-refresh low-power mode by configuring

DDRC_SREFCTRL[sr_req]. In this mode, the power consumption of the DDRn SDRAM is minimized, but the data in the DDRn SDRAM is retained. In this case, the system cannot access the DDRn SDRAM.

Arbitration Mechanism

The DDRC uses the priority scheduling algorithm. That is, the DDRC adds priority attributes to bus commands by configuring DDRC_QOS[pri], and schedules the commands based on the priority attributes. In this way, the DDR2 SDRAM is accessed in a high-effective manner. The DDRC can also add delay attributes to bus commands by configuring DDRC_QOS[qos_en] and DDRC_QOSx[qos], and ensure delay response to the commands based on the delay priority scheduling algorithm. The DDRC adds the traffic control attributes to bus interfaces by configuring DDRC_FLUX[flux_port_en] and DDRC_FLUX[flux]. When the delay time is not consumed, traffic of each bus interface is allocated to ensure that the bandwidth of each interface when the DDRC is accessed in busy hours.

Address Mapping Mode

The DDRC can convert the access address of the system bus into that of the DDRn SDRAM. By configuring DDRC_RNKCFG[mem_map], DDRC_RNKCFG[mem_row], and DDRC_RNKCFG[mem_col], the DDRC converts the system bus address into the address of the DDRn SDRAM based on the address mapping algorithm.

The following example describes the mapping algorithm of the system bus address and the address of the DDRn SDRAM. Assume that the system bus address is BUSADR[28:0], the valid address is BUSADR[m – 1:0], and the address of the DDRn SDRAM is DDRADR[13:0]. When DDRADR[13:0] serves as the row address, its valid address is DDRROW[x – 1:0]; when it serves as the column address, its valid address is DDRCOL[y – 1:0]. In addition, the bank address of the DDR is DDRBA[z – 1:0] and the width of the storage data bus of the DDRC is DW. In this case, the address mappings are as follows:

- When DDRC_RNKCFG[mem_map] is set to 2b00, the mapping mode of the row-bank-column (RBC) is as follows:

  BUSADR[m – 1: 0] = {DDRROW[x – 1: 0],DDRBA[z – 1:0],DDRCOL[y – 1:0],DW{b0}}
- When DDRC_RNKCFG[mem_map] is set to 2b01, the mapping mode of the RBC is as follows:

  BUSADR[m – 1:0] = {DDR_BA[z – 1:0],DDRROW[x – 1:0],DDRCOL[y – 1:0],DW{b0}}

In the preceding expressions, the condition of the equation m = x + y + z + DW is true.

When the DDRC is in 32-bit mode, the value of DW is 2.

Table 4-4 describes the mapping of the system bus address and the DDRn SDRAM address when DDRC_RNKCFG[mem_map] is set to 2b00 and A10 acts as the AP function bit of the DDR.

To be specific, Table 4-4 describes the address mapping in RBC mode. That is, the address is mapped in RBC mode based on the preceding expressions.

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Table 4-4 DDRC address mapping in 32–bit mode

Memory Type	Row Address Width	Column Address Width	DDR BA			Row Address or Column Address	DDR ADR						
Mbitxbw			2	1	0		13	12	11	10/AP	9	8	[7:0]
256 Mbits 4 banks													
16x16	13	9	None	12	11	Row address	None	25	24	23	22	21	[20:13]
						Column address	None	None	None	AP	None	10	[9:2]
512 Mbits 4 banks													
32x16	13	10	Noen	13	12	Row address	None	26	25	24	23	22	[21:14]
						Column address	None	None	NONE	AP	11	10	[9:2]
1024 Mbits 8 banks													
64x16	13	10	14	13	12	Row address	None	27	26	25	24	23	[22:15]
						Column address	None	None	None	AP	11	10	[9:2]
2048 Mbits 8 banks													
128x16	14	10	14	13	12	Row address	28	27	26	25	24	23	[22:15]
						Column address	None	None	None	AP	11	10	[9:2]

When the DDRC is in 16-bit mode, the value of DW is 1.

Table 4-5 describes the mapping of the system bus address and the DDRn SDRAM address when DDRC_RNKCFG[mem_map] is set to 2b00 and A10 acts as the AP function bit of the DDR.

To be specific, Table 4-5 describes the address mapping in RBC mode. That is, the address is mapped in RBC mode based on the preceding expressions.

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Table 4-5 DDRC address mapping in 16–bit mode

Memory Type	Row Address Width	Column Address Width	DDR BA			Row Address or Column Address	DDR ADR						
Mbitxbw			2	1	0		13	12	11	10/AP	9	8	[7:0]
256 Mbits 4 banks													
16x16	13	9	None	11	10	Row address	None	24	23	22	21	20	[19:12]
						Column address	None	None	None	AP	None	9	[8:1]
512 Mbits 4 banks													
32x16	13	10	None	12	11	Row address	None	25	24	23	22	21	[20:13]
						Column address	None	None	None	AP	10	9	[8:1]
1024 Mbits 8 bank													
64x16	13	10	13	12	11	Row address	None	26	25	24	23	22	[21:14]
						Column address	None	None	None	AP	10	9	[8:1]
2048 Mbits 8 bank													
128x16	14	10	13	12	11	Row address	27	26	25	24	23	22	[21:14]
						Column address	None	None	None	AP	10	9	[8:1]

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4.1.4 Operating Mode

4.1.4.1 Clock Gating

After the system enters the low-power mode, the working clock of the DDRC can be disabled. Before the system restores to the normal mode, the working clock of the DDRC must be enabled.

To disable the working clock after the DDRC enters the low-power mode, perform the following steps:

Step 1 Enable the system to run in the flash memory or the TCM.

Set

Step 2 DDRC_SREFCTRL[sr_req] to 1 to request to enter the self-refresh mode.

Step 3 Query DDRC_STATUS[in_sr] until its value is 1. It indicates that the DDRC enters the low-power mode.

Step 4 Disable the DDR clock by setting DDRC_IOCFG[odis_clk] to 0x7.

Step 5 Disable the DDRC clock.

Step 6 Enter the low-power mode.

---End

To enable the working clock after the DDRC exits the low-power mode, perform the following steps:

Step 1 Enable the DDRC clock when the system runs in normal mode.

Step 2 Enable the DDR clock by setting DDRC_IOCFG[odis_clk] to 0x4.

Step 3 Wait 50 μs until the delay locked loop (DLL) is locked.

Set

Step 4 DDRC_SREFCTRL[sr_req] to 0 to request to exit the self-refresh mode.

Step 5 Query DDRC_STATUS[in_sr] until its value is 0. It indicates that the DDRC exits the low-power mode.

Step 6 The system accesses the DDR properly.

---End

4.1.4.2 Soft Reset

The DDRC does not support separate soft reset. It can be reset only by a global soft reset. After reset, the DDRn SDRAM must be reinitialized according to the following initialization processes.

4.1.4.3 Initializing the DDR2 SDRAM

After power-on, the system can access the DDR2 SDRAM only when the DDR2 SDRAM is initialized. Before initializing the DDR2 SDRAM, note the following points:

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- Power on the DDR2 SDRAM according to the JEDEC standard. That is, you must power on VDD, VDDQ, VREF, and VTT in sequence.
- Initialize the DDR2 SDRAM after the system runs in normal mode.

In the DDRC 32-bit mode, assume the memory consists of two 1 Gbit DDR2 SDRAMs with 16-bit width. To initialize the DDRC, perform the following steps:

Step 1 Wait more than 200 µs.

Step 2 Set DDRC_IOCFG to 0x427, and configure the operating mode, matched impedance, and signal driven mode of the IO.

Step 3 Set the value of DDRC_RNKCFG to 0x122 based on the capacity of a single DDR. Set the mapping mode of the bus address to R-B-C-DW, set AP to A10, set the width of the column address to 10, and set the width of the row address to 13.

Step 4 Set DDRC_PHYSRST to 0x0 and set DDRC_CDLLCFG and DDRC_QDLLCFG0–3 to 0x52 to reset the DDR PHY and DLL.

Step 5 Wait 50 µs.

Step 6 Set DDRC_PHYSRST to 0x1 and set DDRC_CDLLCFG and DDRC_QDLLCFG0–3 to 0x56 to deassert the reset on the DDR PHY and DLL.

Step 7 Wait more than 3 µs.

Step 8 Set DDRC_TIMING2[taref] to 0x000 to disable self-refresh.

Set

Step 9 DDRC_SREFCTRL to 0x0 to exit from the self-refresh mode.

Step 10 Wait more than 1 µs.

Step 11 Based on the working frequency and requirements of the DDR2 SDRAM, configure the DDRC_EMRS01 and DDRC_EMRS23 registers to set the column address signal (CAS) latency, write recovery latency, burst length, output driver impedance, and input ODT impedance of the DDR2 SDRAM.

NOTE

- The values of the CL and DDRC_TIMING1[tcl] must be the same.
- DDRC_EMRS01 maps to the mode register (MRS) and extended mode register 1 (EMRS1) of the DDR2 SDRAM. When configuring DDRC_EMRS01, you need to refer to the description of A15–A0 of the mode register in the DDR2 SDRAM manual. The actual valid bits are A13 to A0. You do not need to configure the upper three bits A18−A16 (bank address) of the mode register. Note that the bank address for some DDRn SDRAMs corresponds to bits A17−A15.
- **Before configuring EMRS1 of the DDR2 SDRAM, ensure that RDQS and DQSN are disabled.**

Step 12 Set DDRC_CONFIG0 to 0x8000_0510 and set DDRC_CONFIG1 to 0x784 based on the type and storage space of the DDR2 SDRAM. This indicates that the DDRC is in 32-bit DDR2 SDRAM mode.

NOTE

Note: The low power mode is disabled by default after power-on reset. During initialization, the functions of automatically enabling the low-power mode and disabling clocks must be disabled. In normal mode, you are advised to enable the low-power control function to reduce the power consumption.

Step 13 Set the memory space base address register DDRC_BASEADDR to 0x8000_0000.

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Step 14 Configure DDRC_TIMING0–DDRC_TIMING3 based on the working frequency and the DDR components. The CL value must be consistent with the configured value of the DDRC_EMRS01 register.

Step 15 Set DDRC_DTRCTRL to 0x0F00_0503 to enable initialization automatic training mode.

Step 16 Set DDRC_ODTCFG[wodt0] to 0x1 and DDRC_ODTCFG [rodt0] to 0x0.

Step 17 Set DDRC_PHYCFG to 0x2.

Step 18 Set DDRC_INITCTRL to 0x1 to start the initialization.

Step 19 Wait until the value of DDRC_INITCTRL becomes 0.

---End

After the preceding steps are complete, the DDR2 SDRAM works properly.

4.1.4.4 Initializing the DDR3 SDRAM

After power on, the system can access the DDR3 SDRAM only when the DDR3 SDRAM is initialized. Before initializing the DDR3 SDRAM, note the following points:

- Power on the DDR3 SDRAM by following the JEDEC standard. That is, you must power on VDD, VDDQ, VREF, and VTT in sequence.
- Initialize the DDR3 SDRAM after the system runs in normal mode.

In the DDRC 32-bit mode, assume the memory consists of two 1 Gbit DDR3 SDRAMs with 16-bit width. To initialize the DDRC, perform the following steps:

Step 1 Wait more than 200 µs.

Step 2 Set DDRC_IOCFG to 0x467, and configure the operating mode, matched impedance, and signal driven mode of the IO.

Step 3 Set the value of DDRC_RNKCFG to 0x122 based on the capacity of a single DDR. Set the mapping mode of the bus address to R-B-C-DW, set AP to A10, set the width of the column address to 10, and set the width of the row address to 13.

Step 4 Set DDRC_PHYSRST to 0x0 and set DDRC_CDLLCFG and DDRC_QDLLCFG0–3 to 0x52 to reset the DDR PHY and DLL.

Step 5 Wait 50 µs.

Step 6 .Set DDRC_PHYSRST to 0x1 and set DDRC_CDLLCFG and DDRC_QDLLCFG0–3 to 0x56 to deassert the reset on the DDR PHY and DLL.

Step 7 Wait more than 3 µs.

Step 8 Set DDRC_TIMING2[taref] to 0x000 to disable self-refresh.

Step 9 Set DDRC_CTRL to 0x1 and configure DDR3 SDRAM to exit from the reset status.

Step 10 Wait more than 500 µs.

Set

Step 11 DDRC_SREFCTRL to 0x0 to exit from the self-refresh mode.

Step 12 Wait more than 1 µs.

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Step 13 Based on the working frequency and requirements of the DDR2 SDRAM, configure the DDRC_EMRS01 and DDRC_EMRS23 registers to set the CAS latency, CAS write latency, write recovery latency, burst length, output driver impedance, and input ODT impedance of the DDR3 SDRAM.

NOTE

- The values of the CL and DDRC_TIMING1[cl] must be the same.
- The values of the CAS write latency and DDRC_TIMING1[wl]must be the same.
- DDRC_EMRS01 maps to the MRS and EMRS1 of the DDR3 SDRAM. When configuring DDRC_EMRS01, you only need to configure bits A15 to A0. The actual valid bits are A13 to A0. You do not need to configure the upper three bits A18−A16 (bank address) of the mode register. Note that the bank address for some DDRn SDRAMs corresponds to bits A17−A15.

Step 14 Set DDRC_CONFIG0 to 0x8000_0610 and set DDRC_CONFIG1 to 0x785 based on the type and storage space of the DDR3 SDRAM. This indicates that the DDRC is in 32-bit DDR3 SDRAM mode.

NOTE

The low power mode is disabled by default after power-on reset. During initialization, the functions of automatically enabling the low-power mode and disabling clocks must be disabled. In normal mode, you are advised to enable the low-power control function to reduce the power consumption.

Step 15 Set the memory space base address register DDRC_BASEADDR to 0x8000_0000.

Step 16 Configure DDRC_TIMING0–DDRC_TIMING3 based on the working frequency and the DDR components. The values of cl and wl must be consistent with the configured values of the DDRC_EMRS01 and DDRC_EMRS23 registers.

Step 17 Set DDRC_DTRCTRLto 0x0F00_0503 to enable initialization automatic training mode.

Step 18 Set DDRC_ODTCFG[wodt0] to 0x1 and DDRC_ODTCFG [rodt0] to 0x0.

Step 19 Set DDRC_PHYCFG to 0x2.

Step 20 Set DDRC_INITCTRL to 0x1 to start the initialization.

Step 21 Wait until the value of DDRC_INITCTRL becomes 0.

---End

After the preceding steps are complete, the DDR3 SDRAM works properly.

4.1.4.5 Low-Power Configuration

The DDRC supports two types of low-power modes for the DDRn SDRAM: DDRn SDRAM power-down mode and DDRn SDRAM self-refresh mode.

When DDRC_CONFIG0[pd_en] and DDRC_CONFIG0[pd_prd] are set to valid values, the DDRC automatically forces the DDRn SDRAM to enter the low-power mode if the system is idle. When DDRC_CONFIG0[pd_en] is set to 1 and the DDRC does not access the DDRn SDRAM withinDDRC_CONFIG0[pd_prd] bus clock cycles, the DDRC forces the DDRn SDRAM to enter the low-power mode.

When

DDRC_SREFCTRL[sr_seq] is set to a valid value, the DDRC forces the DDRn SDRAM to enter the self-refresh mode. When

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DDRC_SREFCTRL[sr_req] is set to 1, the DDRC forces the DDRn SDRAM to enter the self-refresh mode without responding to the bus requests after completing the current access operation.

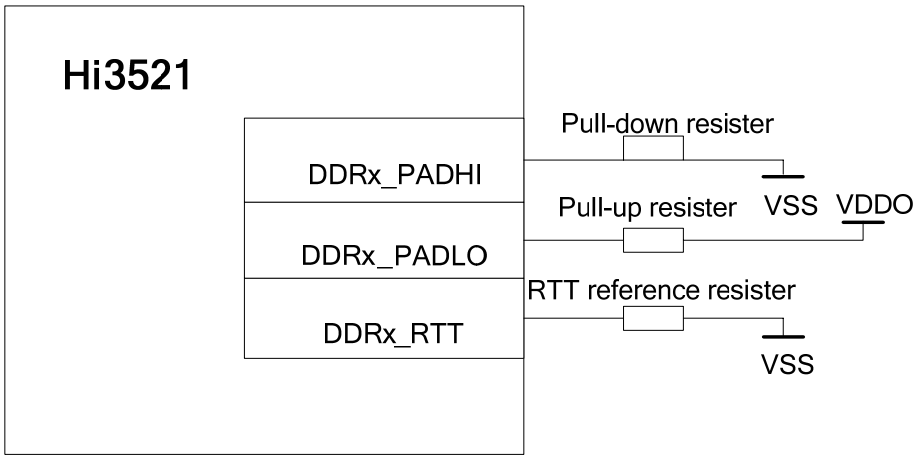
4.1.4.6 DDR IOs Impedance Configuration

When the DDRn SDRAM is used, DDRC automatically calibrates the transmit impedance and receive impedance of the DDR IOs.

You can enable the automatic calibration function by configuring DDRC_IOCMP[update_en]. By default, the automatic calibration function is enabled.

To implement the calibration function, 2% reference resistors need to be connected to chip IOs. Figure 4-3 shows how the reference resistors are connected.

Figure 4-3 Diagram of connecting the reference resistors to the DDR IOs



Description:
The letter *x* in DDRx indicates the DDR controller ID and its value is 0 or 1.

The transmit impedance and receive impedance of the DDR IOs vary according to the reference resistors connected to the DDR IOs. Table 4-6 and Table 4-7 describe the relationships between the reference resistors and the IO transmit impedance and receive impedance.

Table 4-6 Transmit impedance

DDR IO Type	Pull-Up Resistor (Ω)	Pull-Down Resistor (Ω)	Driven Impedance (Ω)
SSTL_1.8V_ClassI	68	68	34
SSTL_1.8v_CalassII	43	43	21.5
SSTL_1.5v	68	68	34

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Table 4-7 Receive impedance

DDRC_IOCFG[rtt]	Reference Resistor RTT (Ω)	Matched Impedance (Ω)
01	200	100
01	240	120
01	300	150
1x	200	50
1x	240	60
1x	300	75

NOTE

You are advised to select the 240 Ω receive resister in DDR3 mode and 300 Ω receive resister in DDR2 mode.

4.1.5 Register Summary

Table 4-8 describes the value ranges and meanings of the variables in the offset addresses of registers.

Table 4-8 Variables in the offset addresses of registers

Variable	Value Range	Description
blanes	0–3	Number of byte lanes supported by the DDRC
id0	0–15	Number of priority supported by the DDRC
ports	0–5	Number of AXI ports

Table 4-9 describes the DDRC registers.

Table 4-9 Summary of the DDRC registers (base address: 0x2011_0000)

Offset Address	Register	Description	Page
0x000	DDRC_STATUS	DDRC status register	4-18
0x004	DDRC_SREFCTRL	DDRC self-refresh control register	4-18
0x008	DDRC_INITCTRL	DDRC initialization control register	4-19
0x010	DDRC_CTRL	DDRC control register	4-19
0x014	DDRC_EMRS01	DDRC mode configuration register	4-20
0x018	DDRC_EMRS23	DDRC extended mode configuration register	4-21

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Offset Address	Register	Description	Page
0x01C	DDRC_CONFIG0	DDRC function configuration register 0	4-21
0x020	DDRC_CONFIG1	DDRC function configuration register 1	4-23
0x024	DDRC_CMDCFG	DDRC command configuration register	4-26
0x028	DDRC_CMDEXE	DDRC software configuration command start register	4-26
0x02C	DDRC_RNKCFG	DDR feature configuration register	4-27
0x040	DDRC_BASEADDR	DDR space base address configuration register	4-28
0x050	DDRC_TIMING0	DDR timing parameter register 0	4-29
0x054	DDRC_TIMING1	DDR timing parameter register 1	4-29
0x058	DDRC_TIMING2	DDR timing parameter register 2	4-30
0x05C	DDRC_TIMING3	DDR timing parameter register 3	4-32
0x060	DDRC_TIMING4	DDR timing parameter register 4	4-33
0x0A0	DDRC_DTRADDR	DDRC gating training address configuration register	4-33
0x0A4	DDRC_DTRDATA0	DDRC gating training data configuration register 0	4-34
0x0A8	DDRC_DTRDATA1	DDRC gating training data configuration register 1	4-34
0x0AC	DDRC_DTRCTRL	DDRC gating training control register	4-35
0x0B0	DDRC_DTRPRD	DDRC gating track period configuration register	4-36
0x0B4	DDRC_DTRGATE	DDRC gating phase position register	4-37
0x0C4	DDRC_DTRLAT	DDRC gating period position register	4-37
0x0D4	DDRC_DTRSTATUS	DDRC gating status register	4-38
0x0F0	DDRC_AXISTATUS	DDRC interface status register	4-39
0x0F4	DDRC_ODTCFG	DDR ODT feature configuration register	4-40
0x100	DDRC_QOSCFG0	DDRC QoS algorithm configuration register 0	4-40
0x150+0x4 x id0	DDRC_QOS	DDRC command priority configuration register	4-41
0x200+0x4 x ports	DDRC_FLUX	DDRC AXI port bandwidth traffic control configuration register	4-42

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Offset Address	Register	Description	Page
0x240	DDRC_TEST0	DDRC test status register	4-43
0x244	DDRC_TEST1	DDRC test status register	4-43
0x248	DDRC_TEST2	DDRC test status register	4-44
0x24C	DDRC_TEST3	DDRC test status register	4-44
0x250	DDRC_TEST4	DDRC test status register	4-45
0x260	DDRC_TEST7	DDRC performance measurement control register	4-45
0x264	DDRC_TEST8	DDRC write command count register	4-46
0x268	DDRC_TEST9	DDRC read command count register	4-46
0x26C	DDRC_TEST10	DDRC DMC wait command count register	4-47
0x280	DDRC_TEST12	DDRC test status register	4-47
0x400	DDRC_PHYCFG	DDRPHY configuration register	4-48
0x410	DDRC_PHYNEG	DDRPHY gating phase position register	4-49
0x420	DDRC_PHYSEL	DDRPHY gating period position register	4-49
0x430	DDRC_CDLLCFG	DDRPHY command channel DLL configuration register	4-50
0x440+0x4 x blanes	DDRC_QDLLCFG	DDRPHY data channel DLL configuration register	4-51
0x470	DDRC_LVLSKEW	DDRPHY data line phase tune control register	4-52
0x474	DDRC_LVLCTRL	DDRPHY write level control register	4-52
0x478	DDRC_LVLSTR	DDRPHY write level DQS control register	4-53
0x47C	DDRC_LVLODT	DDRPHY write level ODT control register	4-53
0x480+0x4 x blanes	DDRC_LVLCTL	DDRPHY write level configuration register 0	4-54
0x4B0+0x4 x blanes	DDRC_LVLFC	DDRPHY write level configuration register 1	4-54
0x4E0	DDRC_LVLRSP	DDRPHY write level response register	4-55
0x4E4	DDRC_LVLST	DDRPHY write level status register	4-53
0x4F0	DDRC_PHYSRST	DDRPHY soft reset control signal register	4-55
0x500	DDRC_WRDQS_SKEW	DDRPHY write DQS tune register	4-56

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Offset Address	Register	Description	Page
0x504	DDRC_RDDQS_SKEW	DDRPHY read DQS tune register	4-56
0x508	DDRC_WRDMSKEW	Write mask tune configuration register	4-57
0x510+0x4 x blanes	DDRC_WRDQSKEW	DDRPHY write data delay tune register	4-57
0x540+0x4 x blanes	DDRC_RDDQSKEW	DDRPHY read data delay tune register	4-58
0x570	DDRC_IOCFG	DDRPHY IO configuration register	4-59
0x580	DDRC_IOCMP	DDRPHY IO compensation configuration register	4-60
0x590	DDRC_CMPSTATUS0	DDRPHY IO compensation status register 0	4-61
0x598	DDRC_CMPSTATUS1	DDRPHY IO compensation status register 1	4-61

4.1.6 Register Description

DDRC_STATUS

DDRC_STATUS is a DDRC status register.

Offset Address	Register Name	Total Reset Value
0x000	DDRC_STATUS	0x0000_0005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												in_init	in_sr	reserved	busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	RO	in_init	Initialization status of a controller. 0: normal 1: initializing
[2]	RO	in_sr	Self-refresh status of a controller. 0: normal 1: self refreshing

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Offset Address	Register Name	Total Reset Value
0x000	DDRC_STATUS	0x0000_0005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												in_init	in_sr	reserved	busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[1]	RO	reserved	Reserved.
[0]	RO	busy	Busy status of a controller. 0: idle 1: A command is being processed.

DDRC_SREFCTRL

DDRC_SREFCTRL is a DDRC self-refresh control register.

Offset Address	Register Name	Total Reset Value
0x004	DDRC_SREFCTRL	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															sr_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	sr_req	SDRAM self-refresh request. 0: exit the self-refresh status 1: enter the self-refresh status

DDRC_INITCTRL

DDRC_INITCTRL is a DDRC initialization control register.

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Offset Address	Register Name	Total Reset Value
0x008	DDRC_INITCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															init_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	init_req	Initialization enable. 0: Initialization is complete or initialization is performed properly. 1: The SDRAM starts to be initialized.

DDRC_CTRL

DDRC_CTRL is a DDRC control register.

Offset Address	Register Name	Total Reset Value
0x010	DDRC_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ddr_rst_n
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	ddr_rst_n	DDR3 SDRAM reset. 0: reset 1: deassert reset **Note: This bit is valid only for the DDR3 SDRAM and is set to 1 by default.**

DDRC_EMRS01

DDRC_EMRS01 is a DDR mode configuration register.

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Offset Address	Register Name	Total Reset Value
0x014	DDRC_EMRS01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	emrs1																mrs															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	emrs1	DDRn SDRAM extended mode register 1. This field corresponds to bits 15−0 of mode register 1 (MR1) in the DDRn SDRAM user manual. Because MR1 bit[15:14] are not used for most DDRs. DDRC_EMRS01 bit[31:30] are set to 0b00. For details about MR1, see the DDRn SDRAM user manual.
[15:0]	RW	mrs	DDRn SDRAM mode register. This field corresponds to bits 15−0 of mode register 0 (MR0) in the DDRn SDRAM user manual. Because MR0 bit[15:14] are not used for most DDRs. DDRC_EMRS01 bit[15:14] are set to 0b00. For details about MR0, see the DDRn SDRAM user manual.

DDRC_EMRS23

DDRC_EMRS23 is a DDR extended mode configuration register.

Offset Address	Register Name	Total Reset Value
0x018	DDRC_EMRS23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	emrs3																emrs2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	emrs3	DDRn SDRAM extended mode register 3. This field corresponds to bits 15−0 of mode register 3 (MR3) in the DDRn SDRAM user manual. Because MR3 bit[15:14] are not used for most DDRs. DDRC_EMRS23 bit[31:30] are set to 0b00. For details about MR3, see the DDRn SDRAM user manual.
[15:0]	RW	emrs2	DDRn SDRAM extended mode register 2. This field corresponds to bits 15−0 of mode register 2 (MR2) in the DDRn SDRAM user manual. Because MR2 bit[15:14] are not used for most DDRs. DDRC_EMRS23 bit[15:14] are set to 0b00. For details about MR2, see the DDRn SDRAM user manual.

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DDRC_CONFIG0

DDRC_CONFIG0 is DDRC function configuration register 0.

Offset Address	Register Name	Total Reset Value
0x01C	DDRC_CONFIG0	0x2000_0510

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	init_arefnum				pd_prd								rcv_pdr	sr_cc	pd_cc	pd_en	reserved			rank	reserved		dram_type		reserved		mem_width		reserved		brst_a12	brstlen
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	init_arefnum	Number of auto-refresh operations when the DDRn SDRAM is being initialized. 0x0–0x2: two 0x3–0xF: n.
[27:20]	RW	pd_prd	Power down cycle of the SDRAM. When the DDRC does not receive any command in pd_prd consecutive cycles, it forces the DDRn SDRAM to enter the low-power mode; when a command is received, the DDRC forces the DDRn SDRAM to exit the low-power mode. 0x00: 1 clock cycle 0x01–0xFF: n clock cycles Note: This parameter is valid only when pd_en is 1.
[19]	RW	rcv_pdr	DDR receive I/O dynamic power-down control enable. The DDRC disables the receive buffer of the DDR data I/O in the non-read status when it is enabled. 0: disabled 1: enabled
[18]	RW	sr_cc	DDRn SDRAM clock control in self-refresh mode. 0: The DDRn SDRAM clock is enabled. 1: The DDRn SDRAM clock is disabled.
[17]	RW	pd_cc	DDRn SDRAM clock control in power-down mode. 0: The DDRn SDRAM clock is enabled. 1: The DDRn SDRAM clock is disabled. Note: This parameter is valid only when the LPDDR SDRAM or LPDDR2 SDRAM is connected.
[16]	RW	pd_en	Automatic low-power enable of the DDRn SDRAM. 0: disabled 1: enabled
[15:14]	RW	reserved	Reserved.

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[13:12]	RW	rank	Rank configuration of the DDRC. 00: 1 rank Other values: reserved
[11]	RW	reserved	Reserved.
[10:8]	RW	dram_type	External memory type. 101: DDR2 110: DDR3 Other values: reserved
[7:6]	RW	reserved	Reserved.
[5:4]	RW	mem_width	Bit width of the storage data bus. 00: 16 bits 01: 32 bits Other values: reserved
[3:2]	RO	reserved	Reserved.
[1]	RO	brst_a12	DDR3 SDRAM A12 command enable. 0: disabled 1: enabled Note: The recommended value is 0.
[0]	RW	brstlen	Burst length of the DDRC. 0: burst4 1: burst8 When the ratio of the frequency of the DDRC to the frequency of the PHY is 1:1, the burst length of the DDR2 SDRAM can be set to burst 4 or burst 8.The burst length of the DDR3 SDRAM can only be set to burst 8. When the ratio of the frequency of the DDRC to the frequency of the PHY is 1:2, the burst length of the DDR2 SDRAM and the DDR3 SDRAM can only be set to burst 4

DDRC_CONFIG1

DDRC_CONFIG1 is DDRC function configuration register 1.

Offset Address	Register Name	Total Reset Value
0x020	DDRC_CONFIG1	0x0000_A380

Bit	31 30 29 28	27 26 25 24	23 22 21	20	19 18	17	16	15 14 13 12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sref_arefnum	reserved		clk_switch	reserved	odis_ddrio	pd_ac	pd_pst_opn	pd_pre_cls	reorder_en	auto_pre_en	wr_rcv_mode	exclu_en	lock_en	aref_mode	wrlvl_en	reserved	read_mode	clkratio	ecc_en	zqc_en

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	sref_arefnum	Number of times of auto refresh operations after DDRn SDRAM exits auto refresh in DFS process. 0x0–0x1: once 0x2–0xF: n times Note: This field is valid only when train_en is 1. When train_en is 0, DDRn SDRAM exits self refresh and DDRC does not perform auto refresh operation.
[27:21]	RW	reserved	Reserved.
[20]	RW	clk_switch	DDRC low-power clock switch control. This field determines whether to perform back pressure on AXI port command when DDRC enters the low-power status (DDR self refresh). 0: not perform back pressure on the command and return the error response. 1: perform back pressure on the command and run the original command when the clock is switched.
[19:18]	RW	reserved	Reserved.
[17]	RW	odis_ddrio	Output disable configuration of the DDR command and data I/O. 0: enable the pin output 1: disable the pin output Note: This is a static configuration. When DDR enters the self–refresh mode, set DDR to 1 to disable the DDR command and data I/O output. Before DDR exits the self–refresh mode, set DDR to 0 to enable the DDR command and data I/O output.
[16]	RW	pd_ac	SDRAM address command status enable control in power-down mode. 0: enable the pin output 1: disable the pin output Note: When pd_en is enabled, pd_ac is valid. The control pins exclude CKE, ODT, CSN, and RESET_N.
[15:14]	RW	pd_pst_opn	SDRAM address/command pin delay before the power-down mode is exited. 00: 0 cycles 01: 1 cycle 10: 2 cycles 11: 3cycles Note: When pd_en is enabled, pd_pst_opn is valid. The control pins exclude CKE and RESET_N.

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[13:12]	RW	pd_pre_cls	SDRAM address/command disable delay after the power-down mode is entered. 00: 0 cycles 01: 1 cycle 10: 2 cycles 11: 3 cycles Note: When pd_en is enabled, pd_pre_cls is valid. The control pins exclude CKE and RESET_N.
[11]	RW	reserved	Reserved.
[10]	RW	auto_pre_en	Auto precharge enable. 0: disabled 1: enabled
[9]	RW	wr_rcv_mode	Mode of receiving the write command over the DDRC AXI port. 0: The write command is received directly. 1: The write command is received only after the expected data to be written arrives.
[8]	RW	exclu_en	Exclusive command enable. 0: disabled 1: enabled
[7]	RW	lock_en	WRAP command lock enable. 0: disabled 1: enabled
[6]	RW	aref_mode	Auto-refresh mode select. 0: An auto-refresh operation is performed every one tREFI period. 1: Eight auto-refresh operations are performed every nine tREFI periods.
[5]	RW	wrlvl_en	Auto-control enable of the DDR3 write level hardware. 0: disabled 1: enabled
[4]	RW	reserved	Reserved. This field is set to 0.
[3]	RW	read_mode	Read mode select of the DDRC. 0: associated read mode 1: delay read mode The associated read mode is a mode in which the DDRC samples data based on the data valid signal from the PHY. The delay read mode is a mode in which the DDRC samples the data from the PHY after the internal delay of the DDRC. Note: This bit must be set to 0 when DDRC_DTRCTRL[train_mode] is set to 0.

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[2]	RW	clkratio	Operating mode of the DDRC. When the frequency ratio of DDRC to PHY is 1:1, this bit is set to 0. When the frequency ratio of DDRC to PHY is 1:2, this bit is set to 1.
[1]	RW	ecc_en	ECC enable of the DDRC 0: disabled 1: enabled
[0]	RW	zqc_en	DDR3 SDRAM ZQ enable. 0: disabled 1: enabled Note: This bit is valid for the DDR3 SDRAM only and is set to 1 by default.

DDRC_CMDCFG

DDRC_CMDCFG is a DDRC command configuration register.

Offset Address	Register Name	Total Reset Value
0x024	DDRC_CMDCFG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1 0
Name	cmd_mrs				cmd_ba		cmd_rank	reserved	cmd_type
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0

Bits	Access	Name	Description
[31:16]	RW	cmd_mrs	Value of the DDR mode register when the load mode register (LMR) command is configured.
[15:8]	RW	cmd_ba	Value of the DDR BA when the LMR command is configured.
[7:4]	RW	cmd_rank	Rank for running commands. 0: The configuration command is executed. 1: The configuration command is not executed. Each bit controls a rank. Note: As the Hi3521 only has rank0, cmd_rank must be set to 0x0 or 0x1.
[3:2]	RW	reserved	Reserved.

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[1:0]	RW	cmd_type	DDR command configuration. 00: enter the deep power-down mode 01: exit the deep power-down mode 10: LMR command 11: ZQCL

DDRC_CMDEXE

DDRC_CMDEXE is a DDRC software configuration command start register.

Offset Address	Register Name	Total Reset Value
0x028	DDRC_CMDEXE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															cmd_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	cmd_req	Request of executing the configuration command of the DDRC. 0: The command is not executed or the parameter is cleared automatically after the command is executed. 1: The command is requested to be executed.

DDRC_RNKCFG

DDRC_RNKCFG is a DDR feature configuration register.

Offset Address	Register Name	Total Reset Value
0x02C	DDRC_RNKCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		mem_map		reserved				mem_bank	reserved			mem_row			reserved		mem_col			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.

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Offset Address	Register Name	Total Reset Value
0x02C	DDRC_RNKCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		mem_map		reserved			mem_bank	reserved		mem_row			reserved		mem_col	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[13:12]	RW	mem_map	Address translation mode of the SDRAM. 00: {Rank, Row, Ba, Col, DW} = AXI_Address 01: {Rank, Ba, Row, Col, DW} = AXI_Address Other values: reserved
[11:9]	RW	reserved	Reserved.
[8]	RW	mem_bank	Number of banks of a single SDRAM. 0: 4 banks 1: 8 banks
[7]	RW	reserved	Reserved.
[6:4]	RW	mem_row	Bit width of the row address of a single SDRAM. 000: 11 bits 001: 12 bits 010: 13 bits 011: 14 bits 100: 15 bits. 101: 16 bits. Other values: reserved
[3]	RW	reserved	Reserved.
[2:0]	RW	mem_col	Bit width of the column address of a single SDRAM. 000: 8 bits 001: 9 bits 010: 10 bits 011: 11 bits 100: 12 bits. Other values: reserved

DDRC_BASEADDR

DDRC_BASEADDR is a DDR space base address configuration register.

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Offset Address	Register Name	Total Reset Value
0x040	DDRC_BASEADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mem_base_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mem_base_addr	Configuration of the start base address of the DDR in the system.

DDRC_TIMING0

DDRC_TIMING0 is DDR timing parameter register 0.

Offset Address	Register Name	Total Reset Value
0x050	DDRC_TIMING0	0xFFFF_3F1F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tmrd				trrd				trp				trcd				reserved				trc				reserved				tras			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:28]	RW	tmrd	Count of wait cycles of LMR command. 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles
[27:24]	RW	trrd	Number of wait cycles of the ACT bank A to ACT bank B command. 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles
[23:20]	RW	trp	Count of wait cycles for disabling commands (PRE period). 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles
[19:16]	RW	trcd	Number of wait cycles from the ACT bank command to the read or write bank command. 0x0–0x3: 3 clock cycles 0x4–0xF: n clock cycles
[15:14]	RW	reserved	Reserved.

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Offset Address	Register Name	Total Reset Value
0x050	DDRC_TIMING0	0xFFFF_3F1F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tmrd				trrd				trp				trcd				reserved				trc				reserved				tras			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[13:8]	RW	trc	Number of wait cycles from an ACT bank command to the next ACT bank command. 0x00–0x01: 1 clock cycle 0x02-0x3F: n clock cycles
[7:5]	RW	reserved	Reserved.
[4:0]	RW	tras	Number of wait cycles from ACT to PRE. 0x00–0x01: 1 clock cycle 0x02-0x0F: n clock cycles

DDRC_TIMING1

DDRC_TIMING1 is DDR timing parameter register 1.

Offset Address	Register Name	Total Reset Value
0x054	DDRC_TIMING1	0xFF01_45FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tsre								trdlat				trtw				twl				tcl				trfc							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RW	tsre	Number of wait cycles from the self-refresh exit command to the read command. 0x0: 1 clock cycle 0x01–0xFF: n x 2 clock cycles. When the DDR3 SDRAM is used, the value is set to tXSDLL.
[23:20]	RW	trdlat	Inherent delay of the DDRPHY. 0x0–0xF: n + 1 clock cycles When the Dophin PHY is used, the value is set to 0x5. This field is valid when read_mode is 1 (delay read mode).

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Offset Address	Register Name	Total Reset Value
0x054	DDRC_TIMING1	0xFF01_45FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tsre								trdlat				trtw				twl				tcl				trfc							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[19:16]	RW	trtw	Delay from the last read data segment to the first written data segment. 0x0–0x1: 1 clock cycle 0x2-0xF: n + 1 clock cycles
[15:12]	RW	twl	Number of wait cycles from the write command to the write data. 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles For example, 0x3 indicates 3 clock cycles. Note: In DDR2 mode, tw1 is set to (tcl – 1) and the equation of twl – taond ≥ 1 must be true.
[11:8]	RW	tcl	DDR CL from the read command to the read data. 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles
[7:0]	RW	trfc	Number of wait cycles of the AREF period or AREF to the ACT command. The register can be set to the maximum value max{trfc, tzqcs}. 0x00–0x01: 1 clock cycle 0x02–0xFF: n clock cycles

DDRC_TIMING2

DDRC_TIMING2 is DDR timing parameter register 2.

Offset Address	Register Name	Total Reset Value
0x058	DDRC_TIMING2	0xF3F3_F000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tcke				twtr				twr				reserved				tfaw				reserved				taref							

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Reset	1	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	tcke	Minimum cycle of maintaining the low-power mode. 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles The value needs to be set to the maximum value among tCKESR, tCKSRE, tCKSRX, and tCKE. When the Dophin DDRPHY is used, the value of this register needs to be set to max{tCKSRx, tCKE} + 3.
[27:24]	RW	twtr	Number of wait cycles of the last write-to-read command. 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles For example, 0x3 indicates 3 clock cycles.
[23:20]	RW	twr	Number of wait cycles of write recovery. 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles Note: When DFS is required, tWR must be set to the maximum frequency in the DFS and cannot be changed with the frequency of the DDR.
[19:18]	RW	reserved	Reserved.
[17:12]	RW	tfaw	4-bank activate period. 0x00-0x3F: n clock cycles For example, 0x14 indicates 20 clock cycles.
[11]	RW	reserved	Reserved.
[10:0]	RW	taref	Number of auto-refresh cycles. 0x000: forbidden 0x001–0x7FF: The auto-refresh cycle of the SDRAM is 16 x n clock cycles. For example, 0x008 indicates 128 clock cycles. The configuration interval is tREFI = 7800/16/tclk. Tclk is the running cycle when the SDRAM is used. When DDRC_CONFIG1[aref_mode] is 1, the interval of DDRC_TIMING2 must be set to 8 x tREFI.

DDRC_TIMING3

DDRC_TIMING3 is DDR timing parameter register 3.

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Offset Address	Register Name	Total Reset Value
0x05C	DDRC_TIMING3	0xFFDF_F0F2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tzq_prd												tzqinit								taond				txard				trtp			
Reset	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	0

Bits	Access	Name	Description
[31:22]	RW	tzq_prd	Number of ZQCS command cycles. 0x000: The ZQCS command is forbidden. 0x001–0x3FF: n x 128 AREF cycles. The number of ZQCS command cycles is n x 128 taref clock cycles.
[21:12]	RW	tzqinit	Number of delay cycles during ZQ initialization. 0x0–0x1FF: n + 1 clock cycles The value needs to be set to the maximum value between tZQINIT and tDLLK.
[11:8]	RW	taond	Count of ODT enable/disable cycles. In DDR2 mode (taond/taofd): 0x0: 2/2.5 0x1: 3/3.5 0x2: 4/4.5 0x3: 5/5.5 Other values: reserved In DDR3 mode, the value is set to (tWL – 1).
[7:4]	RW	txard	Numberof wait cycles of exiting the DDR low-power mode. 0x0–0xF: n clock cycles. The letter *n* indicates the corresponding decimal value. For example, 0x7 indicates 7 clock cycles. The value is set to the maximum value among tXP, tXARD, tXARDS, and tXS. In DDR3 mode, when the register is set to tXS, txard only needs to be set to an equivalent clock cycle of 10 ns.
[3:0]	RW	trtp	Wait delay from the read command to the disable command. 000–010: 2 clock cycles 011–111: n clock cycles Trtp is calculated as follows: AL + BL/2 + Max (trtp,2) – 2

DDRC_TIMING4

DDRC_TIMING4 is DDR timing parameter register 4.

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Offset Address	Register Name	Total Reset Value
0x060	DDRC_TIMING4	0x000F_2028

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												twlo				reserved				twldqsen				reserved				twlmrd			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	0

Bits	Access	Name	Description
[31:20]	RW	reserved	Reserved.
[19:16]	RW	twlo	DDR3 write level status delay. 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles The parameter is equal to twlo+twloe defined in the DDR3 protocol.
[15:14]	RW	reserved	Reserved.
[13:8]	RW	twldqsen	DDR3 write level start delay. 0x0–0x1: 1 clock cycle 0x02-0x3F: n clock cycles
[7:6]	RW	reserved	Reserved.
[5:0]	RW	twlmrd	Valid delay of the initial DQS of DDR3 write level. 0x0–0x1: 1 clock cycle 0x02-0x3F: n clock cycles

DDRC_DTRADDR

DDRC_DTRADDR is a DDRC gating training address configuration register.

Offset Address	Register Name	Total Reset Value
0x0A0	DDRC_DTRADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	train_row																train_bank				train_col											

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	train_row	Row address of the DDRn SDRAM used in the gating position training. When the row address is less than 16 bits, the upper bits are stuffed with 0s.
[15:13]	RW	train_bank	Bank address of the DDRn SDRAM used in the gating position training. When the bank address is less than three bits, the upper bits are stuffed with 0s.
[12:0]	RW	train_col	Column address of the DDRn SDRAM used in the gating position training. When the column address is less than 13 bits, the upper bits are stuffed with 0s.

DDRC_DTRDATA0

DDRC_DTRDATA0 is DDRC gating training data configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0A4	DDRC_DTRDATA0	0xE11E_D22D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dtr_byte3								dtr_byte2								dtr_byte1								dtr_byte0							
Reset	1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	0	1	1	0	1	0	0	1	0	0	0	1	0	1	1	0	1

Bits	Access	Name	Description
[31:24]	RW	dtr_byte3	Gating training data configuration 0 of the DDRC. When the DDRC performs training, data must be transferred in DDR BL8 mode in each read or write operation. Note: The data configured for each byte (data for the upper four bits and lower four bits) must be different.
[23:16]	RW	dtr_byte2	Gating training data configuration of the DDRC.
[15:8]	RW	dtr_byte1	Gating training data configuration of the DDRC.
[7:0]	RW	dtr_byte0	Gating training data configuration of the DDRC.

DDRC_DTRDATA1

DDRC_DTRDATA1 is DDRC gating training data configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0A8	DDRC_DTRDATA1	0xC33C_B44B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dtr_byte7								dtr_byte6								dtr_byte5								dtr_byte4							

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Reset	1	1	0	0	0	0	1	1	0	0	1	1	1	1	0	0	1	0	1	1	0	1	0	0	0	1	0	0	1	0	1	1

Bits	Access	Name	Description
[31:24]	RW	dtr_byte7	Gating training data configuration 1 of the DDRC. When the DDRC performs training, data must be transferred in DDR BL8 mode in each read or write operation. Note: The data configured for each byte (data for the upper four bits and lower four bits) must be different.
[23:16]	RW	dtr_byte6	Gating training data configuration of the DDRC.
[15:8]	RW	dtr_byte5	Gating training data configuration of the DDRC.
[7:0]	RW	dtr_byte4	Gating training data configuration of the DDRC.

DDRC_DTRCTRL

DDRC_DTRCTRL is a DDRC gating training control register.

Offset Address	Register Name	Total Reset Value
0x0AC	DDRC_DTRCTRL	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dt_byte								reserved				train_start_pos				reserved		train_rank		rensel			train_mode	reserved				dt_limit				reserved	track_en	train_en	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dt_byte	Byte training enable. 0: forbidden 1: enable. [24]: DDRC byte0 training enable … [31]: DDRC byte7 training enable
[23:20]	RW	reserved	Reserved.
[19:16]	RW	train_start_pos	Start position of the gating training. 0x0-0x5: n clock cycles Other values: reserved
[15:14]	RW	reserved	Reserved.
[13:12]	RW	train_rank	Number of ranks in the gating training. 0x0–0x3: n + 1 ranks Note: As the Hi3521 has only one rank, train_rank can be set only to 0.

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[11:9]	RW	rensel	Read enable delay cycle. 000–011: n + 1 clock cycles Other values: reserved
[8]	RW	train_mode	Gating training mode. 0: Dophin training mode 1: common training mode
[7:6]	RW	reserved	Reserved.
[5:4]	RW	dt_limit	DQS gating shift control. 00: shift 0° 01: shift 90° 10: shift 180° 11: shift 270°
[3]	RW	reserved	Reserved.
[2]	RW	track_en	Auto-refresh enable for the gating position. 0: disabled 1: enabled Note: A read operation is required between two training operations and the continuous length of the accessed data must be greater than DDR burst 8.
[1]	RW	train_en	Gating position training enable. 0: disabled 1: enabled
[0]	RW	reserved	Reserved.

DDRC_DTRPRD

DDRC_DTRPRD is a DDRC gating track period configuration register.

Offset Address	Register Name	Total Reset Value
0x0B0	DDRC_DTRPRD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												track_prd																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.

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[19:0]	RW	track_prd	Auto-update period configuration of the DQS gating. The DDRC tracks the gating position in the configured period. 0x0: one AREF period 0x1–0x7FF: n + 1 AREF periods

DDRC_DTRGATE

DDRC_DTRGATE is a DDRC gating phase position register.

Offset Address	Register Name	Total Reset Value
0x0B4	DDRC_DTRGATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																gate_sel															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved. Note: This register cannot be read continuously.
[15:0]	RW	gate_sel	Gating phase position of the DDRC. 00: 0° 01: 90° 10: 180° 11: 270° [2 x (N + 1) – 1:2 x N]: gating phase of DDRC byteN N = 0–7

DDRC_DTRLAT

DDRC_DTRLAT is a DDRC gating period position register.

Offset Address	Register Name	Total Reset Value
0x0C4+0x4*rnks rnks (0–0)	DDRC_DTRLAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sys_lat																															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sys_lat	Number of gating delay cycles of the DDRC. 0x0–0x5: n clock cycles Other values: reserved [4 x (N + 1)-1:4 x N]: gating phase of DDRC ByteN. N = 0–7 Note: This register cannot be read or written continuously.

DDRC_DTRSTATUS

DDRC_DTRSTATUS is a DDRC gating status register.

Offset Address	Register Name	Total Reset Value
0x0D4+0x4 x rnks rnks(0–0)	DDRC_DTRSTATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								dtr_st								reserved				dtr_ok				reserved				dtr_err			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	dtr_st	Phase shift status of the byte gating position. 00: shift 0° 01: shift 90° 10: shift 180° 11: shift 270° bit[31:30] to bit[17:16]: Each two bits correspond to DDRC byte7 to DDRC byte0 respectively.
[15:8]	RO	dtr_ok	Gating training status. 0: training error 1: no training error bit[15] to bit[8]: Each bit corresponds to DDRC byte7 to DDRC byte0 respectively.
[7:0]	RO	dtr_err	Auto tracking error status of the gating position. 0: no tracking error 1: tracking error bit[7] to bit[0]: Each bit corresponds to DDRC byte7 to DDRC byte0 respectively.

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DDRC_AXISTATUS

DDRC_AXISTATUS is a DDRC interface status register.

Offset Address	Register Name	Total Reset Value
0x0F0	DDRC_AXISTATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								axi_st7	axi_st6	axi_st5	axi_st4	axi_st3	axi_st2	axi_st1	axi_st0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	RO	axi_st7	Status of DDRC bus interface 7. 0: idle 1: A command is being executed.
[6]	RO	axi_st6	Status of DDRC bus interface 6. 0: idle 1: A command is being executed.
[5]	RO	axi_st5	Status of DDRC bus interface 5. 0: idle 1: A command is being executed.
[4]	RO	axi_st4	Status of DDRC bus interface 4. 0: idle 1: A command is being executed.
[3]	RO	axi_st3	Status of DDRC bus interface 3. 0: idle 1: A command is being executed.
[2]	RO	axi_st2	Status of DDRC bus interface 2. 0: idle 1: A command is being executed.
[1]	RO	axi_st1	Status of DDRC bus interface 1. 0: idle 1: A command is being executed.
[0]	RO	axi_st0	Status of DDRC bus interface 0. 0: idle 1: A command is being executed.

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DDRC_ODTCFG

DDRC_ODTCFG is a DDR ODT feature configuration register.

Offset Address	Register Name	Total Reset Value
0x0F4	DDRC_ODTCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															rodt0	reserved															wodt0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	reserved	Reserved. This field must be fixed at 0.
[16]	RW	rodt0	Read ODT configuration of rank0. 0: disabled 1: enabled
[15:1]	RW	reserved	Reserved. This field must be fixed at 0.
[0]	RW	wodt0	Write ODT configuration of rank1. 0: disabled 1: enabled

DDRC_QOSCFG0

DDRC_QOSCFG0 is DDRC QoS algorithm configuration register 0.

Offset Address	Register Name	Total Reset Value
0x100	DDRC_QOSCFG0	0x0000_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									idmap_mode	id_order_ctl	order_en	dmc_fifo_lvl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:7]	RW	reserved	Reserved.

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[6]	RW	idmap_mode	ID mapping mode. 0: The id_map mapping mode configured by the register is used by default. 1: The QoS mapping mode is used. The AXI port configures this mode in associated mode by running read/write commands. This mapping mode is valid only when its macro definition is enabled in the RTL code. **This field must be 1.**
[5]	RW	id_order_ctl	Out-of –order execution enable of the specified ID. 0: disabled 1: enabled The DDRC does not ensure the order when conflict occurs between the DDR row addresses of the read/write commands with the specified ID and other IDs. Master ensures the consistency of the data.
[4]	RW	order_en	Execution order enable for the commands with the same priority. 0: disabled 1: enabled
[3:0]	RW	dmc_fifo_lvl	Depth of the command register FIFO in the DMC. 0x0–0xF: n + 1 command depths Note: The maximum depth of the command register FIFO in the Hi3521 is 0xB, but it is recommended to set the depth to 0xB.

DDRC_QOS

DDRC_QOS is a DDRC command priority configuration register.

Offset Address	Register Name	Total Reset Value
0x150+0x4 x id0 id0(0–15)	DDRC_QOS	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				rd_pri_apt				rd_age_prd				reserved			rd_qos_en	reserved				rd_qos								reserved			rd_pri	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:28]	RW	reserved	Reserved.
[27:24]	RW	pri_apt	Command priority adaptation configuration. 0x0: disabled 0x1-0xF: n x 16 clock cycles

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[23:20]	RW	age_prd	Command aging cycle configuration. 0x0: disabled 0x1-0xF: n x 16 clock cycles
[19:17]	RW	reserved	Reserved.
[16]	RW	qos_en	Command QoS enable (timeout). 0: disabled 1: enabled
[15:14]	RW	reserved	Reserved.
[13:4]	RW	qos	Command QoS configuration (timeout). 0x1-0x3FF: n clock cycles Other values: reserved Note: The used timeout is an integral multiple of 16. The lower four bits of rd_qos is ignored.
[3]	RW	reserved	Reserved.
[2:0]	RW	pri	Command priority configuration. 000: highest priority 001: higher priority … 111: lowest priority

DDRC_FLUX

DDRC_FLUX is a DDRC AXI port bandwidth traffic control configuration register.

Offset Address	Register Name	Total Reset Value
0x200+0x4 x ports ports(0–5)	DDRC_FLUX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										flux_port_en	flux_ovfl	reserved				flux_lvl				reserved				flux							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RW	reserved	Reserved.
[21]	RW	flux_port_en	AXI port DDRC traffic count enable. 0: disabled 1: enabled

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[20]	RW	flux_ovfl	AXI port traffic overflow allow enable. 0: disabled 1: enabled When this bit is set to 1, the traffic of the AXI port exceeds the bandwidth limit, and no request is raised over the AXI ports without overflow, the bandwidth of the AXI port can exceed the configured value.
[19:17]	RW	reserved	Reserved.
[16:12]	RW	flux_lvl	AXI port traffic overflow allow threshold. 0x0–0xC: DMC threshold for allowing traffic overflow Other values: reserved When flux_ovfl is set to 1, this traffic overflow over the AXI port is allowed if the traffic of the AXI port is greater than the configured bandwidth of flux and the number of the commands to be processed in DMC is less than the configured threshold.
[11:10]	RW	reserved	Reserved.
[9:0]	RW	flux	Bandwidth configuration of the AXI port. 0x0–0x3FF: ratio of the maximum DDR bandwidth to the total bandwidth accessed by the AXI port The total bandwidth is 1024. The configured value is calculated as follows: ratio of the required bandwidth to the total bandwidth x1024. For example, if 20% of bandwidth is required for this AXI port, configure flux to 0xCD.

DDRC_TEST0

DDRC_TEST0 is a DDRC test status register.

Offset Address	Register Name	Total Reset Value
0x240	DDRC_TEST0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmc_ct																dmc_cv															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	dmc_ct	DDRC command type.
[15:0]	RO	dmc_cv	Commands that are being processed by the DDRC.

DDRC_TEST1

DDRC_TEST1 is a DDRC test status register.

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Offset Address	Register Name	Total Reset Value
0x244	DDRC_TEST1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								dt_num				reserved	byte_sel		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved.
[8:4]	RW	dt_num	Cycle n select, data read from the training module (n = 0–23).
[3]	RW	reserved	Reserved.
[2:0]	RW	byte_sel	Channel select of the returned data. 0x0–0x7: channel n select

DDRC_TEST2

DDRC_TEST2 is a DDRC test status register.

Offset Address	Register Name	Total Reset Value
0x248	DDRC_TEST2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data_h																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	data_h	Upper 32 bits of the training data.

DDRC_TEST3

DDRC_TEST3 is a DDRC test status register.

Offset Address	Register Name	Total Reset Value
0x24C	DDRC_TEST3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data_l																															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	data_l	Lower 32 bits of the training data.

DDRC_TEST4

DDRC_TEST4 is a DDRC test status register.

Offset Address	Register Name	Total Reset Value
0x250	DDRC_TEST4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dt_ok_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dt_ok_cnt	Number of times of correct training data. 0x0–0xF: n + 1 [3 x (N + 1) – 1:3 x N]: number of times of correct byteN

DDRC_TEST7

DDRC_TEST7 is a DDRC performance measurement control register.

Offset Address	Register Name	Total Reset Value
0x260	DDRC_TEST7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	perf_mode	perf_en	perf_ch		perf_prd																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	perf_mode	Performance measurement mode. 0: continuous trigger mode. The performance counter counts continuously. No data overflow occurs within 1s = (533 MHz). 1: single trigger mode. When the performance counter reaches the maximum value, the count value is retained but counting is stopped. Note: When an overflow occurs, the count values wrap.

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[30]	RW	perf_en	Performance measurement enable. 0: disabled 1: enabled Note: When perf_mode is 0 and this bit is enabled, performance measurement register starts cyclic counting. When perf_mode is 1, this bit is cleared after counting is complete once.
[29:28]	RW	perf_ch	Read and write count channel. 00: disabled 01: channel 0 10: channel 1 11: channel 0 and channel 1 Note: This register limits the number of read/write command count channels of DDRC_TEST8 and DDRC_TEST9.
[27:0]	RW	perf_prd	Performance measurement cycle. 0x0–0xFFFFFFF: count cycles The actual count cycle is calculated as follows: perf_prd x 4 xtclk. Where, tclk is the bus clock cycle of the DDRC. Note: This configuration is valid only when perf_mode is 1. When perf_mode is set to 0 to select the continuous count mode, the performance counters keep on counting.

DDRC_TEST8

DDRC_TEST8 is a DDRC write command count register.

Offset Address	Register Name	Total Reset Value
0x264	DDRC_TEST8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wr_num																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RWC	wr_num	Count of write commands in the count period. This register is written to clear. Wrap cycle counting is supported.

DDRC_TEST9

DDRC_TEST9 is a DDRC read command count register.

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Offset Address	Register Name	Total Reset Value
0x268	DDRC_TEST9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_num																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RWC	rd_num	Count of read commands in the count period. This register is written to clear. Wrap cycle counting is supported.

DDRC_TEST10

DDRC_TEST10 is a DDRC DMC wait command count register.

Offset Address	Register Name	Total Reset Value
0x26C	DDRC_TEST10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmc_cmd_num																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RWC	dmc_cmd_num	Count of DMC wait commands of the DDRC in the count period. This register is written to clear. Wrap cycle counting is supported. Note: As the register width is limited and data overflow needs to be avoided within 1s under the 533 MHz clock, the displayed count value of this register is the actual count value divided by 2.

DDRC_TEST12

DDRC_TEST12 is a DDRC test status register.

Offset Address	Register Name	Total Reset Value
0x280	DDRC_TEST12	0x0000_0FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wfifo_f																wfifo_e															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	wfifo_f	Write FIFO full status.
[15:0]	RO	wfifo_e	Write FIFO empty status. Note: Only the 12-bit reset value is 0xFFF in Hi3521.

DDRC_PHYCFG

DDRC_PHYCFG is a DDRCPHY configuration register.

Offset Address	Register Name	Total Reset Value
0x400	DDRC_PHYCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ref_e	reserved			comp	comp_en	bl	bl_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	RW	ref_e	DDRCPHY I/O configuration enable. 0: controlled by external inputs 1: controlled by internal resistors
[6:4]	R0	reserved	Reserved.
[3]	RW	comp	DDRPHY gating select. 0: The DDRC outputs the gating value. 1: The gating value of the DDRPHY is used.
[2]	RW	comp_en	DDRPHY gating training enable. 0: disabled 1: enabled
[1]	RW	bl	DDRPHY burst configuration. 0: burst4 1: burst8
[0]	RW	bl_en	DDRPHY burst configuration enable. 0: disabled. Variable burst length is used. 1: enabled

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DDRC_PHYNEG

DDRC_PHYNEG is a DDRPHY gating phase position register.

Offset Address	Register Name	Total Reset Value
0x410	DDRC_PHYNEG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								neg_mod							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved. Note: This register cannot be read continuously.
[7:0]	RW	neg_mod	DDRPHY gating phase select (Dophin mode). 00: 0° phase shift 01: 90° phase shift 10: 180° phase shift 11: 270° phase shift [2 x (N + 1) – 1: 2 x N]: phase position of data channel N. N = 0, 1, 2, or 3

DDRC_PHYSEL

DDRC_PHYSEL is a DDRPHY gating period position register.

Offset Address	Register Name	Total Reset Value
0x420+0x4*rnks rnks (0–0)	DDRC_PHYSEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sel_mod							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved. Note: This register cannot be read continuously.
[7:0]	RW	sel_mod	DDRPHY gating delay select (Dophin mode). 00–11: n clock cycles [2 x (N + 1) – 1: 2 x N]: phase position of data channel N. N = 0, 1, 2, or 3

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DDRC_CDLLCFG

DDRC_CDLLCFG is a DDRPHY command channel DLL configuration register.

Offset Address	Register Name	Total Reset Value
0x430	DDRC_CDLLCFG	0x0000_0053

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		unfl	ovfl	reserved				bypctl				reserved				bypfc				reserved				limit				byp	dll_updt_en	dll_en	dll_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29]	RO	unfl	DLL underflow status. 0: No underflow occurs. 1: An underflow occurs.
[28]	RO	ovfl	DLL overflow status. 0: No overflow occurs. 1: An overflow occurs.
[27:25]	RW	reserved	Reserved.
[24:20]	RW	bypctl	ctlout value of the DLL when it is bypassed.
[19]	RW	reserved	Reserved.
[18:16]	RW	bypfc	fcout value of the DLL when it is bypassed.
[15:11]	RW	reserved	Reserved.
[10:4]	RW	limit	Locked bandwidth of the DLL.
[3]	RW	byp	DLL bypass enable. 0: disabled 1: enabled
[2]	RW	dll_updt_en	DLL update enable. 0: disabled 1: enabled
[1]	RW	dll_en	DLL enable. 0: disabled 1: enabled
[0]	RW	dll_reset	DLL reset. 0: reset 1: deassert reset

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DDRC_QDLLCFG

DDRC_QDLLCFG is a DDRPHY data channel DLL configuration register.

Offset Address	Register Name	Total Reset Value
0x440+0x4 x blanes blanes (0–3)	DDRC_QDLLCFG	0x0000_0053

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		unfl_mod	ovfl_mod	reserved				bypctl_mod				reserved		bypfc_mod		reserved				limit_mod								byp_mod	dll_updt_en_mod	dll_en_mod	dll_reset_mod
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29]	RO	unfl_mod	DLL underflow status. 0: No uderflow occurs. 1: An underflow occurs.
[28]	RO	ovfl_mod	DLL overflow status. 0: No overflow occurs. 1: An overflow occurs.
[27:25]	RW	reserved	Reserved.
[24:20]	RW	bypctl_mod	ctlout value of the DLL when it is bypassed.
[19]	RW	reserved	Reserved.
[18:16]	RW	bypfc_mod	fcout value of the DLL when it is bypassed.
[15:11]	RW	reserved	Reserved.
[10:4]	RW	limit_mod	Locked bandwidth of the DLL.
[3]	RW	byp_mod	DLL bypass enable. 0: disabled 1: enabled
[2]	RW	dll_updt_en_mod	DLL update enable. 0: disabled 1: enabled

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[1]	RW	dll_en_mod	DLL enable. 0: disabled 1: enabled
[0]	RW	dll_reset_mod	DLL reset. 0: reset 1: deassert reset

DDRC_LVLSKEW

DDRC_LVLSKEW is a DDRPHY data line phase tune control register.

Offset Address	Register Name	Total Reset Value
0x470	DDRC_LVLSKEW	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			dm_skew	reserved			dqs_skew
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:16]	RW	dm_skew	Mask signal delay tune enable by writing data. 0: disabled 1: enabled
[15:4]	RW	reserved	Reserved.
[3:0]	RW	dqs_skew	Data line tune enable. 0: disabled 1: enabled

DDRC_LVLCTRL

DDRC_LVLCTRL is a DDRPHY write level control register.

Offset Address	Register Name	Total Reset Value
0x474	DDRC_LVLCTRL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							wrlvl_allow
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.

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[3:0]	RW	wrlvl_allow	Write level operation enable. 0: disabled 1: enabled N: byte N enableN = 0, 1, 2, or 3

DDRC_LVLSTR

DDRC_LVLSTR is a DDRPHY write level DQS control register.

Offset Address	Register Name	Total Reset Value
0x478	DDRC_LVLSTR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							wrlvl_strobe
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3:0]	RW	wrlvl_strobe	Write level single-cycle enable. 0: idle 1: enabled by writing 1 N: byte N enableN = 0, 1, 2, or 3

DDRC_LVLODT

DDRC_LVLODT is a DDRPHY write level ODT control register.

Offset Address	Register Name	Total Reset Value
0x47C	DDRC_LVLODT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							wrlvl_odt
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	wrlvl_odt	ODT control in write-level mode. 0: disabled 1: enabled

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DDRC_LVLCTL

DDRC_LVLCTL is DDRPHY write level configuration register 0.

Offset Address	Register Name	Total Reset Value
0x480+0x4 x blanes blanes (0–3)	DDRC_LVLCTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clkinv	lvlctl_mod																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	clkinv	Leveling phase select. 0: 0° phase 1: 180° phase
[30:0]	RW	lvlctl_mod	Coarse adjustment value of DQS in write-level mode. 0x0000_0000: 0 delay unit 0x0000_0001: 1 delay unit 0x0000_0003: 2 delay units 0x0000_0007: 3 delay units … 0x7FFF_FFFF: 31 delay units Note: DDRC_CONFIG1[wrlvl_en] determines whether the register is accessible. That is, this register is accessible only when DDRC_CONFIG1[wrlvl_en] is disabled.

DDRC_LVLFC

DDRC_LVLFC is DDRPHY write level configuration register 1.

Offset Address	Register Name	Total Reset Value
0x4B0+0x4 x blanes blanes (0–3)	DDRC_LVLFC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								lvlfc_mod							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved.

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[6:0]	RW	lvlfc_mod	Fine adjustment value of DQS in write-level mode. Note: Do not configure this register.

DDRC_LVLRSP

DDRC_LVLRSP is a DDRPHY write level response register.

Offset Address	Register Name	Total Reset Value
0x4E0	DDRC_LVLRSP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												lvlrsp_mod			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3:0]	RO	lvlrsp_mod	Response is returned in write-level mode. 0: ERROR 1: OK

DDRC_LVLST

DDRC_LVLST is a DDRPHY write level status register.

Offset Address	Register Name	Total Reset Value
0x4E4	DDRC_LVLST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												lvl_ok			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3:0]	RO	lvl_ok	Write level status. 0: failure after initialization is complete 1: success

DDRC_PHYSRST

DDRC_PHYSRST is a DDRPHY soft reset control signal register.

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Offset Address	Register Name	Total Reset Value
0x4F0	DDRC_PHYSRST	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ddrphy_srst
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved.
[0]	RW	ddrphy_srst	DDRPHY reset control. 0: reset 1: deassert reset

DDRC_WRDQS_SKEW

DDRC_WRDQS_SKEW is a DDRPHY write DQS tune register.

Offset Address	Register Name	Total Reset Value
0x500	DDRC_WRDQS_SKEW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				wrdqs_skew											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	wrdqs_skew	DDR write DQS delay tune. 0x0–0x7: count of delay units [3 x (N + 1) – 1:3 x N]: write DQS delay configuration N = 0, 1, 2, or 3 N indicates the write DQS of the corresponding bytelaneN.

DDRC_RDDQS_SKEW

DDRC_WRDQS_SKEW is a DDRPHY read DQS tune register.

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Offset Address	Register Name	Total Reset Value
0x504	DDRC_RDDQS_SKEW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				rddqs_skew											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	rddqs_skew	DDR read DQS delay tune. 0x0–0x7: count of delay units [3 x (N + 1) – 1:3 x N]: read DQS delay configuration N = 0, 1, 2, or 3 N indicates the read DQS of the corresponding BytelaneN.

DDRC_WRDMSKEW

DDRC_WRDMSKEW is a write mask tune configuration register.

Offset Address	Register Name	Total Reset Value
0x508	DDRC_WRDMSKEW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				dm_wr_skew											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	dm_wr_skew	Delay tune for the write data mask signal. 0x0–0x7: count of delay units [3 x (N + 1) – 1:3 x N]: DM delay configuration N = 0, 1, 2, or 3 N indicates DM of the corresponding bytelaneN.

DDRC_WRDQSKEW

DDRC_WRDQSKEW is a DDRPHY write data delay tune register.

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Offset Address	Register Name	Total Reset Value
0x510+0x4 x blanes blanes (0–3)	DDRC_WRDQSKEW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dq_skew_wr_mod								dq_skew_wrsel_mod																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dq_skew_wr_mod	DDR write data delay tune enable. 0: disabled 1: enabled bit[24]: write data delay tune control for DQ0 … bit[31]: write data delay tune control for DQ7
[23:0]	RW	dq_skew_wrsel_mod	Write data delay tune. 0x0–0x7: number of delay units [3 x (N + 1) – 1:3 x N]: DQ write data delay configuration N = 0–7

DDRC_RDDQSKEW

DDRC_RDDQSKEW is a DDRPHY read data delay tune register.

Offset Address	Register Name	Total Reset Value
0x540+0x4 x blanes blanes (0–3)	DDRC_RDDQSKEW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dq_skew_rd_mod								dq_skew_rdsel_mod																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dq_skew_rd_mod	DDR read data delay tune enable. 0: disabled 1: enabled bit[24]: read data delay tune control for DQ0 … bit[31]: read data delay tune control for DQ7

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[23:0]	RW	dq_skew_rdsel_mod	Read data delay tune. 0x0–0x7: number of delay units [3 x (N + 1) – 1:3 x N]: DQN read data delay configuration N = 0–7

DDRC_IOCFG

DDRC_IOCFG is a DDRPHY IO configuration register.

Offset Address	Register Name	Total Reset Value
0x570	DDRC_IOCFG	0x0000_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				lpddr_en	odis_clk			fena_rcv	ddr3	rtt		reserved	sl		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11]	RW	lpddr_en	DDR read DQS single port receive mode enable. 0: disabled Differential DQS mode is used. 1: enabled Single port DQS mode is used.
[10:8]	RW	odis_clk	Output clock enable. odis_clk[n] corresponds to DDR_CLKP/N[n] and the value of *n* is 0, 1, or 2. odis_clk[0] corresponds to bit[8], odis_clk[1] corresponds to bit[9], and odis_clk[2] corresponds to bit[10]. 0: output clock enable of DDR_CLKP/N 1: output clock disable of DDR_CLKP/N
[7]	RW	fena_rcv	Forcible receive enable. 0: disabled 1: enabled
[6]	RW	ddr3	Mode select. 0: DDR2 mode 1: DDR3 mode
[5:4]	RW	rtt	Impedance of the matched resistor (ren75, ren150). 0: disabled 01: impedance of the external resistor/2 1x: impedance of the external resistor/4
[3]	RO	reserved	Reserved.

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[2:0]	RW	sl	Signal slew rate control. 111: highest … 000: lowest

DDRC_IOCMP

DDRC_IOCMP is a DDRPHY I/O compensation configuration register.

Offset Address	Register Name	Total Reset Value
0x580	DDRC_IOCMP	0x0000_0005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															rtt_byp_en	rtt_byp				drv_byp_n				drv_byp_p				drv_byp_en	update_en	mvg_en	comp_e
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved.
[16]	RW	rtt_byp_en	Bypass enable of the compensation circuit with the matched resistor. 0: disabled 1: enabled
[15:12]	RW	rtt_byp	Configured impedance in bypass mode.
[11:8]	RW	drv_byp_n	Configured impedance of the pull-down resistor in bypass mode.
[7:4]	RW	drv_byp_p	Configured impedance of the pull-up resistor in bypass mode.
[3]	RW	drv_byp_en	Bypass enable. 0: disabled 1: enabled
[2]	RW	update_en	Compensation update enable. 0: disabled 1: enabled
[1]	RW	mvg_en	Averaging enable. 0: disabled 1: enabled
[0]	RW	comp_e	Drive and receive enable. 0: disabled 1: enabled

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DDRC_CMPSTATUS0

DDRC_CMPSTATUS0 is DDRPHY IO compensation status register 0.

Offset Address	Register Name	Total Reset Value
0x590	DDRC_CMPSTATUS0	0x0001_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pctl_core																nctl_core															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	pctl_core	Status of the pull-up compensation resistor.
[15:0]	RO	nctl_core	Status of the pull-down compensation resistor.

DDRC_CMPSTATUS1

DDRC_CMPSTATUS1 is DDRPHY IO compensation status register 1.

Offset Address	Register Name	Total Reset Value
0x598	DDRC_CMPSTATUS1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ctl_core											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.
[13:0]	RO	ctl_core	Status of the RTT compensation resistor.

4.2 NAND Flash Controller

4.2.1 Overview

The NAND flash controller (NANDC) provides memory controller interfaces. These interfaces enable the Hi3521 to connect to external NAND flash memories to access data.

4.2.2 Features

The NANDC has the following features:

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- Provides 2 KB (2048 + 320 bytes) on-chip buffer for improving the read speed.
- Supports two CSs and two ready/busy signals and allows two NAND flash memories to share one ready/busy signal.
- Supports NAND flash interfaces with 8-bit data bus.
- Allows the chip to boot from the NAND flash corresponding to CS 0 and supports the NAND flash memory with the page size of 2 KB, 4 KB, or 8 KB.
- Enables or disables error correcting code (ECC) check and error correction. 1-bit/512 bytes, 4-bit/512 bytes, and 24-bit/1024 bytes ECC check and error correction are supported.
- Reports read/write interrupts, erase interrupts, programming complete interrupts, and ECC check error interrupts.
- Reads/writes data with variable lengths.
- Flexibly configures the commands issued by the controller to support various NAND flash command operations including cache read and write.
- Supports interruption in the process of reading and writing the NAND flash to release the shared bus.
- Operates two NAND flash memories in an alternate manner to improve efficiency.
- Supports write protection for the NAND flash and configurable write-protection addresses.
- Supports the lock and lock-down modes and the enabling and disabling of flash lock and flash global lock. By default, flash lock and flash global lock are enabled. The NANDC always reports operation error interrupts if the locked addresses are written.
- Reads NAND flash data in enhanced data out (EDO) mode.

4.2.3 Function Description

4.2.3.1 Block Diagram of NANDC Interfaces

The chip provides two CS signals and two ready/busy signals, so it can connect to NAND flash memories conveniently. If only one ready/busy signal is used, NF_RB0 is required. Figure 4-4 shows the block diagram of NANDC interfaces.

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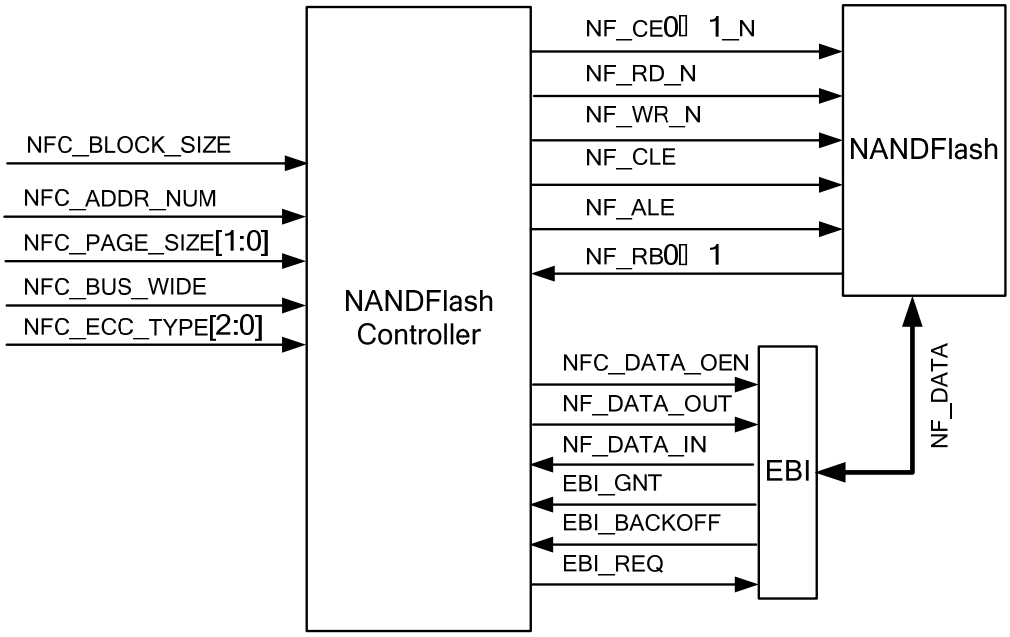
Figure 4-4 Block diagram of NANDC interfaces



4.2.3.2 Function Principle

The data is generally stored in the NAND flash by blocks and pages. Each block consists of several pages. Before writing data to the NAND flash, you must erase it by blocks. Then, you can read/write the NAND flash by pages.

The commands for operating the NAND flash vary according to vendors. That is, the specific commands are subject to component manuals.

A typical read operation is performed as follows:

Step 1 Transmit the read command 0x00 to the NAND flash.

Step 2 Transmit the read start address. The start address consists of the internal page address, page address, and block address. For details, see the NAND flash manuals provided by relevant vendors.

Step 3 Transmit the read acknowledgement command 0x30. The NAND flash pulls the RB signal low. This indicates that the NAND flash is being read. About 25 μs later, the RB signal becomes high. This indicates that data of the NAND flash is ready.

Step 4 The CPU reads data from the NAND flash through the NF_RD_N signal.

---End

Figure 4-5 shows the typical timing when the NANDC reads the data of a page size from the NAND flash.

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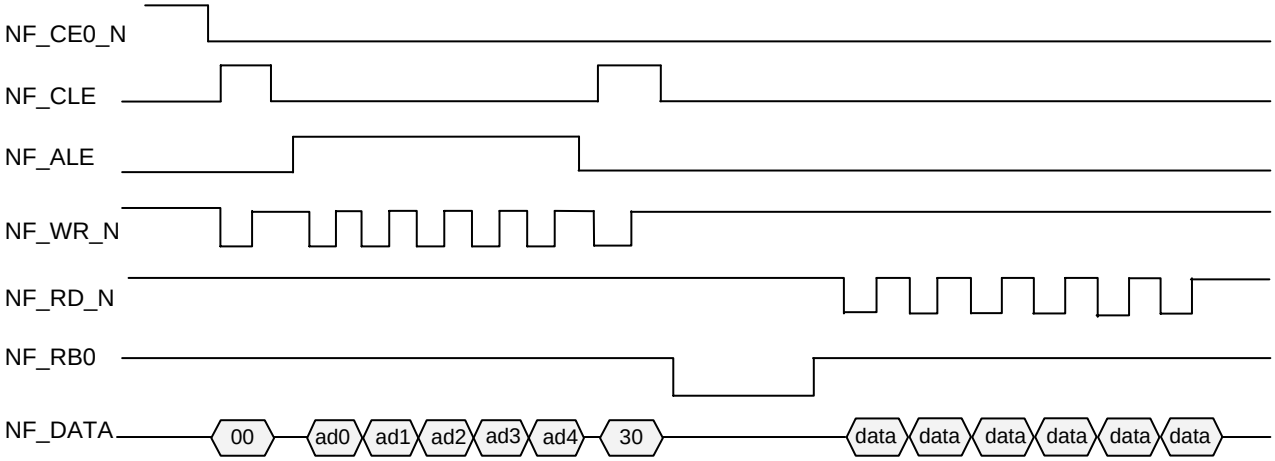
Figure 4-5 Typical timing when the NANDC reads the data of a page size from the NAND flash



A typical programming operation (writing data) is performed as follows:

Step 1 Transmit the programming command 0x80 to the NAND flash.

Step 2 Transmit the start address from which data is written. The start address consists of the internal page address, page address, and block address. For details, see the NAND flash manuals provided by relevant vendors.

Step 3 Write data to the internal buffer of the NAND flash.

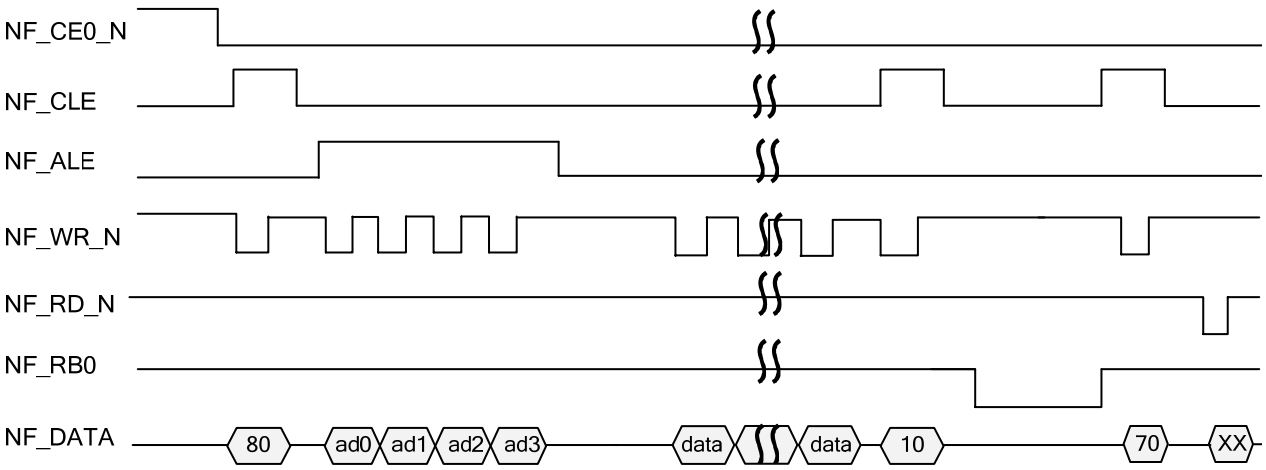
Step 4 The CPU sends the programming acknowledgement command 0x10. In this case, the NAND flash pulls the RB signal low. This indicates that the NAND flash is being programmed. About 200 ms later, the RB signal becomes high. This indicates that the programming operation is complete.

Step 5 The CPU transmits the read status command 0x70 to read the status data that indicates whether the programming operation is successful.

---End

Figure 4-6 shows the timing when NANDC starts programming.

Figure 4-6 Timing when the NANDC starts programming



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4.2.4 Operating Mode

Mapping Mode of the NAND Flash

When the Hi3521 boots, you need to select the NAND flash type by setting the pull-up or pull-down modes of the pins NF_BOOT_PIN0 (multiplexed with the LCD_DV pin), NF_BOOT_PIN1 (multiplexed with the SIO2_DOUT pin), NF_BOOT_PIN2 (multiplexed with the SPI_CSN1 pin), NF_BOOT_PIN3 (multiplexed with the SPI_CSN2 pin), and NF_BOOT_PIN4 (multiplexed with the SPI_CSN3 pin). Note that you must set the pull-up or pull-down modes of pins properly no matter whether the system boots from the NAND flash. Otherwise, the system fails to boot.

Table 4-11 describes the mapping modes of pins.

Table 4-10 Mapping modes of pins

{NF_BOOT_PIN4, NF_BOOT_PIN3, NF_BOOT_PIN2, NF_BOOT_PIN1, NF_BOOT_PIN0}	Page Size	ecc_type	block_size	addr_num	bus_wide	Remarks
00000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
00001	001	001	00	1	0	2 KB page size 1-bit ECC 64 pages/block 5 addresses
00010	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
00011	001	010	00	1	0	2 KB pages size 4-bit ECC 64 pages/block 5 addresses
00100	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
00101	001	100	00	1	0	2 KB pages size 24-bit ECC 64 pages/blocks 5 addresses
00110	001	001	00	0	0	2 KB pages size 1-bit ECC 64 pages/blocks 4 addresses
00111	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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{NF_BOOT_PIN4, NF_BOOT_PIN3, NF_BOOT_PIN2, NF_BOOT_PIN1, NF_BOOT_PIN0}	Page Size	ecc_type	block_size	addr_num	bus_wide	Remarks
01000	010	010	01	1	0	4 KB pages size 4-bit ECC 128 pages/blocks 4 addresses
01001	010	010	00	1	0	4 KB pages size 4-bit ECC 64 pages/blocks 4 addresses
01010	001	010	00	0	0	2 KB pages size 4-bit ECC 64 pages/blocks 4 addresses
01011	010	100	01	1	0	4 KB pages size 24-bit ECC 128 pages/blocks 4 addresses
01100	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
01101	011	100	01	1	0	8 KB pages size 24-bit ECC 128 pages/blocks 4 addresses
01110	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
01111	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
10000	011	100	00	1	0	8 KB pages size 24-bit ECC 64 pages/blocks 4 addresses
10001	010	100	00	1	0	4 KB pages size 24-bit ECC 64 pages/blocks 4 addresses
10010	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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{NF_BOOT_PIN4, NF_BOOT_PIN3, NF_BOOT_PIN2, NF_BOOT_PIN1, NF_BOOT_PIN0}	Page Size	ecc_type	block_size	addr_num	bus_wide	Remarks
10011	010	001	00	1	0	4 KB pages size 1-bit ECC 64 pages/blocks 4 addresses
10100	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
10101	001	010	01	1	0	2 KB pages size 4-bit ECC 128 pages/blocks 4 addresses
10110	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
10111	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11001	001	100	01	1	0	2 KB pages size 24-bit ECC 128 pages/blocks 4 addresses
11010	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11011	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11100	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11101	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11110	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11111	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Clock Gating

When the NAND flash is not used, you can disable the working clock of the NANDC. To disable the clock, perform the following steps:

Step 1 Read NFC_STATUS[nfc_ready] of the NANDC.

Step 2 If NFC_STATUS[nfc_ready] is 1 and the NAND flash is not read and written by the software, go to step 3; otherwise, go to step 1.

Step 3 Write 0 to PERI_CRG52[nfc_cken] to disable the clock.

---End

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Soft Reset

After the NANDC is enabled by writing data to NFC_OP, if NFC_STATUS[nfc_ready] is changed to 0 and cannot be changed to 1 for a long period, the NANDC is abnormal and a soft reset operation is required. The maximum duration depends on the NAND flash. For the SLC flash, it is less than 4 ms; for the MLC, it is less than 11 ms.

The NANDC can be soft-reset by writing 1 to PERI_CRG52[nfc_srst_req]. After reset, each configuration register is restored to its default value. Therefore, these registers must be reinitialized. In addition, a reset command must be sent to the NAND flash after soft reset (if the NAND flash supports reset) to ensure its reliability.

NOTE

The NANDC supports the lock function. If this function is enabled, it can be disabled until a hard reset is performed.

Boot Configuration Pins

The NANDC supports the NAND boot function and the memory with the page size of 2 KB, 4KB, or 8 KB. The NANDC can boot from the NAND flash corresponding only to CS 0.

After reset, the boot mode of the NANDC depends on the levels of the NANDC boot configuration pins. When the NANDC is reset, the levels of the boot configuration pins are sampled. After sampling, the operating status of the NANDC is not affected by the levels. Table 4-11 shows the boot configuration pins.

Table 4-11 Boot configuration pins

Register	I/O	Description
NFC_ADDR_NUM	I	Number of addresses sent to the NAND flash by the NANDC during booting. 0: 4 address cycles 1: 5 address cycles.
NFC_PAGE_SIZE	I	Page size of the NAND flash during booting. 01: 2 KB 10: 4 KB 11: 8 KB Other values: reserved
NFC_BUS_WIDE	I	Bus width of the NAND flash during booting. 0: 8 bits 1: 16 bits
NFC_ECC_TYPE[2:0]	I	ECC mode during booting. 000: disabled 001: 1-bit mode 010: 4-bit mode 100: 24-bit mode Other values: reserved

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Register	I/O	Description
NFC_BLOCK_SIZE	I	Block size of the NAND flash during booting. 0: 64 pages 1: 128 pages

Boot Mode

By default, the NANDC is in boot mode and the NANDC can be booted only from CS 0 corresponding to the NAND flash.

In boot mode:

- Data stored in the 1 MB address can be read by the CPU.
- Bad blocks can be automatically detected and skipped.
- When the NANDC boots from the NAND flash, the NANDC automatically sends a command to read the corresponding page of the NAND flash based on the addresses read by the CPU and then returns the corresponding data.
- Data cannot be written to the internal buffer through the CPU.
- The boot configuration pins must be configured properly according to the models of the connected NAND flash.

Normal Mode

The NANDC is switched to the normal mode when NFC_CON[op_mode] is set to 1. In this mode, the CPU can erase, program, and read the NAND flash. The NANDC is switched to the quick ECC error correction clock when PERI_CRG52[nfc_clk_sel] is set to 1.

Setting the Address of the NAND Flash

The NANDC does not translate addresses. According to the number of addresses configured by the command configuration register, the NANDC sends the values of lower-bit and upper-bit address registers to the NAND flash directly. Therefore, the software needs to translate the address of the CPU into the address of the NAND flash and write the translated address to the address register. For details about the address configuration requirements on each flash memory, see the user manuals of the corresponding NAND flash.

Table 4-12 describes the requirements on the addresses of Samsung K9F2G08U0M memory. Its capacity is 256 MB x 8 bits and its page size is 2 KB. A0 to A11 indicate the internal page addresses (column addresses) and A12 to A27 indicate the page addresses (row addresses).

Table 4-12 Addresses of the K9F2G08U0M

Cycle	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
First cycle	A0	A1	A2	A3	A4	A5	A6	A7
Second cycle	A8	A9	A10	A11	0	0	0	0
Third cycle	A12	A13	A14	A15	A16	A17	A18	A19

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Cycle	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
Fourth cycle	A20	A21	A22	A23	A24	A25	A26	A27

Table 4-13 describes the requirements on the addresses of Samsung K9GAG08X0M memory. Its capacity is 2 GB x 8 bits and its page size is 4 KB. A0 to A12 indicate the internal page addresses (column addresses) and A13 to A31 indicate the page addresses (row addresses).

Table 4-13 Addresses of the K9GAG08X0M

Cycle	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
First Cycle	A0	A1	A2	A3	A4	A5	A6	A7
Second Cycle	A8	A9	A10	A11	A12	0	0	0
Third cycle	A13	A14	A15	A16	A17	A18	A19	A20
Fourth cycle	A21	A22	A23	A24	A25	A26	A27	A28
Fifth cycle	A29	A30	A31	0	0	0	0	0

Address Mapping

In normal mode, the address mapping of the NANDC is as follows:

- The base address of the internal buffer of the NANDC is 0x5000_0000.
- The base address of the internal register area of the NANDC is 0x1000_0000.

Operation Commands

The NAND flash memories provide certain advanced commands. Table 4-14 shows the common commands for operating NAND flash memories.

Table 4-14 Common commands for operating the NAND flash

Description	First Cycle	Second Cycle	Remarks
Read	00H	30H	None
Programming	80H	10H	None
Block erase	60H	D0H	None
Read ID	90H	None	None
Read status	70H	None	None

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Description	First Cycle	Second Cycle	Remarks
Reset	FFH	None	None

Data Storage Structure

The size of the internal buffer of the NANDC is (2048 + 320) bytes. This section describes the storage structures of the data in the NANDC buffer. The data is read from or written to the NAND flash.

- 1-Bit ECC Mode
  - 2 KB (2048 + 64 Bytes) Page Size

    2048-byte valid data is stored in the buffer ranging from 0x000 to 0x7FF; 64-byte spare data is stored in the buffer ranging from 0x800 to 0x83F.

    The data structures of the driver, NANDC buffer, and NAND flash are the same, as shown in Figure 4-7.

Figure 4-7 Data storage structure of the NAND flash with the page size of 2 KB (2048 + 64 bytes) in 1-bit ECC mode

B: indicates bad block, 2 bytes
CTRL: indicates the control area for the software, 42 bytes

DECC: indicates the ECC code in the data area, 12 bytes
SECC: indicates the bad block flag and ECC code in the CTRL area, 8 bytes. (Starting from the bad block flag, each 16-byte data is used to calculate a 2-byte check code. During calculation, the position data of DECC and SECC is masked as 0.)

  - 4 KB (4096 Bytes +56 Bytes) Page Size

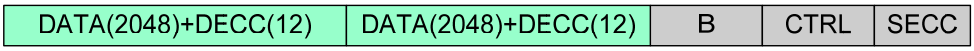
    Figure 4-8 shows the (4096 + 56)-byte data structure of the driver. In the NAND flash, data is stored in (2048 + 12)-byte ECC code alternate mode (4096 + 24 bytes in total), as shown in Figure 4-9.

Figure 4-8 (4096 + 56)-byte data structure of the driver in 1-bit ECC mode

B: indicates bad block, 2 bytes

CTRL: indicates the control area for the software, 54 bytes

Figure 4-9 Data structure of the NAND flash in 1-bit ECC mode



B: indicates bad block, 2 bytes

CTRL: indicates the control area for the software, 54 bytes

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SECC: indicates the bad block flag and ECC code in the CTRL area, 8 bytes. (Starting from the bad block flag, each 16-byte data is used to calculate a 2-byte check code. During calculation, the position data of SECC is masked as 0.)

- 4-Bit ECC Mode

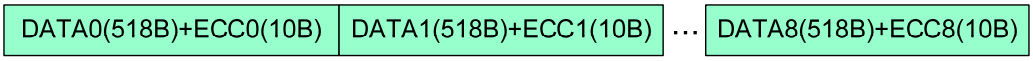
  4 KB (4096 + 128 Bytes) Page Size

  For the device with 4 KB page size, the available spare area for the software is 46 bytes. Figure 4-10 shows the (4096 + 128)-byte data structure of the driver. Figure 4-11 shows the structure of the data written to the NAND flash. The valid data of the software is divided into eight 518-byte data blocks. Each data block is used to calculate the ECC code once. The data written to the NAND flash is automatically stored in alternate mode of 518-byte data + 10-byte ECC code. In general, the data is stored in eight groups.

Figure 4-10 (4096 + 48)-byte data structure of the driver in 4-bit ECC mode

B: indicates bad block, 2 bytes CTRL: indicates the control area for the software, 46 bytes

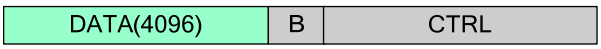
Figure 4-11 (4096 + 128)-byte data structure of the NAND flash in 4-bit ECC mode



- 24-Bit ECC Mode
  - 4 KB Page Size

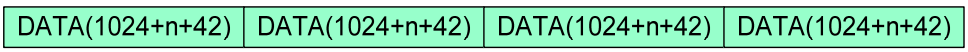
    Figure 4-12 shows the (4096 + 32)-byte data structure of the driver when the page size is 4 KB. When data is written to the NAND flash, the data is divided into four (1024 + n)-byte data blocks (*n* can be set to 4 or 8). Each data block is used to calculate a 42-byte ECC code. Then the data blocks and ECC code are stored alternately. The total size of the data and code is 4096 + 200 bytes, as shown in Figure 4-13.

Figure 4-12 (4096 + 32)-byte data structure of the driver in 24-bit ECC mode



B: indicates bad block, 2 bytes CTRL: indicates the control area for the software, 30 bytes (when *n* is set to 8)

Figure 4-13 (4096 + 200)-byte data structure of the NAND flash in 24-bit ECC mode (n = 8)



In boot mode, the value of *n* is 8 bytes by default.

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- 8 KB Page Size

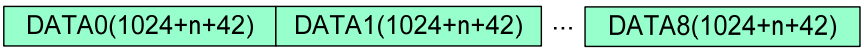
  Figure 4-14 shows the (8192 + 32)-byte data structure of the driver when the page size is 8 KB. When data is written to the NAND flash, the data is divided into eight (1024 + n)-byte data blocks (*n* is 4 or 8). Each data block is used to calculate a 42-byte ECC code. Then the data blocks and ECC code are stored alternately, as shown in Figure 4-15.

Figure 4-14 (8192 + 32)-byte data structure of the driver in 24-bit ECC mode

B: indicates bad block, 2 bytes

CTRL: indicates the control area for the software, 30 bytes (when *n* is set to 4)

Figure 4-15 (8192 + 368)-byte data structure of the NAND flash in 24-bit ECC mode (n = 4)



In boot mode, the value of *n* is 8 bytes by default.

Initialization

To initialize the NAND Flash perform the following steps:

Step 1 Write 1 to NFC_CON[op_mode] to enter the normal mode, set NFC_CON[bus_width] and NFC_CON[page_size] based on the page size and bit width of the interconnected component and set NFC_CON[rb_sel] based on the number of CSs and the number of ready_busy signals of the interconnected component, write NFC_CON[ecc_type] to set the check and error correction modes.

Step 2 Write to NFC_PWIDTH based on the timing requirements of the connected component.

Step 3 In query mode, write the interrupt enable register NFC_INTEN to mask all the interrupts; in interrupt mode, enable only the op_done interrupt and mask other interrupts.

---End

Erasing Data in the NAND Flash

To erase data in the NAND flash perform the following steps:

Step 1 Write the programming page address to NFC_ADDRL and NFC_ADDRH and write the erase command 0x0070_D060 to NFC_CMD.

Step 2 Write 0x369 to NFC_OP and enable the NANDC to erase the NAND flash. Assume that the NAND flash chip needs three addresses and the operation is performed on CS 0.

Step 3 In query mode, check whether NFC_STATUS[nfc_ready] is 1. If the value is 1, go to step 4; otherwise, continue the query. In interrupt mode, check whether NFC_INTS[op_done] is 1. If the value is 1, go to step 4.

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Step 4 Read NFC_STATUS[nf_status] to check whether the erase operation is successful.

---End

Writing Data to the NAND Flash in DMA Mode

To write data to the NAND Flash in DMA mode, perform the following steps:

Step 1 Set the parameters of NFC_CON such as page size, ecc_type, and bus_wide based on the type of the interconnected component. If the error correction type is 24-bit ECC check, configure NFC_OP_PARA[ext_len].

Step 2 The CPU configures NFC_BADDR_D, and NFC_BADDR_OOB. The CPU also needs to configure NFC_DMA_LEN if it is in ECC0 mode.

Step 3 The CPU writes to NFC_DMA_CTRL and enables the NANDC to write to the NAND flash.

Step 4 The CPU waits until the NANDC transmits a DMA transfer done interrupt.

----End

Reading the NAND Flash in DMA Mode

To read data to the NAND Flash in DMA mode, perform the following steps:

Step 1 Set the parameters of NFC_CON such as page size, ecc_type, and bus_wide based on the type of the interconnected component. If the error correction type is 24-bit ECC check, configure NFC_OP_PARA[ext_len].

Step 2 The CPU configures NFC_BADDR_D, NFC_DMA_LEN, NFC_RD_LOGIC_ADDR, and NFC_RD_LOGIC_LEN.

Step 3 The CPU writes to NFC_DMA_CTRL and enables the NANDC to read the NAND flash.

Step 4 The CPU waits until the NANDC transmits a DMA transfer done interrupt.

----End

4.2.5 Precautions

Take the following precautions:

- The operation commands supported by the NAND flash memories vary according to vendors. Therefore, the command register NFC_CMD must be configured properly according to memory manuals. In addition, the number of address cycles required by the NAND flash memories of different capacities is different. You need to configure the address_cycles field of NFC_OP according to memory manuals. Furthermore, the timings supported by memories are different. Therefore, the read/write pulse width register NFC_PWIDTH and operation interval register NFC_OPIDLE must be configured properly according to memory manuals.
- After configuring related registers and buffer, write to the NFC_OP register to enable the NANDC to read and write to the flash memory. After that, do not write to related registers; otherwise, the NANDC or flash memory may be abnormal.
- After enabling the NAND flash to be read and written by writing to NFC_OP, do not read and write the buffer of the NANDC when the flag NFC_STATUS[nfc_ready] is 0. Otherwise, error data may be returned.

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4.2.6 NANDCRegister Summary

Table 4-15 describes the NANDC registers.

Table 4-15 Summary of NANDC registers (base address; 0x1000_0000)

Offset Address	Register	Description	Page
0x00	NFC_CON	NANDC configuration register	4-76
0x04	NFC_PWIDTH	Read/write pulse width configuration register	4-78
0x08	NFC_OPIDLE	Operation interval configuration register	4-78
0x0C	NFC_CMD	Command word configuration register	4-79
0x10	NFC_ADDRL	Lower-bit address configuration register	4-79
0x14	NFC_ADDRH	Upper-bit address configuration register	4-80
0x18	NFC_DATA_NUM	Read/written data count configuration register	4-80
0x1C	NFC_OP	Operation register	4-80
0x20	NFC_STATUS	Status register	4-82
0x24	NFC_INTEN	Interrupt enable register	4-83
0x28	NFC_INTS	Interrupt status register	4-84
0x2C	NFC_INTCLR	Interrupt clear register	4-85
0x30	NFC_LOCK	Lock address configuration register	4-86
0x34	NFC_LOCK_SA0	Lock start address 0 configuration register	4-87
0x38	NFC_LOCK_SA1	Lock start address 1 configuration register	4-87
0x3C	NFC_LOCK_SA2	Lock start address 2 configuration register	4-88
0x40	NFC_LOCK_SA3	Lock start address 3 configuration register	4-89
0x44	NFC_LOCK_EA0	Lock end address 0 configuration register	4-89
0x48	NFC_LOCK_EA1	Lock end address 1 configuration register	4-90
0x4C	NFC_LOCK_EA2	Lock end address 2 configuration register	4-90
0x50	NFC_LOCK_EA3	Lock end address 3 configuration register	4-91
0x54	NFC_EXPCMD	Extended page command register	4-91
0x58	NFC_EXBCMD	Extended block command register	4-92
0x5C	NFC_ECC_TEST	ECC test register	4-92
0x60	NFC_DMA_CTRL	DMA control register	4-93

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Offset Address	Register	Description	Page
0x64	NFC_BADDR_D	Base address register of the data transfer area.	4-95
0x68	NFC_BADDR_OOB	Base address register of the out-of-band (OOB) area.	4-95
0x6C	NFC_DMA_LEN	Transfer length register.	4-95
0x70	NFC_OP_PARA	Operation parameter register	4-96
0x74	NFC_VERSION	Controller version register	4-97
0x78	NFC_BUF_BADDR	Base address register of the NANDC buffer	4-97
0x7C	NFC_RD_LOGIC_ADDR	Logic address register for reading the NAND flash in DMA mode	4-98
0x80	NFC_RD_LOGIC_LEN	Logic length register for reading the NAND flash in DMA mode	4-99
0x90	NFC_FIFO_EMPTY	Internal FIFO status register	4-99
0x94	NFC_BOOT_SET	Boot parameter configuration register	4-99
0x98	NF_STATUS	NAND flash status register	4-100

4.2.7 Register Description

NFC_CON

NFC_CON is a NANDC configuration register.

Offset Address	Register Name	Total Reset Value
0x00	NFC_CON	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				edo_en	ecc_type			rb_sel	cs_ctrl	reserved		bus_width		pagesize		op_mode	
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	1	0	1	?	0	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved.

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[11]	RW	edo_en	NAND flash data read enable in EDO mode. 0: normal mode 1: EDO mode This function must be used according to the requirements of specific memories.
[10:8]	RW	ecc_type	ECC mode select. 000: non-ECC mode 001: 1-bit mode 010: 4-bit mode 011: reserved 100: 24-bit mode for 1 KB 101–111: reserved The reset value depends on the NFC_ECC_TYPE pin.
[7]	RW	rb_sel	This field is valid when multiple external NAND flash memories (multiple CSs) are connected. 0: The NAND flash memories share a ready/busy signal. 1: The NAND flash memories use their own ready/busy signals. When only one NAND flash is connected, only CS0 and ready/busy 0 are used.
[6]	RW	cs_ctrl	CS control. 0: When the NAND flash is busy, the CS signal is fixed at 0. 1: When the NAND flash is busy, the CS signal is set to 1. This mode maps to the "cs do not care" mode of the NAND flash.
[5:4]	-	reserved	Reserved.
[3]	RW	bus_width	Data line width of the NAND flash. 0: 8 bits. 1: 16 bits The reset value depends on the NFC_BUS_WIDE pin.
[2:1]	RW	pagesize	Page size of the NAND flash. 01: 2 KB 10: 4 KB 11: 8 KB Other values: reserved The reset value depends on the NFC_PAGE_SIZE pin.
[0]	RW	op_mode	Operating mode of the NANDC. 0: boot mode 1: normal mode

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NFC_PWIDTH

NFC_PWIDTH is a read/write pulse width configuration register.

Offset Address	Register Name	Total Reset Value
0x04	NFC_PWIDTH	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				rw_hcnt				r_lcnt				w_lcnt			
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	1	1	0	0	1	1	0	0	1	1

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved.
[11:8]	RW	rw_hcnt	High-level width of the read/write signal of the NAND flash. 0x0–0xF: 1–16 clock cycles.
[7:4]	RW	r_lcnt	Low-level width of the read signal of the NAND flash. 0x0–0xF: 1–16 clock cycles.
[3:0]	RW	w_lcnt	Low-level width of the write signal of the NAND flash. 0x0–0xF: 1–16 clock cycles.

NFC_OPIDLE

NFC_OPIDLE is an operation interval configuration register.

Offset Address	Register Name	Total Reset Value
0x08	NFC_OPIDLE	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								frb_wait				cmd1_wait				addr_wait				write_data_wait				cmd2_wait				frb_idle			
Reset	?	?	?	?	?	?	?	?	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:20]	RW	frb_wait	When a number of cycles are delayed after a read/write command is sent, the ready signal is detected to check whether it becomes high. The number of delay cycles is frb_wait x 8.
[19:16]	RW	cmd1_wait	Number of wait cycles after command 1 is sent. 0x0–0xF: 1–16 clock cycles.
[15:12]	RW	addr_wait	Number of wait cycles after the address is sent. 0x0–0xF: 1–16 clock cycles.

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[11:8]	RW	write_data_wait	Number of wait cycles after data is written. 0x0–0xF: 1–16 clock cycles.
[7:4]	RW	cmd2_wait	Number of wait cycles after command 2 is sent. 0x0–0xF: 1–16 clock cycles.
[3:0]	RW	frb_idle	A read signal can be sent only when a number of cycles are delayed after the ready signal of the NAND flash becomes high. The number of delay cycles is frb_idle x 8.

NFC_CMD

NFC_CMD is a command word configuration register.

Offset Address	Register Name	Total Reset Value
0x0C	NFC_CMD	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								read_status_cmd								cmd2								cmd1							
Reset	?	?	?	?	?	?	?	?	0	1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	read_status_cmd	Read status command word.
[15:8]	RW	cmd2	Command 2 that is sent to the NAND flash by the NANDC.
[7:0]	RW	cmd1	Command 1 that is sent to the NAND flash by the NANDC.

NFC_ADDRL

NFC_ADDRL is a lower-bit address configuration register.

Offset Address	Register Name	Total Reset Value
0x10	NFC_ADDRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	addr_l																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	addr_l	Lower 32-bit address of the NAND flash.

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NFC_ADDRH

NFC_ADDRH is an upper-bit address configuration register.

Offset Address	Register Name	Total Reset Value
0x14	NFC_ADDRH	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																addr_h															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	addr_h	Upper 16-bit address of the NAND flash.

NFC_DATA_NUM

NFC_DATA_NUM is a read/written data count configuration register.

Offset Address	Register Name	Total Reset Value
0x18	NFC_DATA_NUM	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				nfc_data_num											
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	1	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved.
[11:0]	RW	nfc_data_num	Number of data segments that are read and written randomly by the NANDC. The maximum value is 2368 bytes. Note: This field is valid only when ecc_type is 00.

NFC_OP

NFC_OP is an operation register.

Offset Address	Register Name	Total Reset Value
0x1C	NFC_OP	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				address_cycles				nf_cs				cmd1_en	addr_en	write_data_en	cmd2_en	wait_ready_en	read_data_en	read_status_en

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Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved.
[11:9]	RW	address_cycles	Number of address cycles sent to the NAND flash.
[8:7]	RW	nf_cs	NAND flash CS signal select. 00: CS 0 01: CS 1 Other values: reserved
[6]	RW	cmd1_en	Command 1 transmit enable. 0: disabled 1: enabled
[5]	RW	addr_en	NAND flash address write enable. 0: disabled 1: enabled
[4]	RW	write_data_en	NAND flash data write enable. 0: disabled 1: enabled Note: read_data_en and write_data_en cannot be 1 at the same time.
[3]	RW	cmd2_en	Command 2 transmit enable. 0: disabled 1: enabled
[2]	RW	wait_ready_en	Wait ready/busy high enable. 0: disabled 1: enabled
[1]	RW	read_data_en	NAND flash data read enable by starting to read the state machine. 0: disabled 1: enabled Note: read_data_en and write_data_en cannot be 1 at the same time.

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[0]	RW	read_status_en	When this bit is 1, the command 0x70 for reading the status is sent to the NAND flash and the status data is read from the NAND flash. After that, the returned data is written to the NFC_STATUS field of the NANDC status register instead of the internal buffer. After the NAND flash is erased and programmed, the results need to be read to check whether the operations are successful. If this bit is enabled, the operations such as erasing and programming can be performed at a time, and the data indicating whether the operation is successful can be returned from the NAND flash. In this way, the CPU intervention is reduced. Note: When read_data_en is 1, this bit is invalid.

NFC_STATUS

NFC_STATUS is a status register.

Offset Address	Register Name	Total Reset Value
0x20	NFC_STATUS	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				nf_status								reserved			nf1_ready	nf0_ready	nfc_ready
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved.
[12:5]	RO	nf_status	Status data read from the NAND flash. This field is valid only when both NFC_OP[read_status] and NFC_STATUS[nfc_ready] are 1.
[4:3]	-	reserved	Reserved.
[2]	RO	nf1_ready	Status of the ready/busy signal of the NAND flash corresponding to CS 1. This bit is valid when multiple flash memories are connected and they use their own ready_busy signals. This is because multiple NAND flash memories share a ready/busy signal by default. The reset value of the bit is 0.
[1]	RO	nf0_ready	Status of the ready/busy signal of the NAND flash corresponding to CS 0. This bit is valid when multiple flash memories are connected and they use their own ready_busy signals. This is because multiple NAND flash memories share a ready/busy signal by default. The reset value of the bit is 0.
[0]	RO	nfc_ready	Status of the ready/busy signal of the NANDC.

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			0: The NANDC is working. 1: The operation is complete and the next command can be received. When NFC_OP is written to start a NANDC operation, the bit is cleared automatically.

NFC_INTEN

NFC_INTEN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x24	NFC_INTEN	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							wr_lock_en	ahb_op_en	err_invalid	err_valid	reserved		cs1_done_en	cs0_done_en	op_done_en
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved.
[8]	RW	wr_lock_en	Lock address write error interrupt enable. 0: disabled 1: enabled
[7]	RW	ahb_op_en	CPU read/write NANDC buffer error interrupt enable when the NANDC is reading/writing data from/to the NAND flash. 0: disabled 1: enabled
[6]	RW	err_invalid	Uncorrectable error interrupt.
[5]	RW	err_valid	Correctable error interrupt.
[4:3]	-	reserved	Reserved.
[2]	RW	cs1_done_en	CS 1 ready/busy signal going high interrupt enable. 0: disabled 1: enabled
[1]	RW	cs0_done_en	CS 0 ready/busy signal going high interrupt enable. 0: disabled 1: enabled
[0]	RW	op_done_en	Current operation done enable of the NANDC. 0: disabled 1: enabled

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NFC_INTS

NFC_INTS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x28	NFC_INTS	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							wr_lock_en	ahb_op_en	err_invalid	err_vavid	reserved		csl_done	cs0_done	op_done
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved.
[8]	RO	wr_lock_en	Interrupt generated when the lock address is written. 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	ahb_op_en	Interrupt generated when the CPU reads and writes the NANDC buffer in the process of reading/writing data from/to the NAND flash by the NANDC. 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	err_invalid	Uncorrectable error interrupt. 0: No interrupt is generated. 1: An interrupt is generated. In 1-bit ECC mode, if errors occur in two or more bits in the checked 512-byte data, an interrupt is generated. In 4-bit ECC mode, if errors occur in five or more bits in the checked 512-byte data, an interrupt is generated. In 8-bit ECC mode, if errors occur in eight or more bits in the checked 512-byte data, an interrupt is generated.
[5]	RO	err_vavid	Correctable error interrupt. 0: No interrupt is generated. 1: An interrupt is generated. In 1-bit ECC mode, if an error occurs in one bit in the checked 512-byte data, an interrupt is generated. In 4-bit ECC mode, if errors occur in one to four bits in the checked 512-byte data, an interrupt is generated. In 8-bit ECC mode, if errors occur in one to eight bits of the checked 512-byte data, an interrupt is generated.

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[4:3]	-	reserved	Reserved.
[2]	RO	cs1_done	CS 1 ready/busy signal going high interrupt. 0: No interrupt is generated. 1: An interrupt is generated. This bit is valid when two flash memories are connected and the two flash memories use their own ready/busy signals. Otherwise, the bit is fixed at 0.
[1]	RO	cs0_done	CS 0 ready/busy signal going high interrupt. 0: No interrupt is generated. 1: An interrupt is generated. This bit is valid when two flash memories are connected and the two flash memories use their own ready/busy signals. Otherwise, the bit is fixed at 0.
[0]	RO	op_done	Current operation done interrupt of the NANDC. 0: No interrupt is generated. 1: An interrupt is generated. After NFC_OP is written, the bit is automatically cleared.

NFC_INTCLR

NFC_INTCLR is an interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x2C	NFC_INTCLR	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							wr_lock_en	ahb_op_en	r_5bit_err_clr	r_4bit_err_clr	reserved			cs1_done_clr	cs0_done_clr	op_done_clr
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved.
[8]	WO	wr_lock_en	wr_lock_en interrupt clear. 0: not cleared 1: cleared
[7]	WO	ahb_op_en	ahb_op_en interrupt clear. 0: not cleared 1: cleared

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[6]	WO	r_5bit_err_clr	r_5bit_err interrupt clear. 0: not cleared 1: cleared
[5]	WO	r_4bit_err_clr	r_4bit_err interrupt clear. 0: not cleared 1: cleared
[4:3]	-	reserved	Reserved.
[2]	WO	cs1_done_clr	cs1_done interrupt clear. 0: not cleared 1: cleared
[1]	WO	cs0_done_clr	cs0_done interrupt clear. 0: not cleared 1: cleared
[0]	WO	op_done_clr	op_done interrupt clear. 0: not cleared 1: cleared

NFC_LOCK

NFC_LOCK is a lock address configuration register.

Offset Address	Register Name	Total Reset Value
0x30	NFC_LOCK	-

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved							lock_excmd_en	lock_en	global_lock_en	lock_down
Reset	? ? ? ?	? ? ? ?	? ? ? ?	? ? ? ?	? ? ? ?	? ? ? ?	? ? ? ?	0	0	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved.
[3]	RW	lock_excmd_en	Protection address write-protection enable according to the extended write command (new commands may be added to new memories). 0: disabled 1: enabled

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[2]	RW	lock_en	Flash lock enable. When this control bit is 1, if the erased or programmed address is between the start lock address and the end lock address, the erasing and programming operations are invalid. 0: disabled 1: enabled
[1]	RW	global_lock_en	Flash global lock enable. When this bit is 1, the NAND flash cannot be erased or programmed. 0: disabled 1: enabled
[0]	RW	lock_down	NAND flash lock mode. 0: lock mode 1: lock-down mode. After the value 1 is written, this bit cannot be written. In addition, this bit can be cleared only when a hard reset is performed.

NFC_LOCK_SA0

NFC_LOCK_SA0 is lock start address 0 configuration register.

Offset Address	Register Name	Total Reset Value
0x34	NFC_LOCK_SA0	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flash_lock_cs				flash_lock_addr0															
Reset	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.
[20:19]	RW	flash_lock_cs	NAND flash lock CS. 00: CS 0 01: CS 1 Other values: reserved
[18:0]	RW	flash_lock_addr0	Lock start address 0. The LSB maps to the fifth row address of the NAND flash.

NFC_LOCK_SA1

NFC_LOCK_SA1 is lock start address 1 configuration register.

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Offset Address	Register Name	Total Reset Value
0x38	NFC_LOCK_SA1	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flash_lock_cs				flash_lock_addr1															
Reset	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.
[20:19]	RW	flash_lock_cs	NAND flash lock CS. 00: CS 0 01: CS 1 Other values: reserved
[18:0]	RW	flash_lock_addr1	Lock start address 1. The LSB maps to the fifth row address of the NAND flash.

NFC_LOCK_SA2

NFC_LOCK_SA2 is lock start address 2 configuration register.

Offset Address	Register Name	Total Reset Value
0x3C	NFC_LOCK_SA2	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flash_lock_cs				flash_lock_addr2															
Reset	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.
[20:19]	RW	flash_lock_cs	NAND flash lock CS. 00: CS 0 01: CS 1 Other values: reserved
[18:0]	RW	flash_lock_addr2	Lock start address 2. The LSB maps to the fifth row address of the NAND flash.

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NFC_LOCK_SA3

NFC_LOCK_SA3 is lock start address 3 configuration register.

Offset Address	Register Name	Total Reset Value
0x40	NFC_LOCK_SA3	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flash_lock_cs				flash_lock_addr3															
Reset	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.
[20:19]	RW	flash_lock_cs	NAND flash lock CS. 00: CS 0 01: CS 1 Other values: reserved
[18:0]	RW	flash_lock_addr3	Lock start address 3. The LSB maps to the fifth row address of the NAND flash.

NFC_LOCK_EA0

NFC_LOCK_EA0 is lock end address 0 configuration register.

Offset Address	Register Name	Total Reset Value
0x44	NFC_LOCK_EA0	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flash_lock_cs				flash_lock_eaddr0															
Reset	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.
[20:19]	RW	flash_lock_cs	NAND flash lock CS. 00: CS 0 01: CS 1 Other values: reserved

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[18:0]	RW	flash_lock_eaddr0	Lock end address 0. The LSB maps to the fifth row address of the NAND flash.

NFC_LOCK_EA1

NFC_LOCK_EA1 is lock end address 1 configuration register.

Offset Address	Register Name	Total Reset Value
0x48	NFC_LOCK_EA1	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flash_lock_cs				flash_lock_eaddr1															
Reset	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.
[20:19]	RW	flash_lock_cs	NAND flash lock CS. 00: CS 0 01: CS 1 Other values: reserved
[18:0]	RW	flash_lock_eaddr1	Lock end address 1. The LSB maps to the fifth row address of the NAND flash.

NFC_LOCK_EA2

NFC_LOCK_EA2 is lock end address 2 configuration register.

Offset Address	Register Name	Total Reset Value
0x4C	NFC_LOCK_EA2	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flash_lock_cs				flash_lock_eaddr2															
Reset	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.

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[20:19]	RW	flash_lock_cs	NAND flash lock CS. 00: CS 0 01: CS 1 Other values: reserved
[18:0]	RW	flash_lock_eaddr2	Lock end address 2. The LSB maps to the fifth row address of the NAND flash.

NFC_LOCK_EA3

NFC_LOCK_EA3 is lock end address 3 configuration register.

Offset Address	Register Name	Total Reset Value
0x50	NFC_LOCK_EA3	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flash_lock_cs	flash_lock_eaddr3																			
Reset	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.
[20:19]	RW	flash_lock_cs	NAND flash lock CS. 00: CS 0 01: CS 1 Other values: reserved
[18:0]	RW	flash_lock_eaddr3	Lock end address 3. The LSB maps to the fifth row address of the NAND flash.

NFC_EXPCMD

NFC_EXPCMD is an extended page command register.

Offset Address	Register Name	Total Reset Value
0x54	NFC_EXPCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ex_pcmd3								ex_pcmd2								ex_pcmd1								ex_pcmd0							

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	ex_pcmd3	Extended page write command 3 of the NAND flash.
[23:16]	RW	ex_pcmd2	Extended page write command 2 of the NAND flash.
[15:8]	RW	ex_pcmd1	Extended page write command 1 of the NAND flash.
[7:0]	RW	ex_pcmd0	Extended page write command 0 of the NAND flash.

NFC_EXBCMD

NFC_EXBCMD is an extended block command register.

Offset Address	Register Name	Total Reset Value
0x58	NFC_EXBCMD	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ex_bcmd1								ex_bcmd0							
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:8]	RW	ex_bcmd1	Extended block write command 1 of the NAND flash.
[7:0]	RW	ex_bcmd0	Extended block write command 0 of the NAND flash.

NFC_ECC_TEST

NFC_ECC_TEST is an ECC test register.

Offset Address	Register Name	Total Reset Value
0x5C	NFC_ECC_TEST	0x0020_F001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													ecc_mask	dec_only	enc_only
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved.

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[2]	RW	ecc_mask	ECC function mask. 0: Whether the ECC check and correction are performed depends on the value of ecc_type. 1: The ECC check and correction are forbidden. The structure of the data read from or written to the NAND flash is still converted based on the format of ecc_type.
[1]	RW	dec_only	Decoding only enable. When 1 is written to this bit, ECC decoding is enabled, but the NAND flash is not read or written. When the bit is read, the value 0 is returned.
[0]	RW	enc_only	Encoding only enable. When 1 is written to this bit, ECC encoding is enabled, but the NAND flash is not read or written. When this bit is read, the return value 1 indicates that ECC encoding and decoding are complete and the value 0 indicates that ECC encoding and decoding are being performed.

NFC_DMA_CTRL

NFC_DMA_CTRL is a DMA control register.

Offset Address	Register Name	Total Reset Value
0x60	NFC_DMA_CTRL	0x0000_0070

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				wr_cmd_disable	rw_nf_disable	dma_nf_cs		dma_addr_num	burst16_en	burst8_en	burst4_en	reserved		dma_wr_en	dma_start
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	1	1	1	0	0	0	0	0	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved.
[11]	RW	wr_cmd_disable	Whether the NANDC initiates a complete timing for reading/writing to the NAND flash. 0: The NANDC initiates a complete timing for reading/writing to the NAND flash. 1: The NANDC initiates a timing for reading/writing to data rather than a command. That is, the NANDC initiates CS signals and read/write pulse signals for reading/writing data rather than the CLE and ALE signals.

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[10]	RW	rw_nf_disable	Whether the DMA operation and the read/write operation are performed at the same time. 0: The DMA operation and the read/write operation on the NAND flash are performed at the same time. 1: Data is transferred between the buffer and the DDR, but the NAND flash is not read or written.
[9:8]	RW	dma_nf_cs	NAND flash CS select for operating the DMA. 00: CS 0 01: CS 1 Other values: reserved
[7]	RW	dma_addr_num	Number of addresses. 0: 5 addresses 1: 4 addresses
[6]	RW	burst16_en	Burst 16 enable. 0: disabled 1: enabled
[5]	RW	burst8_en	Burst 8 enable. 0: disabled 1: enabled
[4]	RW	burst4_en	Burst 4 enable. 0: disabled 1: enabled
[3]	RW	oob_area_en	OOB area write enable. This bit is valid only in 1-bit ECC mode. 0: disabled 1: enabled
[2]	RW	data_area_en	Data area write enable. This bit is valid only in 1-bit ECC mode. 0: disabled 1: enabled
[1]	RW	dma_wr_en	DMA read/write enable. 0: read 1: write
[0]	RW	dma_start	DMA operation enable. When the value 1 is written to this bit, the DMA operations are enabled. The bit retains 1 until the DMA operations are complete. Writing 0 to this bit has no effect. If the value 0 is returned after this bit is read, the DMA operations are complete.

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NFC_BADDR_D

NFC_BADDR_D is a base address register of the data transfer area in DMA mode.

Offset Address	Register Name	Total Reset Value
0x64	NFC_BADDR_D	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	base_addr_d																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	base_addr_d	Base address of the DDR data area that stores the data to be read or written.

NFC_BADDR_OOB

NFC_BADDR_OOB is a base address register of the OOB area in DMA mode.

Offset Address	Register Name	Total Reset Value
0x68	NFC_BADDR_OOB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	base_addr_oob																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	base_addr_oob	Base address of the OOB area that stores the data to be read. This register is valid only when the NAND flash is written in DMA mode.

NFC_DMA_LEN

NFC_DMA_LEN is a transfer length register in DMA mode.

Offset Address	Register Name	Total Reset Value
0x6C	NFC_DMA_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				len_oob												reserved				len_data											

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	reserved	Reserved.
[28:16]	RW	len_oob	Length of the OOB area when the NAND flash is written in DMA mode. The long words must be 4-byte aligned. This field is valid only in ECC0 mode. In other modes, the OOB length is fixed.
[15:12]	RW	reserved	Reserved.
[11:0]	RW	len_data	Length of the data to be read or written in DMA mode. This field is valid only when rw_nf_disable is 1.

NFC_OP_PARA

NF_OP_PARA is an operation parameter register.

Offset Address	Register Name	Total Reset Value
0x70	NFC_OP_PARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ext_len		oob_ecc_en	data_ecc_en	oob_edc_en	data_edc_en	oob_rw_en	data_rw_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:6]	RW	ext_len	Length of the extended data area to be corrected. In 24-bit ECC mode, this field indicates the length of the extended data area in each ECC data block. In boot mode, when the page size is 4 KB, the default length is 8 bytes; when the page size is 8 KB, the default length is 4 bytes. 01: 4 bytes 11: 8 bytes Other values: reserved
[5]	RW	oob_ecc_en	ECC correction enable in OOB area. 0: disabled 1: enabled This field is valid only when data is read.

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[4]	RW	data_ecc_en	ECC correction enable. 0: disabled 1: enabled This field is valid only when data is read.
[3]	RW	oob_edc_en	OOB area check enable. 0: disabled 1: enabled In programming mode, the function of generating the ECC code of the OOB area is enabled. In data read mode, the check on the OOB area is enabled.
[2]	RW	data_edc_en	Check enable. 0: disabled 1: enabled In programming mode, ECC code is generated. In data read mode, the check is enabled.
[1]	RW	oob_rw_en	Read/write redundancy enable for the data area of the NAND flash. 0: disabled 1: enabled
[0]	RW	data_rw_en	Read/write enable for the data area of the NAND flash. 0: disabled 1: enabled

NFC_VERSION

NFC_VERSION is a version register.

Offset Address	Register Name	Total Reset Value
0x74	NFC_VERSION	0x0000_0300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	version_id																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	version_id	Version number.

NFC_BUF_BADDR

NFC_BUF_BADDR is a NANDC buffer base address register.

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Offset Address	Register Name	Total Reset Value
0x78	NFC_BUF_BADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	buf_baddr_rd			reserved	buf_baddr_wr		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	buf_baddr_rd	Indicates the base address from which the buffer is read in DMA mode when rw_nf_disable is 1. Indicates undefined when rw_nf_disable is 0.
[15:12]	RW	reserved	Reserved.
[11:0]	RW	buf_baddr_wr	Indicates the base address from which the buffer is written in DMA mode when rw_nf_disable is 1. Indicates undefined when rw_nf_disable is 0.

NFC_RD_LOGIC_ADDR

NFC_RD_LOGIC_ADDR is a logic address register for reading the NAND flash in DMA mode

Offset Address	Register Name	Total Reset Value
0x007C	NFC_RD_LOGIC_ADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				rd_logic_addr			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	rd_logic_addr	Start address (excluding the ECC code) for reading data. For example, if you want to read data from the bad block flag, you can set the field value to 2048 for the 2 KB page size or 4096 for the 4 KB page size. After data is read in DMA mode, the field value is automatically accumulated based on the value of NFC_DMA_LEN[len_data]. The rd_logic_addr field is valid only when data is read in DMA mode and NFC_DMA_CTRL[rw_nf_disable] is 0.

NFC_RD_LOGIC_LEN

NFC_RD_LOGIC_LEN is a logic length register for reading the NAND flash in DMA mode.

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Offset Address	Register Name	Total Reset Value
0x0080	NFC_RD_LOGIC_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rd_logic_len															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	rd_logic_len	Length (excluding the length of the ECC code) of the data read from the NAND flash in DMA mode. After data is read in DMA mode, the field value is cleared automatically. The rd_logic_addr field is valid only when data is read in DMA mode and NFC_DMA_CTRL[rw_nf_disable] is 0.

NFC_FIFO_EMPTY

NFC_FIFO_EMPTY is an internal FIFO status register.

Offset Address	Register Name	Total Reset Value
0x0090	NFC_FIFO_EMPTY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																empty_dbg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RO	empty_dbg	Empty status of the internal FIFO, for debugging only.

NFC_BOOT_SET

NFC_BOOT_SET is a boot parameter configuration register.

Offset Address	Register Name	Total Reset Value
0x0094	NFC_BOOT_SET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														addr_num	block_size

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	-	rsv	Reserved.
[1]	RW	addr_num	Number of addresses sent to the NAND flash by the NANDC during booting. 0: 4 address cycles 1: 5 address cycles. The reset value depends on the nfc_addr_num pin.
[0]	RW	block_size	Bus width of the NAND flash during booting. 0: 64 pages 1: 128 pages The reset value depends on the nfc_block_size pin.

NF_STATUS

NF_STATUS is a NAND flash status register.

Offset Address	Register Name	Total Reset Value
0x0098	NF_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								status							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	RO	status	Status data read from the NAND flash. This field is valid when NFC_OP is written and NFC_OP[read_status_en] is 1.

4.3 SPI Flash Controller

4.3.1 Overview

The serial peripheral interface flash controller (SFC) provides an advanced high performance bus (AHB) slave interface on the service side. By using the slave interface, the access to the SPI flash through the AHB channel can be controlled.

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4.3.2 Features

4.3.2.1 AHB Interface

The AHB interface has the following features:

- Provides an AHB slave interface. Through this interface, the internal configuration register can be accessed or the SPI flash memory can be accessed directly based on selected signals.
- Supports the AMBA2.0 protocol.
- Supports the little endian mode.

4.3.2.2 Memory Interfaces

The memory interface has the following features:

- Supports two CSs: CS0 and CS1. Each CS supports a maximum of 128 Mbit (in 3-byte address mode) or 8 Gbit (in 4-byte address mode) storage space, and the flash memories with different capacities. In addition, each CS can be mapped to the system address space with configurable base address, and CS1 supports address alias.
- Supports the following types of interfaces: standard SPI, dual-output/dual-input SPI, quad-output/quad-input SPI, dual I/O SPI, quad I/O SPI, full dual I/O SPI, and full quad I/O SPI. After power-on, the standard SPI is supported by default. You can change the interface type by configuring the corresponding register.
- Supports two flash address modes: 3-byte address mode and 4-byte address mode. After power-on, the 3-byte address mode is supported by default. You can change the address mode by configuring the corresponding register.
- Supports read/write operations by means of bus or register programming.
- Supports write protection.

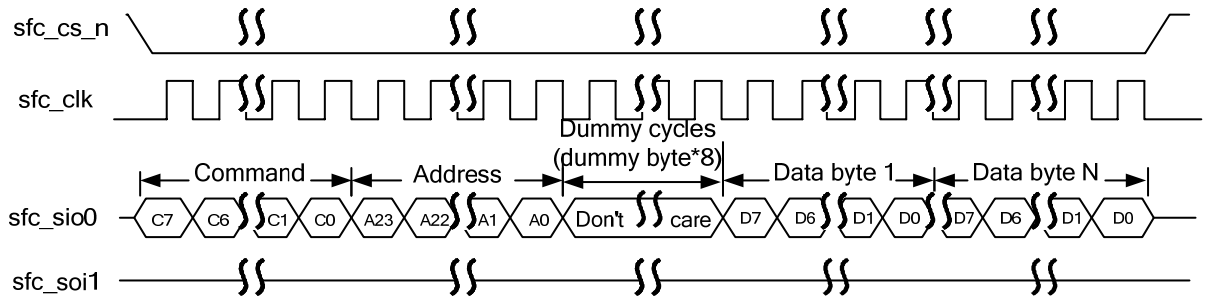
4.3.3 Function Description

4.3.3.1 Interface Timing

Standard SPI

The standard SPI is connected to a 1-bit data input line and a 1-bit data output line. Figure 4-16 and Figure 4-17 show the timings of the standard SPI.

Figure 4-16 Timing of the standard SPI (write)



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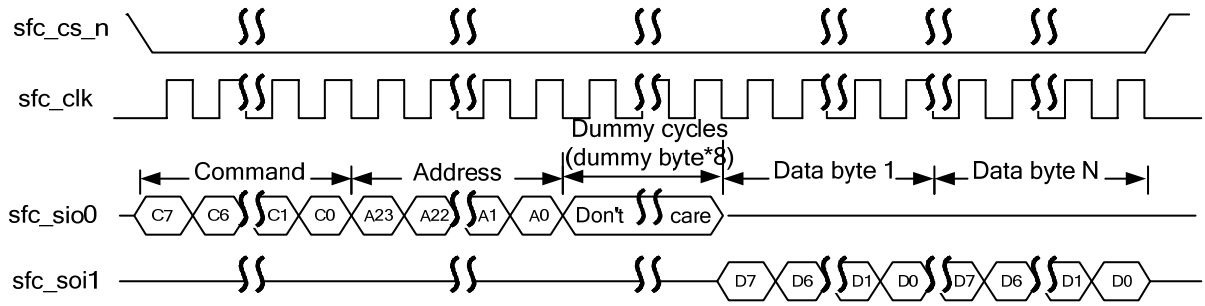
NOTE

The opcode bytes, address bytes, and dummy bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.

The data bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.

Figure 4-17 Timing of the standard SPI (read)



NOTE

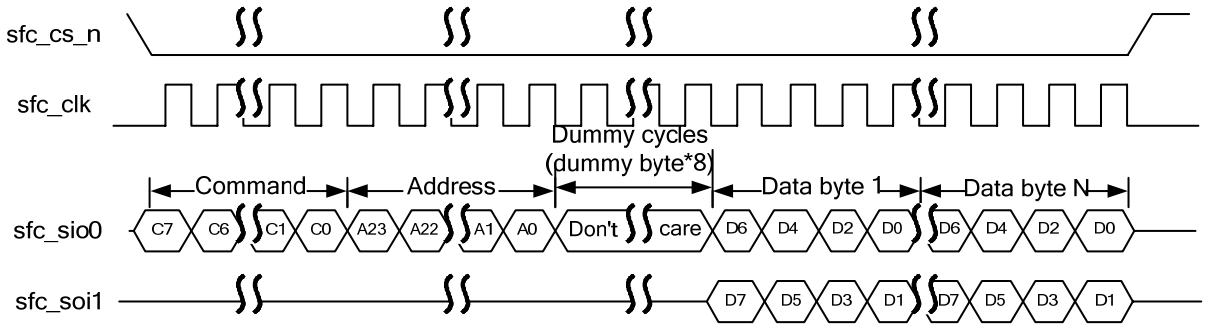
The opcode bytes, address bytes, and dummy bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.

The data bytes are input in unit of a single bit in serial mode through the sfc_sio1 line.

Dual Input/Dual Output SPI

In dual input/output SPI mode, a 2-bit bidirectional data line is used. Figure 4-18 shows the timing in dual input/output SPI mode.

Figure 4-18 Timing of the dual input/output SPI



NOTE

The opcode bytes, address bytes, and dummy bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.

The data bytes are output (write) and input (read) in unit of dual bits in serial mode through the sfc_sio0 or sfc_sio1 line.

Dual I/O SPI

In dual I/O SPI mode, a 2-bit bidirectional data line is used. Figure 4-19 shows the timing in this mode.

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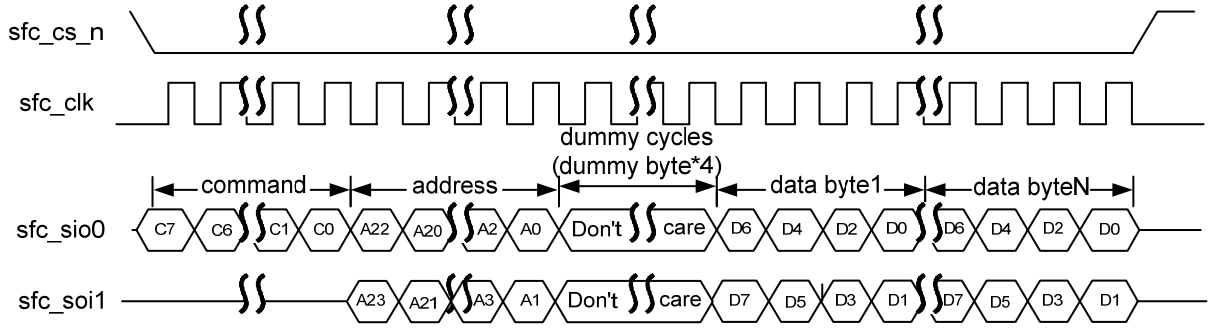
Figure 4-19 Timing in dual I/O SPI mode

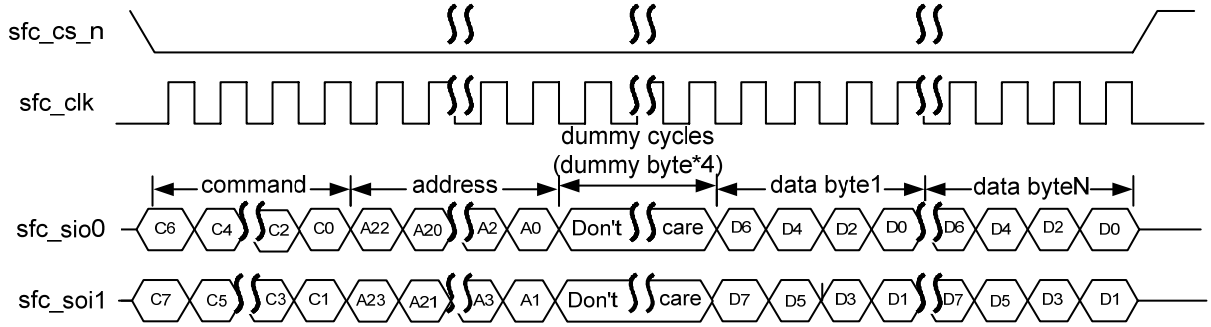


NOTE

The opcode bytes are output in unit of a single bit in serial mode through the sfc_sio0 line. The address bytes and dummy bytes are output in unit of dual bits through the sfc_sio0 or sfc_soi1 line. The data bytes are output (write) and input (read) in unit of dual bits through the sfc_sio0 or sfc_soi1 line.

Full Dual I/O SPI

In full dual I/O SPI mode, a 2-bit bidirectional data line is used. Figure 4-20 shows the timing in this mode.Timing in dual I/O SPI mode



NOTE

The opcode bytes, address bytes, and dummy bytes are output in unit of dual bits through the sfc_sio0 or sfc_soi1 line. The data bytes are output (write) and input (read) in unit of dual bits through the sfc_sio0, sfc_soi1, sfc_wp, or sfc_hold line.

Quad Input/Quad Output SPI

In quad input/output SPI mode, a 4-bit bidirectional data line is used. Figure 4-21 shows the timing in quad input/output SPI mode.

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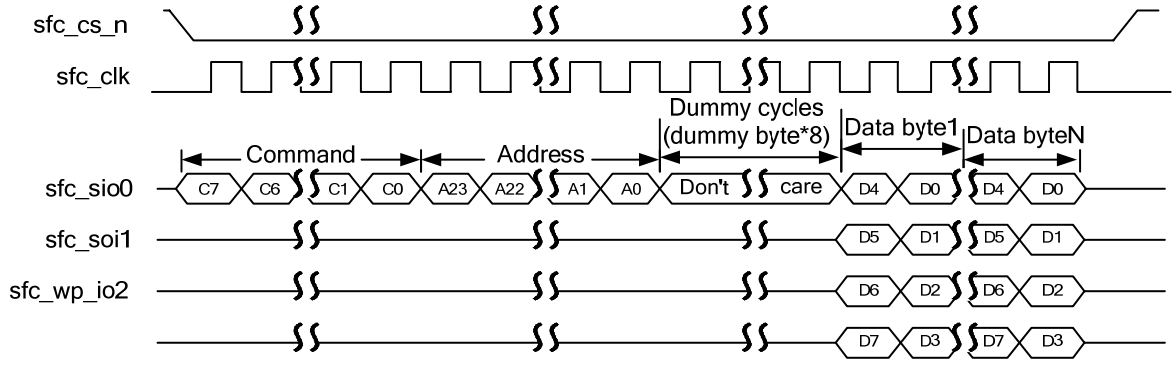
Figure 4-21 Timing of the quad input/output SPI



NOTE

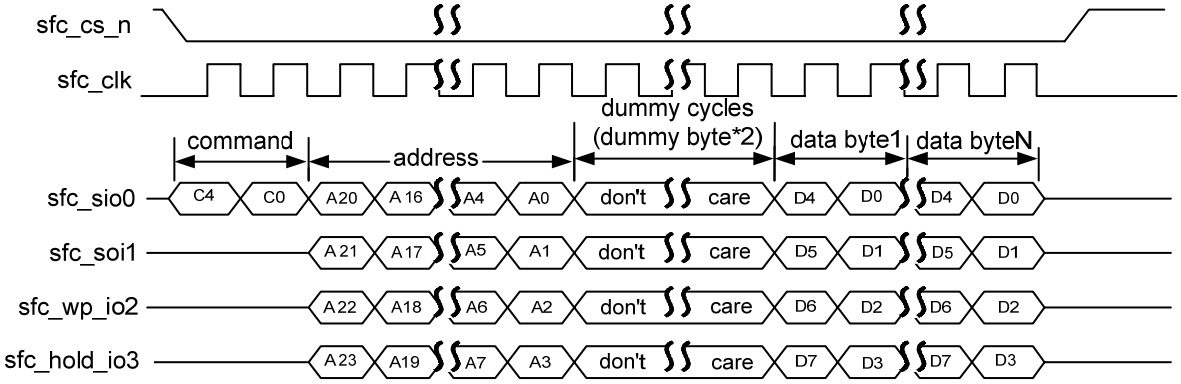
The opcode bytes, address bytes, and dummy bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.

The data bytes are output (write) and input (read) in unit of dual bits in serial mode through the sfc_sio0, sfc_soi1, sfc_wp_io2, or sfc_hold_io3 line.

Quad I/O SPI

In quad I/O SPI mode, a 4-bit bidirectional data line is used. Figure 4-22 shows the timing in this mode.

Figure 4-22 Timing in quad I/O SPI mode



NOTE

The opcode bytes are output in unit of a single bit in serial mode through the sfc_sio0 line. The address bytes and dummy bytes are output in unit of quad bits through the sfc_sio0, sfc_soi1, sfc_wp, or sfc_hold line. The data bytes are output (write) and input (read) in unit of quad bits through the sfc_sio0, sfc_soi1, sfc_wp, or sfc_hold line.

Full Quad I/O SPI

In full quad I/O SPI interface mode, a 4-bit bidirectional data line is used. Figure 4-23 shows the timing in quad-SPI interface mode.

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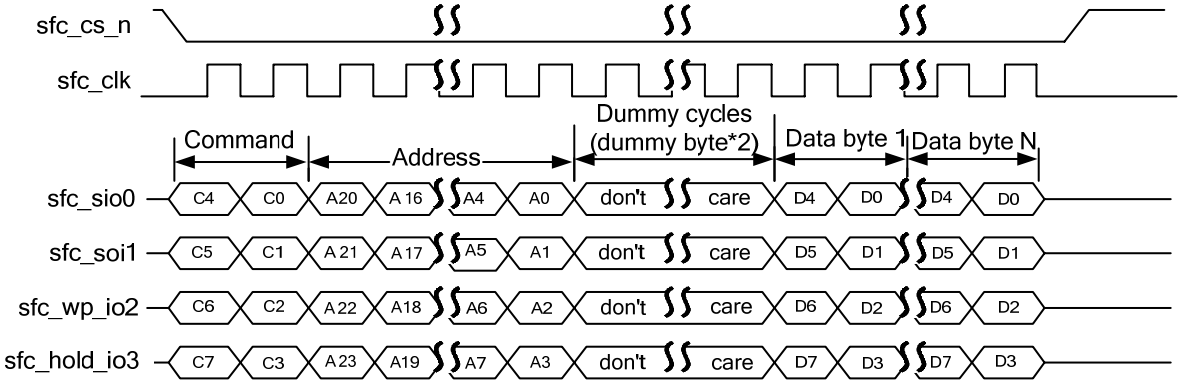
Figure 4-23 Timing of the full quad I/OSPI



NOTE

The opcode bytes, address bytes, and dummy bytes are output in unit of quad bits through the sfc_sio0, sfc_soi1, sfc_wp_io2, or sfc_hold_io3 line.

The data bytes are output (write) and input (read) in unit of dual bits in serial mode through the sfc_sio0, sfc_soi1, sfc_wp_io2, or sfc_hold_io3 line.

4.3.3.2 Reading and Writing the FPI Flash

Reading the SPI Flash

The SPI flash can be read in either of the following two ways:

- Read the flash memory by using the AHB bus. In this case, the flash memory is read in a high-efficient manner. The SFC automatically maps the read timing of the AHB bus as the SPI timing.
- Read the flash memory by configuring the configuration register of the SFC with using software.

  The SFC converts all the memory read operations through the AHB bus into the read operations over the SPI interface. After power-on, the normal read operation (opcode = 0x3) is performed by default. The number of dummy bytes corresponding to this read operation is 0. When the system starts after power-on, the number of opcodes and dummy bytes in a read command can be configured by using software to perform other read operations. For example, iocode is 0xB and the number of dummy bytes is 1 for fast read. For a wrap read operation through the AHB, the SFC divides the operation into two bursts.

Writing the SPI Flash

The SPI flash can be written in either of the following ways:

- Write the flash memory by using the AHB bus. The SFC automatically converts a write operation through the AHB bus into the write enable (WREN) operation, page program (PP) operation, and read status register (RDSR) operation on the flash memory side. When the bus writes in unspecified lengths (INCR), the performance is poor.
- Read the flash memory by setting the configuration register of the SFC using software. This operation mode is recommended when the data amount is large.

  Before writing to a flash memory, software must configure the corresponding SFC register to erase the flash memory.

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A PP operation may take some time, because the flash memory needs to read the status register of the flash memory to check whether the PP operation is complete. The next write operation can be started only after the PP operation is complete. Otherwise, data is lost.

A PP operation cannot span the page boundary. If the write operation spans the page boundary, the operation is split into two. When the flash memory is written by using the AHB bus, the SFC module automatically checks whether the write operation spans the page boundary based on the address and burst length. If the write operation spans the page boundary, the operation is split into two. For a wrap write operation through the AHB bus, the SFC divides the operation into two bursts.

Other Operations

Other operations such as erasing the flash memory, enabling the flash memory to enter the deep power-down mode, and reading the device ID can be implemented by accessing related registers.

4.3.3.3 Switching the Flash Address Mode

The SFC supports 3-byte and 4-bypte flash address modes. The 3-byte flash address mode is used by default. You can switch the address mode dynamically by configuring related registers. The address modes of the flash memories connected to the two CSs must be the same. Otherwise, you must reconfigure the SFC configuration register and command register before using the flash memories.

To switch the flash address mode, perform the following steps:

NOTE

Before switching the flash address mode, ensure that the operations related to flash memories are complete.

Step 1 Transmit the instruction for switching the address mode to flash memories by using the related registers.

Step 2 Configure GLOBAL_CONFIG[flash_addr_mode].

Step 3 Start the operation in the new address mode.

---End

For details about the instruction for switching the address mode of the SPI flash, see the related component manuals.

4.3.3.4 Timing Description

Figure 4-24 and Figure 4-25 show the timings and related parameters.

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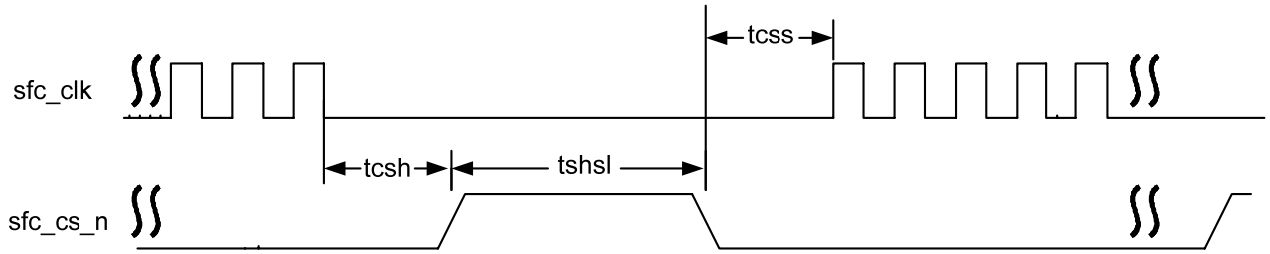
Figure 4-24 SPI output timing



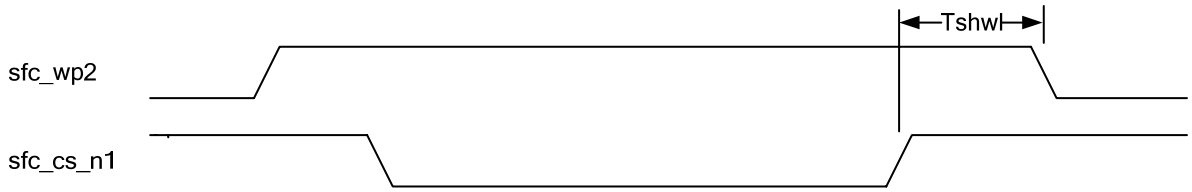
NOTE

Tcsh: CS setup time

Tcss: CS hold time

Tshsl: CS deselect time

Figure 4-25 SPI write protection timing



NOTE

tshwl: write protect hold time.

4.3.4 Working Flowchart

4.3.4.1 Reading the Flash Memory by Configuring Registers

Figure 4-26 shows the process of reading the flash memory by configuring registers in query mode.

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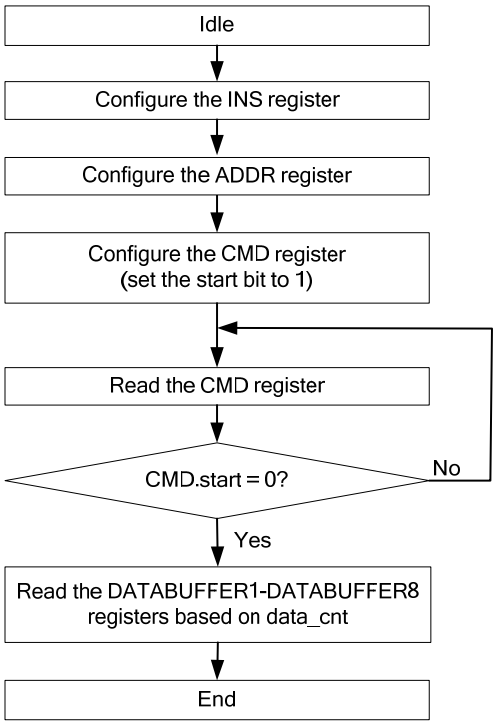
Figure 4-26 Process of reading the flash memory by configuring registers in query mode



4.3.4.2 Writing to the Flash Memory by Configuring registers

Figure 4-27 shows the process of writing to the flash memory by configuring registers in interrupt mode.

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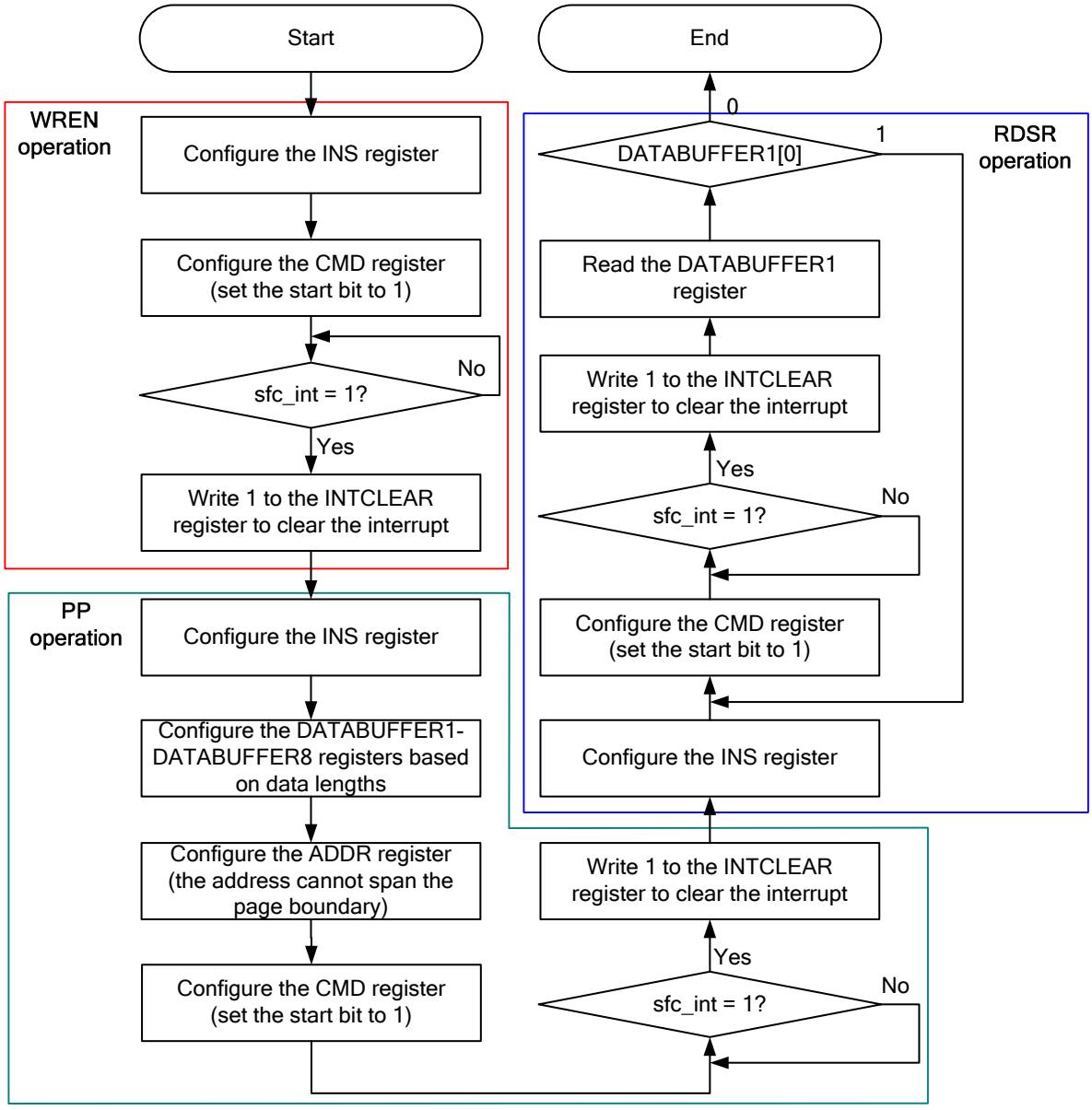
Figure 4-27 Process of writing to the flash memory by configuring registers in interrupt mode



4.3.4.3 Reading and Writing to the Flash Memory by Using the Bus

Figure 4-28 shows the process of reading and writing to the flash memory by using the bus.

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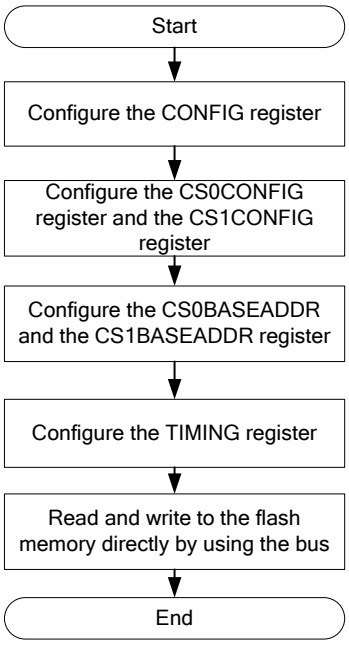
Figure 4-28 Process of reading and writing to the flash memory directly by using the bus



4.3.5 Register Summary

Table 4-16 describes the SFC registers.

Table 4-16 Summary of the SFC registers (base address: 0x1001_0000)

Offset Address	Register	Description	Page
0x0100	GLOBAL_CONFIG	Global configuration register	4-112
0x0110	TIMING	Timing configuration register	4-113
0x0120	INT_RAW_STATUS	Raw interrupt status register	4-114
0x0124	INT_STATUS	Masked interrupt status register	4-115
0x0128	INT_MASK	Interrupt mask register	4-115
0x012C	INT_CLEAR	Interrupt clear register	4-116
0x01F8	VERSION	Version register	4-117
0x01FC	VERSION_SEL	Version selection register	4-117
0x0200	BUS_CONFIG1	Bus operation mode configuration register 1	4-118
0x0204	BUS_CONFIG2	Bus operation mode configuration register 2	4-119
0x0210	BUS_FLASH_SIZE	Mapping size register for the bus operation mode	4-120

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Offset Address	Register	Description	Page
0x0214	BUS_BASE_ADDR_CS0	Bus mapping base address register for CS 0	4-121
0x0218	BUS_BASE_ADDR_CS1	Bus mapping base address register for CS 1	4-121
0x021C	BUS_ALIAS_ADDR_CS1	Bus alias base address register for CS 1	4-121
0x0300	CMD_CONFIG	Command operation mode configuration register	4-122
0x0308	CMD_INS	Instruction register for the command operation mode	4-124
0x030C	CMD_ADDR	Address register for the command operation mode	4-124
0x0400 + 4xN	CMD_DATABUF_N	Data buffer register for the command operation mode	4-125

Table 4-17 describes the mode of accessing the flash memory based on the register configurations.

Table 4-17 Mode of accessing the flash memory based on the register configurations

Register	Field	Available Access Mode	
		Accessing the Flash Memory by Using the Bus	Accessing the Flash Memory By Using Related Registers
CONFIG	wr_ins	Yes	No
	rd_ins	Yes	No
	prefetch_cnt	Yes	No
	rd_delay	Yes	Yes
	flash_addr_mode	Yes	Yes
	wip_locate	Yes	Yes
	dummy_byte	Yes	No
	mem_if_type	Yes	Yes
	Reserved	Yes	Yes
	mode	Yes	Yes
CMD	None	No	Yes

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Register	Field	Available Access Mode	
		Accessing the Flash Memory by Using the Bus	Accessing the Flash Memory By Using Related Registers
INS	None	No	Yes
ADDR	None	No	Yes
DATABUFFER1–8	None	No	Yes
CS0CONFIG	None	Yes	No
CS1CONFIG	None	Yes	No
CS1BASEADDR	None	Yes	No
CS1BASEADDR	None	Yes	No
CS1ALIASADDR	None	Yes	No
TIMING	None	Yes	Yes
INTRAWSTATUS	None	No	Yes
INTSTATUS	None	No	Yes
INTMASK	None	No	Yes
INTCLEAR	None	No	Yes

4.3.6 Register Description

GLOBAL_CONFIG

GLOBAL_CONFIG is the global configuration register.

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Offset Address	Register Name	Total Reset Value
0x0100	GLOBAL_CONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											rd_delay			flash_addr_mode	wp_en	mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:3]	RW	rd_delay	Number of delayed clock cycles for reading data from the SPI flash. 00: no delay (default value) 01: 1 clock cycle 10: 2 clock cycles 11: 3 clock cycles
[2]	RW	flash_addr_mode	SPI address mode. 0: 3-byte address mode (default value) 1: 4-byte address mode The write operation is invalid when CMD.start is 1.
[1]	RW	wp_en	Hardware write protection enable. The WP pin is forcibly pulled down when the bit is set to 1. 0: disabled 1: enabled
[0]	RW	mode	SPI mode configuration. 0: mode 0 1: mode 3

TIMING

TIMNG is the timing configuration register.

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Offset Address	Register Name	Total Reset Value
0x0110	TIMING	0x0000_660F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	tcsh			reserved	tcss			reserved				tshsl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14:12]	RW	tcsh	CS hold time. 000–111: *n* + 1 clock cycles(*n* = 0, 1, 2, …, or 7)
[11]	RW	reserved	Reserved.
[10:8]	RW	tcss	CS setup time. 000–111: *n* + 1 clock cycles(*n* = 0, 1, 2, …, or 7)
[7:4]	RO	reserved	Reserved.
[3:0]	RW	tshsl	CS deselect time. It is equal to the interval between two flash operations. 0000–1111: n + 2 clock cycles(*n* = 0, 1, 2, …, or 15)

INT_RAW_STATUS

INT_RAW_STATUS is the raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0120	INT_RAW_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															cmd_op_end_raw_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.

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[0]	RO	cmd_op_end_raw_status	Raw interrupt status of instruction operation end (not masked). 0: The operation is not complete. 1: The operation is complete.

INT_STATUS

INT_STATUS is the masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0124	INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															cmd_op_end_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	cmd_op_end_status	Interrupt status of instruction operation end (masked). 0: The operation is not complete. 1: The operation is complete.

INT_MASK

INT_MASK is the interrupt mask register.

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Offset Address	Register Name	Total Reset Value
0x0128	INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															cmd_op_end_int_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	cmd_op_end_int_mask	Instruction operation end interrupt mask. 0: masked 1: not masked

INT_CLEAR

INT_CLEAR is the interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x012C	INT_CLEAR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															cmd_op_end_int_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.

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[0]	WO	cmd_op_end_int_clr	Instruction operation completion interrupt clear. Writing 1 to this bit clears cmd_op_end_status and cmd_op_end_raw_status. 0: not cleared 1: cleared After a clear operation is complete, this bit returns 0 automatically.

VERSION

VERSION is the version register.

Offset Address	Register Name	Total Reset Value
0x01F8	VERSION	0x0000_0300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VERSION																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	VERSION	SFC version number.

VERSION_SEL

VERSION_SEL is the version selection register.

Offset Address	Register Name	Total Reset Value
0x01FC	VERSION_SEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															version_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	version_sel	Register group version indicator. 0: earlier version register group 1: new version register group

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BUS_CONFIG1

BUS_CONFIG1 is bus operation mode configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0200	BUS_CONFIG1	0x8080_0300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	wr_enable	wr_ins									wr_dummy_bytes	wr_mem_if_type				rd_ins								rd_prefetch_cnt				rd_dummy_bytes			rd_mem_if_type
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	reserved	Reserved.
[30]	RW	wr_enable	Bus write control. 0: disabled 1: enabled
[29:22]	RW	wr_ins	Write instruction.
[21:19]	RW	wr_dummy_bytes	Dummy bytes of the bus write operation. 0: no dummy byte 1: 1 byte 2: 2 bytes ... 7: 7 bytes
[18:16]	RW	wr_mem_if_type	Type of the connected SPI flash interface for the bus write operation. 000: standard SPI 001: dual I/O SPI 010: dual I/O SPI 011: full dual I/O SPI 100: reserved 101: quad-input/dual-output SPI 110: quad I/O SPI 111: full quad I/O SPI
[15:8]	RW	rd_ins	Read instruction.

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[7:6]	RW	rd_prefetch_cnt	Clock cycle for prefetching data when the flash memory is accessed at a variable data length through the bus. 00: not prefetched (default value) 01: Data is prefetched in 1 clock cycle. 10: Data is prefetched in 2 clock cycles. 11: Data is prefetched in 3 clock cycles.
[5:3]	RW	rd_dummy_bytes	Dummy bytes of the bus read operation. 0: no dummy byte 1: 1 byte 2: 2 bytes ... 7: 7 bytes
[2:0]	RW	rd_mem_if_type	Type of the connected SPI flash interface for the bus read operation. 000: standard SPI 001: dual I/O SPI 010: dual I/O SPI 011: full dual I/O SPI 100: reserved 101: quad-input/dual-output SPI 110: quad I/O SPI 111: full quad I/O SPI

BUS_CONFIG2

BUS_CONFIG2 is the bus configuration register 2.

Offset Address	Register Name	Total Reset Value
0x0204	BUS_CONFIG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														wip_locate	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.

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[2:0]	RW	wip_locate	Position of the write in progress (WIP) bit in the flash status register. 000: The WIP is located at bit 0 of the flash status register. 001: The WIP is located at bit 1 of the flash status register. 010: The WIP is located at bit 2 of the flash status register. 011: The WIP is located at bit 3 of the flash status register. 100: The WIP is located at bit 4 of the flash status register. 101: The WIP is located at bit 5 of the flash status register. 110: The WIP is located at bit 6 of the flash status register. 111: The WIP is located at bit 7 of the flash status register.

BUS_FLASH_SIZE

BUS_FLASH_SIZE is the mapping size register for the bus operation mode.

Offset Address	Register Name	Total Reset Value
0x0210	BUS_FLASH_SIZE	0x0000_0909

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				flash_size_cs1				reserved				flash_size_cs0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:8]	RW	flash_size_cs1	Capacity of the SPI flash connected to CS 1. 0000: No SPI flash is connected. 0001: 512 kbits 0010: 1 Mbit 0011: 2 Mbits 0100: 4 Mbits 0101: 8 Mbits 0110: 16 Mbits 0111: 32 Mbits 1000: 64 Mbits 1001: 128 Mbits (default value) 1010: 256 Mbits 1011: 512 Mbits 1100: 1 Gbit 1101: 2 Gbits 1110: 4 Gbits 1111: 8 Gbits

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[7:4]	RW	reserved	Reserved.
[3:0]	RW	flash_size_cs0	Capacity of the SPI flash connected to CS 0. 0000: No SPI flash is connected. 0001: 512 kbits 0010: 1 Mbit 0011: 2 Mbits 0100: 4 Mbits 0101: 8 Mbits 0110: 16 Mbits 0111: 32 Mbits 1000: 64 Mbits 1001: 128 Mbits (default) 1010: 256 Mbits 1011: 512 Mbits 1100: 1 Gbit 1101: 2 Gbits 1110: 4 Gbits 1111: 8 Gbits

BUS_BASE_ADDR_CS0

BUS_BASE_ADDR_CS0 is a bus mapping base address register for CS 0.

Offset Address	Register Name	Total Reset Value
0x0214	BUS_BASE_ADDR0	0x5A00_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bus_base_addr_high_cs0																reserved															
Reset	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	bus_base_addr_high_cs0	Base address for the system space to which the SPI flash of CS 0 is mapped.
[15:0]	RO	reserved	Reserved.

BUS_BASE_ADDR_CS1

BUS_BASE_ADDR_CS1 is a bus mapping base address register for CS 1.

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Offset Address	Register Name	Total Reset Value
0x0218	BUS_BASE_ADDR	0x5800_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bus_base_addr_high_cs1																reserved																
Reset	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	bus_base_addr_high_cs1	Base address for the system space to which the SPI flash of CS 1 is mapped.
[15:0]	RO	reserved	Reserved.

BUS_ALIAS_ADDR_CS1

BUS_ALIAS_ADDR is the alias mapping base address register for the bus operation mode.

Offset Address	Register Name	Total Reset Value
0x021C	BUS_ALIAS_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flash_alias_addr																reserved																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	flash_alias_addr	The flash memory of CS 1 is mapped to the second base address for the system space.
[15:0]	RO	reserved	Reserved.

CMD_CONFIG

CMD_CONFIG is the command operation mode configuration register.

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Offset Address	Register Name	Total Reset Value
0x0300	CMD_CONFIG	0x0000_7E00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												mem_if_type				data_cnt							rw	data_en	dummy_byte_cnt			addr_en	reserved	sel_cs	start	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:17]	RW	mem_if_type	Type of the connected SPI flash interface in register command operation mode. 000: standard SPI 001: dual I/O SPI 010: dual I/O SPI 011: full dual-I/O SPI 100: reserved 101: quad-input/dual-output SPI 110: quad I/O SPI 111: full quad I/O SPI
[16:9]	RW	data_cnt	The length of the read and written data is (N + 1) bytes.
[8]	RW	rw	Indicates whether data is read or written in the current operation. data_en must be set to 1. 0: write. Data is transmitted. 1: read. Data is returned.
[7]	RW	data_en	Indicates whether data is involved in the current operation. 0: No data is involved. 1: Data is involved.
[6:4]	RW	dummy_byte_cnt	Dummy bytes in register command operation mode. 000: no dummy byte 001: 1 byte 010: 2 bytes ... 111: 7 bytes

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[3]	RW	addr_en	Indicates whether an address is involved in the current operation. 0: No address is involved. 1: An address is involved.
[2]	RO	reserved	Reserved.
[1]	RW	sel_cs	CS select. 0: CS0; 1: CS1.
[0]	RW	start	Instruction operation start indicator. 0: The operation is complete. 1: The operation starts. After the current operation is complete, the bit returns 0 automatically.

CMD_INS

CMD_INS is the instruction register for the command operation mode.

Offset Address	Register Name	Total Reset Value
0x0308	CMD_INS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								REG_INS							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	REG_INS	Instruction code in the mode in which the register accesses the flash memory.

CMD_ADDR

CMD_ADDR is the address register for the command operation mode.

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Offset Address	Register Name	Total Reset Value
0x030C	CMD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cmd_addr																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:0]	RW	cmd_addr	Operation address in the mode in which the register accesses the flash memory.

CMD_DATABUF_N

CMD_DATABUF_N is the buffer register for the command operation mode.

Offset Address	Register Name	Total Reset Value
0x0400 + 4xN (N = 0–63)	CMD_DATABUF_N	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cmd_databuf_n																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cmd_databuf_n	Data buffer *N* in the mode in which the register accesses the flash memory. The register offset address is 0x400 + 4Xn. The variable *N* ranges from 0 to 63.

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Contents

5 TOE 5-1
5.1 Overview 5-1
5.2 Features 5-1
5.2.1 GMAC 5-1
5.2.2 TOE Acceleration 5-1
5.3 Function Description 5-2
5.4 Operating Modes 5-4
5.4.1 Interface Timings 5-4
5.4.2 Bypass Modes 5-7
5.4.3 Operating Modes of the TOE 5-13
5.5 Register Summary 5-22
5.6 Register Description 5-28

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Figures

Figure 5-1 Functional block diagram of the TOE 5-3
Figure 5-2 MDIO read timing 5-4
Figure 5-3 MDIO write timing 5-5
Figure 5-4 RX timing parameters for the MDIO interface 5-5
Figure 5-5 RGMII RX timing 5-6
Figure 5-6 RGMII TX timing 5-6
Figure 5-7 MII RX timing 5-7
Figure 5-8 MII TX timing 5-7
Figure 5-9 Receiving Ethernet packets in bypass mode 5-8
Figure 5-10 RX descriptor in bypass mode 5-8
Figure 5-11 Transmitting Ethernet packets in bypass mode 5-11
Figure 5-12 TX descriptor in bypass mode 5-12
Figure 5-13 State switching of the TCP protocol 5-15
Figure 5-14 Receiving TCP packets in TOE mode 5-16
Figure 5-15 RX descriptor for TCP packets 5-16
Figure 5-16 Transmitting TCP packets in TOE mode 5-21
Figure 5-17 TX descriptor for TCP packets 5-22

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Tables

Table 5-1 Timing parameters for the MDIO interface 5-5
Table 5-2 RGMII timing parameters 5-6
Table 5-3 MII timing parameters 5-7
Table 5-4 Data structure of an RX descriptor in bypass mode 5-8
Table 5-5 Data structure of a TX descriptor in bypass mode 5-12
Table 5-6 Format of a typical TCP packet 5-14
Table 5-7 Data structure of an RX descriptor for TCP packets 5-17
Table 5-8 Data structure of a TX descriptor for TCP packets 5-22
Table 5-9 Variables in the offset addresses of TOE registers 5-23
Table 5-10 Summary of the TOE registers (base address: 0x101C_0000) 5-23

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5 TOE

5.1 Overview

The Transmission Control Protocol offload engine (TOE) can receive data from or transmit data to one Ethernet port at the same time. It can work at 10 Mbit/s, 100 Mbit/s, or 1000 Mbit/s, and supports the half-duplex and full-duplex modes. The TOE provides the media independent interface (MII) and reduced gigabit media independent interface (RGMII).

By using the hardware, the TOE supports TCP/IP acceleration, which increases the throughput of the Ethernet port and reduces the CPU usage.

5.2 Features

5.2.1 GMAC

The TOE provides one GMACs that have the following features:

- Support the full-duplex mode at 10 Mbit/s, 100 Mbit/s, or 1000 Mbit/s.
- Support the half-duplex mode at 10 Mbit/s or 100 Mbit/s.
- Support the MII and RGMII.
- Support 802.3x traffic control in full-duplex mode.
- Support carrier sense multiple access (CSMA) and collision detection (CD) in half-duplex mode.
- Check the frame length and discard the packets without required lengths.
- Automatically add start frame delimiters (SFDs) to the transmitted frames and delete SFDs from received frames.
- Provide a management data input/output (MDIO) interface.
- Count the frames that are received and transmitted over ports.
- Control whether to receive broadcast frames, multicast frames, and unicast frames.
- Support filtering by configurable MAC address.
- Support 802.3-2005.

5.2.2 TOE Acceleration

The TOE core supports TCP/IP acceleration. The details are as follows:

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- TCP acceleration is supported for a maximum of 254 connections. The maximum connections can be configured. The connections beyond the upper limit are processed by the standard TCP/IP protocol stack.
- Hardware acceleration complying with various protocols such as the TCP and IP is supported. The packets complying with other layer-3 and layer-4 protocols are processed by the standard TCP/IP protocol stack.
- All Internet Protocol version 6 (IPv6) packets are processed by the standard TCP/IP protocol stack.
- All virtual local area network (VLAN) packets are processed by the standard TCP/IP protocol stack.
- Various bypass modes are supported. In bypass mode, the TOE processes only layer-2 packets (that is, only the GMAC function is implemented), and the standard TCP/IP protocol stack processes layer-3 and layer-4 packets.
- During TCP acceleration, the hardware supported the following functions:
  - Connection management. The hardware processes all data transfers after connections are set up.
  - Slow start.
  - Configurable maximum segment size (MSS).
  - Congestion control algorithm.
  - TCP check and IP header check and calculation in receive (RX) and transmit (TX) directions.
  - Traffic control in the sliding window.
  - Out-of-order packets detection and drop.
  - Hardware timers including the retransmission timer and persist timer. The keep-alive timer and 2MSL timer are implemented in the software protocol stack.
  - Window scale option.
  - Round trip time (RTT) measurement and calculation.
  - TCP timeout retransmission and fast retransmission.
- Two driven modes are supported for determining whether to accelerate the current TCP connection.
  - Threshold-based: If the traffic of a connection exceeds the threshold, the connection is accelerated until it is removed.
  - First come, first served: Only the first 254 connections are accelerated. A new connection is accelerated only after one of the first 254 connections is removed.
- The counter for TCP-accelerated connections in TX and RX directions is supported.

5.3 Function Description

Figure 5-1 shows the functional block diagram of the TOE.

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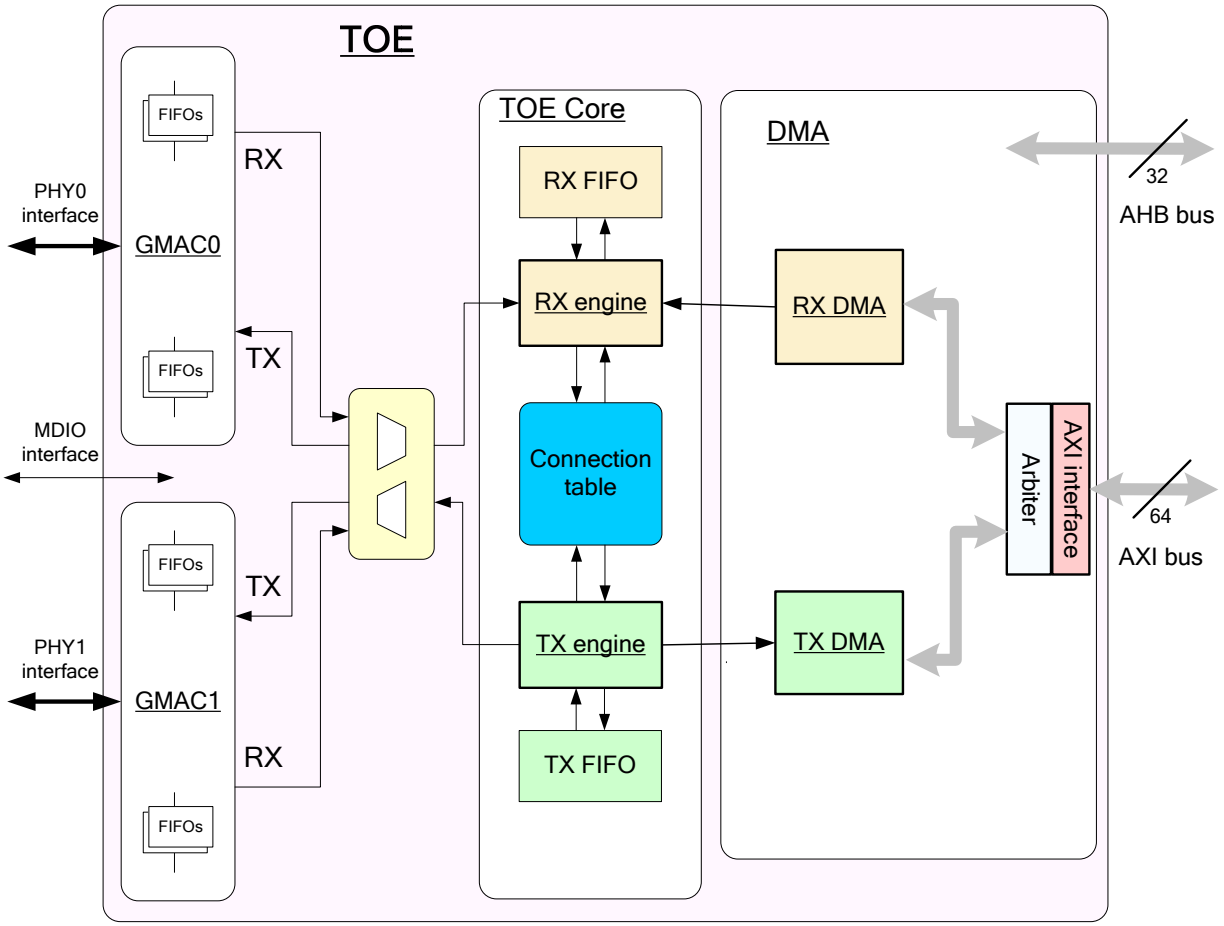
Figure 5-1 Functional block diagram of the TOE



The TOE provides the GMAC, TOE core, and DMA module. They have the following features:

- The TOE provides one PHY interface that supports the RGMII and MII modes, rates of 10/100/1000 Mbps, and half-duplex and full-duplex modes. The TOE also provides an MDIO interface for configuring the two PHYs.
- The TOE has one GMAC. The GMAC process the layer-2 packets and buffers the received data and data to be transmitted in internal FIFOs.
- The TOE core implements TCP/IP acceleration.
  - The connection table in the TOE core maintains the information about a maximum of 254 TCP-accelerated connections.
  - By using the state machine, the TOE core manages and controls the received data and transmitted data.
  - In the RX direction, the TOE core performs the following operations:

    Buffers received data in the RX FIFO.

    Parses packets.

    Performs checksum calculations on packets.

    Obtains details about the connection corresponding to a packet from the connection table by using the lookup function.

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Counts the received packets.

– In the TX direction, the TOE core performs the following operations:

Buffers the data to be transmitted in the TX buffer.

Controls the data to be transmitted by using the TX engine.

Performs checksum calculations on packets.

Periodically manages data.

- The DMU module has multiple DMA units that are used to receive and transmit common Ethernet packets and some TCP packets.
- The TOE also provides a 64-bit AXI master interface and a 32-bit AHB slave interface.

5.4 Operating Modes

5.4.1 Interface Timings

This section describes MDIO, RGMII, and MII timings. For details about TOE interface signals, see section 2.2 "Pin Descriptions" in chapter 2 "Hardware."

5.4.1.1 MDIO Timings

The MDIO interface controls the read and write access to the PHY chip. The software writes data, the address for the PHY chip, the register addresses, and related control information to the GMACn_GMII_DATA register. If GMACn_GMII_DATA [GB] is 0, the hardware has finished reading or writing to the PHY chip. The hardware converts addresses, data, and control information into MDIO timings. During a read operation, the read data is stored in GMACn_GMII_DATA. After querying that GMACn_GMII_DATA [GB] is 0, the CPU reads data from GMACn_GMII_DATA.

The Hi3521 can automatically obtain the working status of the PHY chip over the MDIO interface. If the TOE is set to adaptation mode, you must configure the address for the PHY chip status register by configuring GMACn_GMII_DATA. The TOE automatically reads status information from the related register of a specified PHY chip over the MDIO interface, and then stores the information in GMACn_GMII_DATA. For details about the addresses for status registers, see the related PHY manuals.

Figure 5-2 shows the MDIO read timing.

Figure 5-2 MDIO read timing

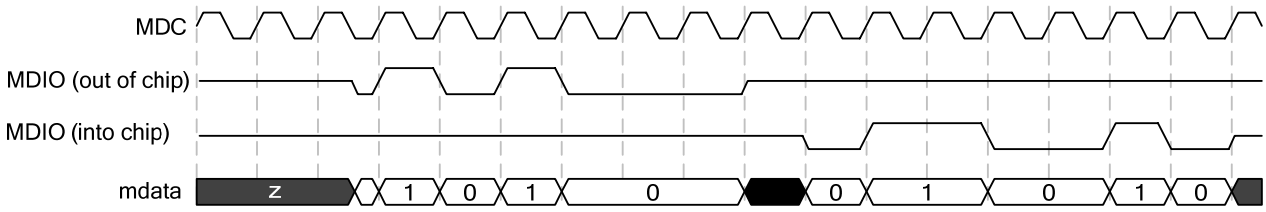

Figure 5-3 shows the MDIO write timing.

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Figure 5-3 MDIO write timing

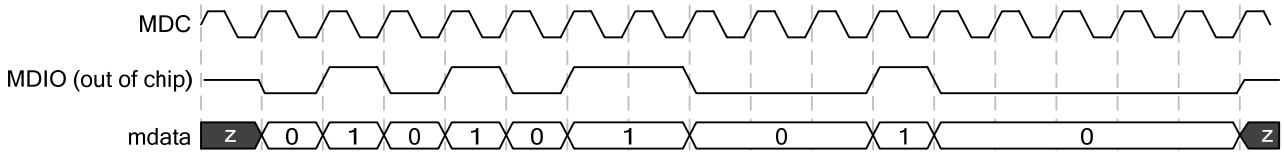

Figure 5-4 shows the RX timing parameters for the MDIO interface.

Figure 5-4 RX timing parameters for the MDIO interface

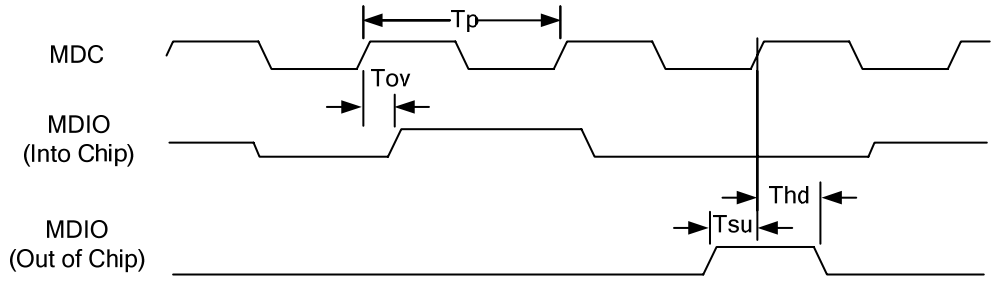

Table 5-1 describes the timing parameters for the MDIO interface.

Table 5-1 Timing parameters for the MDIO interface

Parameter	Symbol	Signal	Min	Max	Unit
MDIO data receive delay	Tov	MDIO	0	300	ns
MDIO clock cycle	Tp	MDC	400	1240	ns
MDIO data transmit setup time	Tsu	MDIO	10	None	ns
MDIO data transmit hold time	Thd	MDIO	10	None	ns

NOTE

The MDC clock cycle Tp can be changed by adjusting the MDC frequency (MDIO_RWCTRL[frq_dv]). To be specific, you can divide the TOE working clock by 102, 62, or other values. Tov is related to Tp, and its value is about Tmdc/2.

5.4.1.2 RGMII Timings

Figure 5-5 shows the RGMII RX timing.

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Figure 5-5 RGMII RX timing

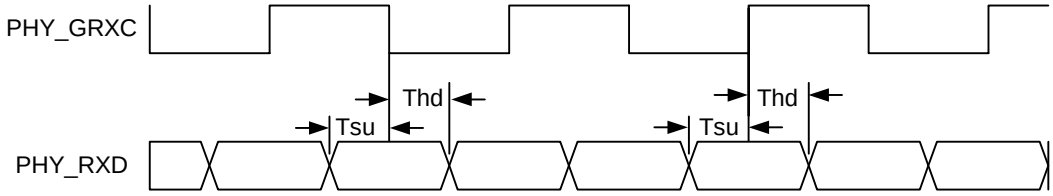

Figure 5-6 shows the RGMII TX timing.

Figure 5-6 RGMII TX timing

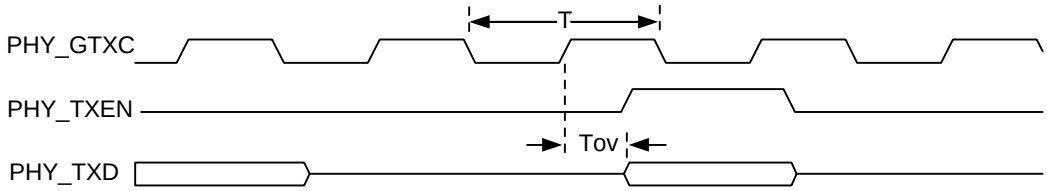

Table 5-2 describes RGMII timing parameters.

Table 5-2 RGMII timing parameters

Parameter	Symbol	Signal	Min	Max	Unit
RGMII clock cycle	T	PHY_GRXC PHY_GTXC	8	8	ns
RGMII signal setup time	Tsu (RX)	PHY_RXER, PHY_RXDV, PHY_RXD[3:0]	1	None	ns
RGMII signal hold time	Thd (RX)	PHY_RXER, PHY_RXDV, PHY_RXD[3:0]	1	None	ns
RGMII output signal delay	Tov (TX)	PHY_TXD[3:0], PHY_TXEN	-0.5	0.5	ns

5.4.1.3 MII Timing

The Hi3521 provides a standard MII that complies with the MII timing standard. The MII is used to connect the Hi3521 to the PHY chip.

Figure 5-7 shows the MII RX timing.

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Figure 5-7 MII RX timing

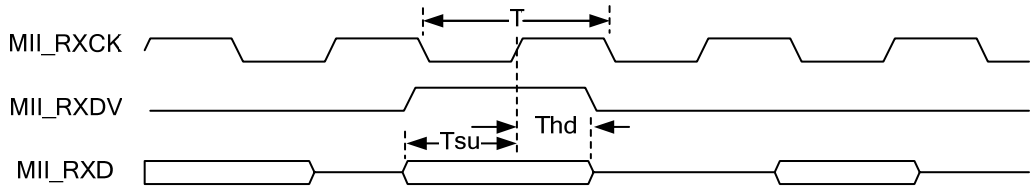

Figure 5-8 shows the MII TX timing.

Figure 5-8 MII TX timing

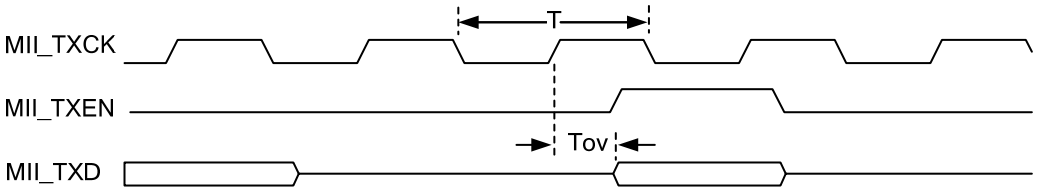

Table 5-3 describes MII timing parameters.

Table 5-3 MII timing parameters

Parameter	Symbol	Signal	Min	Max	Unit
MII clock cycle	T	ETH_RXCK, ETH_TXCK	400(10Mbit/s)	400	ns
			40(100Mbit/s)	40	ns
MII signal setup time	Tsu (RX)	ETH_RXER, ETH_RXDV, ETH_RXD[3:0]	10	None	ns
MII signal hold time	Thd (RX)	ETH_RXER, ETH_RXDV, ETH_RXD[3:0]	10	None	ns
MII output signal delay	Tov (TX)	ETH_TXD[3:0], ETH_TXEN	0	25	ns

5.4.2 Bypass Modes

In bypass mode, the TOE processes only layer-2 packets. That is, only the GMAC function is implemented in bypass mode. The bypass mode can be set only after the bypass driver is loaded. The following describes the processes for receiving and transmitting packets in bypass mode.

5.4.2.1 Receiving Packets in Bypass Mode

Figure 5-9 shows the process for receiving Ethernet packets in bypass mode.

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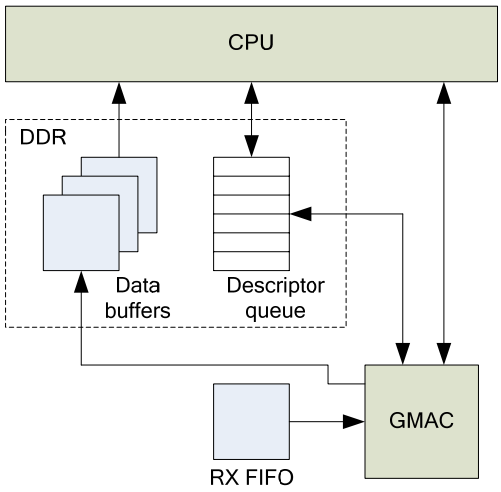
Figure 5-9 Receiving Ethernet packets in bypass mode



The CPU configures the RX descriptor queue to ensure that the GMAC has available RX descriptors, and configures registers to start an RX process. The GMAC reads available RX descriptors based on register configurations, reads Ethernet packets from the RX FIFO that are received on the PHY side, and processes these packets. If the Ethernet packets meet requirements, the GMAC writes the packets to the data buffers specified by RX descriptors, and writes RX descriptors back. Then the GMAC reports an interrupt to instruct the CPU to start reception. At last, the CPU reads the RX descriptors written back by the GMAC, and fetches Ethernet packets from the data buffers. This is a process for receiving packets.

An RX descriptor consists of four words in bypass mode. As shown in Figure 5-10, each word has 32 bits, and an RX descriptor has 128 bits in total.

Figure 5-10 RX descriptor in bypass mode

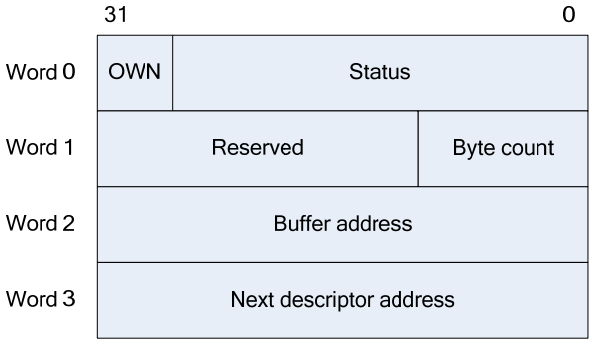


Table 5-4 describes the data structure of an RX descriptor.

Table 5-4 Data structure of an RX descriptor in bypass mode

Bit	Name	Description
[127:96]	next_desc_addr	Address for the next descriptor.
[95:64]	buff_addr	Start address for the buffer.

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Bit	Name	Description
[63]	DIC	Whether to generate an RX interrupt after reception is complete. 0: yes 1: no
[62:58]	reserved	Reserved.
[57]	RER	Whether the current descriptor is the last one in ring mode. 0: no 1: yes
[56:45]	reserved	Reserved.
[44:32]	byte_count	Byte count. It specifies the size of the RX buffer.
[31]	own	OWN bit. It specifies the object that operates the current descriptor. 0: CPU 1: GMAC
[30]	AFM	Result of filtering the destination address for the current packet. 0: failure 1: success
[29:16]	FL	Length of the packet being received, in the unit of byte.
[15]	ES	Error summary. It indicates the logical OR of bit 0, bit 1, bit 3, bit 4, bit 6, bit 7, bit 11, and bit 14. Bit 15 is valid only when bit 8 is set to 1. 0: The currently received packet has no error. 1: The currently received packet has an error.
[14]	DE	Descriptor error. 0: The current descriptor buffer is sufficient to store the packet. 1: The current descriptor buffer is insufficient to store the packet, and the packet is truncated. This bit is valid only when bit 8 is set to 1.
[13]	SAF	Result of filtering the source address for the current packet. 0: failure 1: success
[12]	LE	Whether the length field matches the actual packet length. This bit is valid only when bit 5 is set to 0, and this bit is invalid when a cyclic redundancy check (CRC) error occurs. 0: match 1: mismatch

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Bit	Name	Description
[11]	OE	Buffer overflow indicator in the MTL. 0: The buffer is normal when packets are being received. 1: The received packets are destroyed due to buffer overflow.
[10]	VLAN	VLAN indicator. 0: The current packet is not a VLAN packet. 1: The current packet is a VLAN packet.
[9]	FS	Reserved.
[8]	LS	Reserved.
[7]	GF	Oversized packet indicator. 0: The current packet is not an oversized packet (greater than 1518 bytes). 1: The current packet is an oversized packet.
[6]	LC	Late collision. 0: No late collision is transmitted in half-duplex mode. 1: A late collision is transmitted in half-duplex mode.
[5]	FT	Packet type. 0: IEEE 802.3 packet 1: Ethernet packet
[4]	RWT	Watchdog timeout indicator when packets are being received. 0: The watchdog is normal when packets are being received. 1: The watchdog times out when packets are being received, and packets are truncated.
[3]	RE	RX error. 0: If gmii_rxdv_i is valid when packets are being received, gmii_rxer_i is fixed at 0. 1: If gmii_rxdv_i is valid when packets are being received, gmii_rxer_i is 1.
[2]	DE	Dribble bit error. This bit is valid only in MII mode. 0: The current packet length is an integral multiple of a byte. 1: The current packet length is not an integral multiple of a byte.
[1]	CE	CRC error. This bit is valid only when bit 8 is set. 0: No CRC error occurs on the received packets. 1: A CRC error occurs on the received packets.

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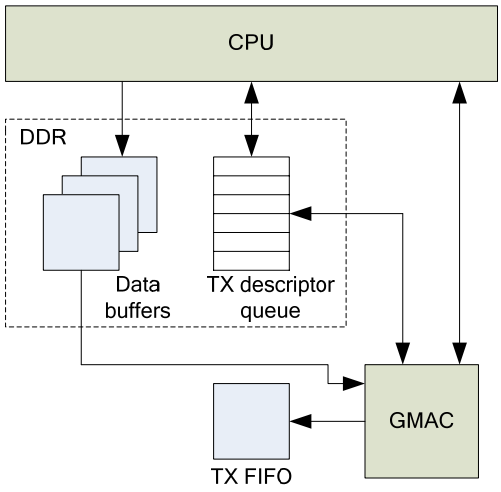
Bit	Name	Description
[0]	Rx MAC Address	RX MAC address indicator. 0: The RX MAC address for the current packet matches the values for RxMAC registers 1–15. 1: The RX MAC address for the current packet matches the value for RxMAC register 0.

5.4.2.2 Transmitting Packets in Bypass Mode

Figure 5-11 shows the process for transmitting Ethernet packets in bypass mode.

Figure 5-11 Transmitting Ethernet packets in bypass mode



When there is data to be transmitted, the CPU configures the TX descriptor queue, and configures registers to start a GMAC TX process. The GMAC obtains available TX descriptors based on register configurations, and reads Ethernet packets to be transmitted from the data buffers specified by TX descriptors. After processing the packets, the GMAC writes the packets in the TX FIFO. Then the GMAC writes back the TX descriptors corresponding to the Ethernet packets, and reports an interrupt to notify the CPU that packets are transmitted. At last, the CPU recycles the TX descriptors written back by the GMAC from the TX descriptor queue for transmitting subsequent data.

A TX descriptor consists of four words in bypass mode. As shown in Figure 5-12, each word has 32 bits, and a TX descriptor has 128 bits in total.

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Figure 5-12 TX descriptor in bypass mode

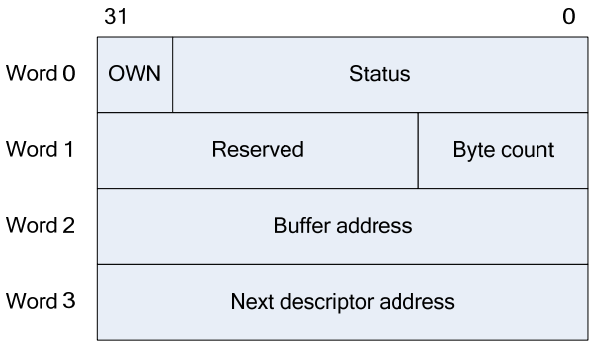

Table 5-5 describes the data structure of a TX descriptor in bypass mode.

Table 5-5 Data structure of a TX descriptor in bypass mode

Bit	Name	Description
[127:96]	next_desc_addr	Address for the next descriptor.
[95:64]	buff_addr	Buffer address.
[63:45]	reserved	Reserved.
[44:32]	byte_count	Byte count. It specified the length of a packet to be transmitted.
[31]	own	OWN bit. It specifies the object that operates the current descriptor. 0: CPU 1: GMAC
[30]	intr	TX completion interrupt enable. 0: disabled 1: enabled
[29:22]	reserved	Reserved.
[21]	TER	Whether the current descriptor is the last one in ring mode. 0: no 1: yes
[20:16]	reserved	Reserved.
[15]	ES	Error summary. It indicates the logical OR of bit 1, bit 8, bit 9, bit 10, and bit 11. 0: The currently transmitted packet has no error. 1: The currently transmitted packet has an error.
[14:12]	reserved	Reserved.

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Bit	Name	Description
[11]	LC	Carrier lost. This bit is valid only in half-duplex mode. 0: The carrier signal is normal when data is being transmitted. 1: The carrier signal is pulled down unexpectedly when data is being transmitted.
[10]	NC	No carrier. This bit is valid only in half-duplex mode. 0: Carrier signals from the PHY are received when data is being transmitted. 1: No carrier signals from the PHY are received when data is being transmitted.
[9]	LC	Late collision. 0: No late collision is transmitted in half-duplex mode. 1: A late collision is transmitted in half-duplex mode.
[8]	EC	Whether collisions exceed the allowed upper limit. 0: No collisions occur when data is transmitted for 16 consecutive times. 1: Collisions occur when data is transmitted for 16 consecutive times, which results in transmission failures.
[7]	VLAN	VLAN indicator. 0: The current packet is not a VLAN packet. 1: The current packet is a VLAN packet.
[6:3]	CC	Collision count. It specifies the collision times before packets are transmitted successfully.
[2]	reserved	Reserved.
[1]	UF	Underflow error. 0: The data from the host memory is received, and the GMAC starts to transmit data. 1: The data from the host memory is delayed, and the GMAC cancels data transmission.
[0]	DB	Delay bit. This bit is valid only in half-duplex mode. 0: No carriers are detected in the data before the GMAC transmits data, and data can be transmitted. 1: Carriers are detected in the data before the GMAC transmits data, and data transmission is delayed.

5.4.3 Operating Modes of the TOE

The processing method and descriptor data structure of non-TCP packets in TOE operating mode are the same as those in bypass mode. The following describes how the TOE processes TCP packets.

The TOE operating mode can be set only after the TOE driver is loaded.

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Formats of the Packets Processed by the TOE

The TCP is a reliable stream transmission protocol. Its retransmission acknowledgment mechanism ensures the transmission reliability, and its sliding window ensures the transmission efficiency. A point-to-point TCP connection has the source IP address, source TCP port number, destination IP address, and destination TCP port number. Table 5-6 describes the format of a typical TCP packet that is encapsulated by using the IPv4 protocol.

Table 5-6 Format of a typical TCP packet

Byte 0		Byte 1	Byte 2	Byte 3
Version	Header Length	Type of Service (TOS)	Total Length	
Identification			Flags	Fragment Offset
Time to Live (TTL)		Protocol (0x06-TCP)	Header Checksum	
Source Address				
Destination Address				
Source Port			Destination Port	
Sequence Number				
Acknowledge Number				
Header Length	Reserved	Control Bits	Window	
Checksum			Urgent Pointer	
Data				
...				

The TOE implementation complies with the IETF RFC standard. Figure 5-13 shows the state switching of the TCP protocol.

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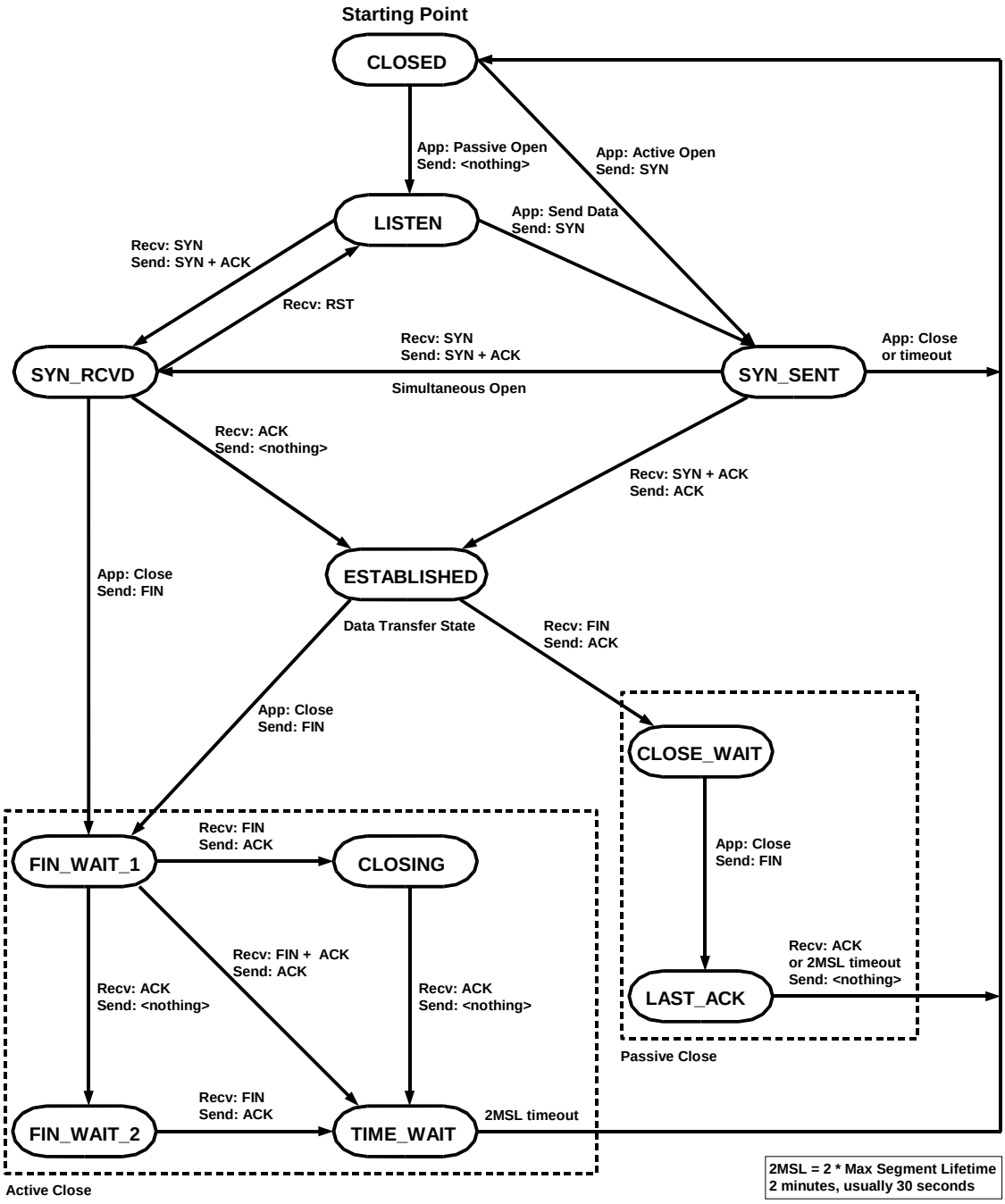
Figure 5-13 State switching of the TCP protocol



The following describes the processes for transmitting and receiving TCP packets in TOE mode.

Receiving TCP Packets in TOE Mode

Figure 5-14 describes the process for receiving TCP packets.

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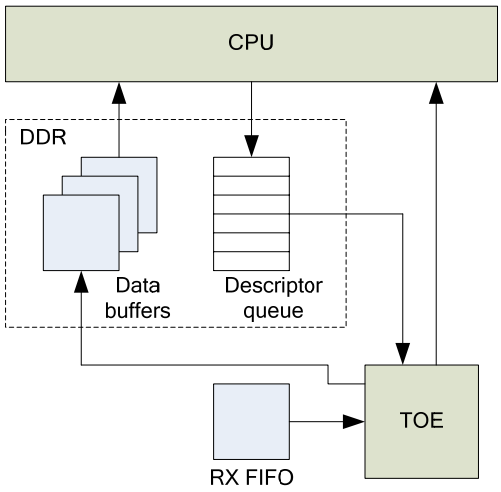
Figure 5-14 Receiving TCP packets in TOE mode



The CPU configures the RX descriptor queue to ensure that the TOE has available RX descriptors, and configures registers to start an RX process. The TOE reads available RX descriptors based on register configurations, reads packets from the RX FIFO that are received on the PHY side, and processes these packets. If the packets meet requirements, the TOE removes the TCP headers and IP headers of the packets, writes valid payloads to the data buffers specified by RX descriptors, and writes RX descriptors back. Then the TOE reports an interrupt to instruct the CPU to start reception. At last, the CPU reads the RX descriptors written back by the TOE, and fetches valid TCP payloads from the data buffers. This is a process for receiving packets.

An RX descriptor for TCP packets consists of eight words in TOE mode. As shown in Figure 5-15, each word has 32 bits, and an RX descriptor for TCP packets has 256 bits in total. Words 0–3 of an RX descriptor for TCP packets in TOE mode are the same as those of a GMAC RX descriptor in bypass mode.

Figure 5-15 RX descriptor for TCP packets

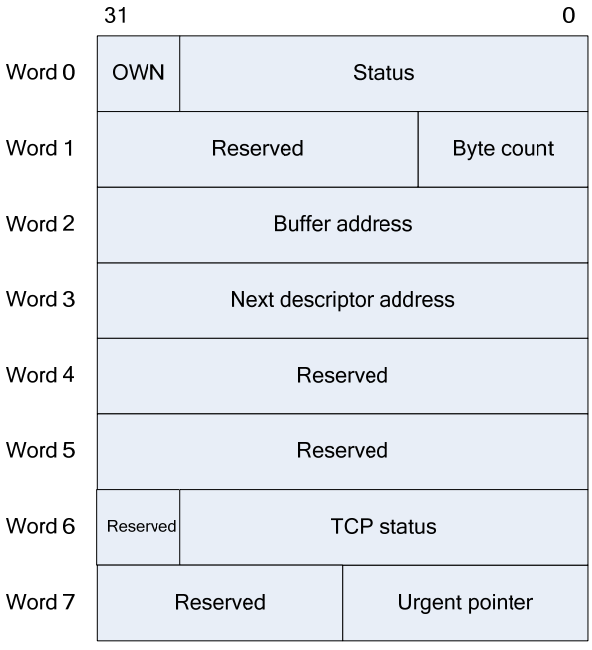


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Table 5-7 describes the data structure of an RX descriptor for TCP packets.

Table 5-7 Data structure of an RX descriptor for TCP packets

Bit	Name	Description
[255:240]	Reserved	Reserved.
[239:224]	urg_ptr	Urgent pointer.
[223:222]	Reserved	Reserved.
[221]	FIN	Whether the finish (FIN) tag bit is configured in a TCP packet. 0: no 1: yes
[220]	SYN	Whether the synchronization (SYN) tag bit is configured in a TCP packet. 0: no 1: yes
[219]	RST	Whether the reset (RST) tag bit is configured in a TCP packet. 0: no 1: yes
[218]	PSH	Whether the push (PSH) tag bit is configured in a TCP packet. 0: no 1: yes
[217]	ACK	Whether the acknowledgment (ACK) tag bit is configured in a TCP packet. 0: no 1: yes
[216]	URG	Whether the urgent (URG) tag bit is configured in a TCP packet. 0: no 1: yes
[215]	toe_err	Incorrect TCP packet. The received data is not acknowledged by the TOE core, and must be dropped. 0: correct TCP packet 1: incorrect TCP packet
[214]	full_pkt_sent	Whether an entire packet is transmitted. 0: no 1: yes
[213]	Reserved	Reserved.

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Bit	Name	Description
[212]	pkt_dropped	Packet indicator. 0: The RX FIFO is normal when packets are being received. 1: An overflow occurs in the RX FIFO, and packets are dropped.
[211]	out_of_order	Out-of-order indicator for the received sequence number. 0: The received TCP sequence number is normal. 1: The received TCP sequence number is out of order.
[210]	connection_err	Connection error. 0: correct 1: error
[209]	dst_ip_mismatch	Whether the destination IP address is matched. 0: match 1: mismatch
[208]	non_tcp	Whether the current packet is a TCP packet. 0: yes 1: no
[207]	ip_hdr_chk_err	IP header checksum error. 0: correct 1: error
[206]	tcp_chk_err	TCP checksum error. 0: correct 1: error
[205]	dst_mac_mismatch	Whether the destination MAC address is matched or the TOE works in bypass mode. 0: The TOE works in TOE mode, and the destination MAC address is matched. 1: The destination MAC address is mismatched or the TOE works in bypass mode.
[204]	not_ip	Whether the current packet is an IP packet. 0: yes 1: no
[203]	premature_eop	Whether packet reception is aborted unexpectedly. 0: no 1: yes
[202:192]	cid	Current TCP connection ID. It specifies the TCP connection to which the current packet belongs.
[191:128]	Reserved	Reserved.

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Bit	Name	Description
[127:96]	next_desc_addr	Address for the next descriptor.
[95:64]	buff_addr	Buffer address.
[63]	DIC	RX completion interrupt enable. 0: enabled 1: disabled
[62:58]	reserved	Reserved.
[57]	RER	Whether the current descriptor is the last one in ring mode. 0: no 1: yes
[56:45]	reserved	Reserved.
[44:32]	byte_count	Byte count. It specifies the size of the RX buffer.
[31]	own	OWN bit. It specifies the object that operates the current descriptor. 0: CPU 1: TOE
[30]	AFM	Result of filtering the destination address for the current packet. 0: failure 1: success
[29:16]	FL	Length of the currently received packet.
[15]	ES	Error summary. It indicates the logical OR of bit 0, bit 1, bit 3, bit 4, bit 6, bit 7, bit 11, and bit 14. Bit 15 is valid only when bit 8 is set to 1. 0: The currently received packet has no error. 1: The currently received packet has an error.
[14]	DE	Descriptor error. This bit is valid only when bit 8 is set to 1. 0: The current descriptor buffer is sufficient to store the packet. 1: The current descriptor buffer is insufficient to store the packet, and the packet is truncated.
[13]	SAF	Result of filtering the source address for the current packet. 0: failure 1: success

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Bit	Name	Description
[12]	LE	Whether the length field matches the packet length. This bit is valid only when bit 5 is set to 0, and this bit is invalid when a CRC error occurs. 0: match 1: mismatch
[11]	OE	Buffer overflow indicator in the MTL. 0: The buffer is normal when packets are being received. 1: The received packets are destroyed due to buffer overflow.
[10]	VLAN	VLAN indicator. 0: The current packet is not a VLAN packet. 1: The current packet is a VLAN packet.
[9]	FS	Reserved.
[8]	LS	Reserved.
[7]	GF	Oversized packet indicator. 0: The current packet is not an oversized packet (greater than 1518 bytes). 1: The current packet is an oversized packet.
[6]	LC	Late collision. 0: No late collision is transmitted in half-duplex mode. 1: A late collision is transmitted in half-duplex mode.
[5]	FT	Packet type. 0: IEEE 802.3 packet 1: Ethernet packet
[4]	RWT	Watchdog timeout indicator when packets are being received. 0: The watchdog is normal when packets are being received. 1: The watchdog times out when packets are being received, and packets are truncated.
[3]	RE	RX error. 0: If gmii_rxdv_i is valid when packets are being received, gmii_rxer_i is fixed at 0. 1: If gmii_rxdv_i is valid when packets are being received, gmii_rxer_i is 1.
[2]	DE	Dribble bit error. This bit is valid only in MII mode. 0: The current packet length is an integral multiple of a byte. 1: The current packet length is not an integral multiple of a byte.

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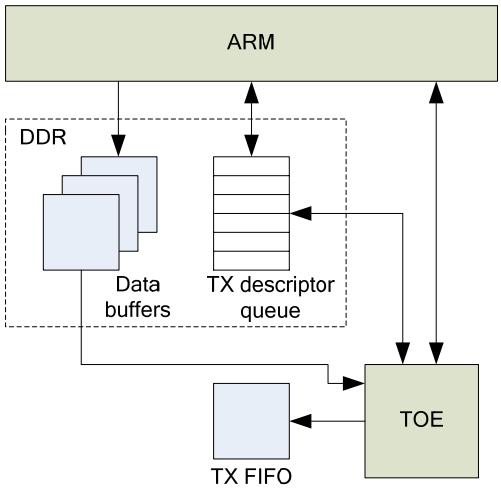
Bit	Name	Description
[1]	CE	CRC error. This bit is valid only when bit 8 is set. 0: No CRC error occurs on the received packets. 1: A CRC error occurs on the received packets.
[0]	Rx MAC address	RX MAC address indicator. 0: The RX MAC address for the current packet matches the value for RxMAC registers 1–15. 1: The RX MAC address for the current packet matches the value for RxMAC register 0.

Transmitting TCP Packets in TOE Mode

Figure 5-16 shows the process for transmitting TCP packets in TOE mode.

Figure 5-16 Transmitting TCP packets in TOE mode



When an upper-layer application needs to transmit data, the CPU configures the TX descriptor queue, and configures registers to start a TOE TX process. The TOE obtains available TX descriptors based on GAMC and DMA configurations, and determines whether to start a TX operation based on status of the connection to which the current TCP payload belongs. When TCP packets need to be transmitted, the TOE reads valid payloads to be transmitted from the data buffers specified by TX descriptors, encapsulates the payloads as TCP packets, and writes the packets in the TX FIFO. Then the TOE waits for a TX command. If the acknowledgment information about all TCP payloads in the current descriptor is received, the TOE writes TX descriptors back, and reports an interrupt to notify the CPU that the data specified by descriptors is transmitted. At last, the CPU recycles the TX descriptors written back by the TOE from the TX descriptor queue for transmitting subsequent data.

A TX descriptor for TCP packets consists of four words in TOE mode. As shown in Figure 5-17, each word has 32 bits, and a TX descriptor has 128 bits in total.

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Figure 5-17 TX descriptor for TCP packets

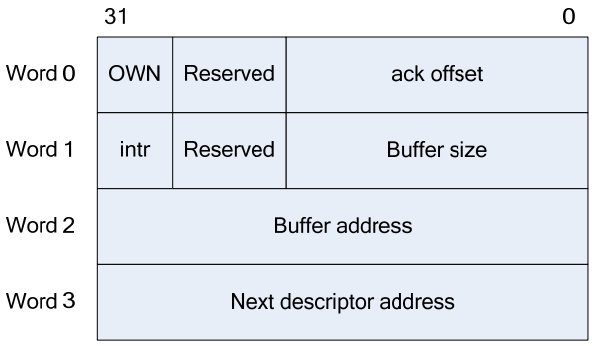

Table 5-8 describes the data structure of a TX descriptor for TCP packets.

Table 5-8 Data structure of a TX descriptor for TCP packets

Bit	Name	Description
[127:96]	next_desc_addr	Address for the next descriptor.
[95:64]	buff_addr	Buffer address.
[63]	intr	Whether the current descriptor generates an interrupt. 0: no 1: yes
[62:56]	reserved	Reserved.
[55:32]	byte_count	Byte count. It specifies the size of the TCP payloads to be transmitted.
[31]	own	OWN bit. It specifies the object that operates the current descriptor. 0: CPU 1: TOE
[30:24]	reserved	Reserved.
[23:0]	ack_offset	Count of TCP payloads in the current descriptor that are acknowledged by the peer end. The count is in the unit of byte. The software sets the value to 0 during initialization, and the TOE can dynamically change the value during transmission.

5.5 Register Summary

Table 5-9 describes the value ranges and meanings of the variables in the offset addresses of TOE registers.

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Table 5-9 Variables in the offset addresses of TOE registers

Variable	Value Range	Description
n	0	MAC ID
p	0, 2	DMA channel ID
x	1–15	MAC address ID1
y	16–31	MAC address ID2

Table 5-10 lists the TOE registers.

Table 5-10 Summary of the TOE registers (base address: 0x101C_0000)

Offset Address	Name	Description	Page
0x0000	GMACn_CTRL_REG	The MAC Configuration register establishes receive and transmit operating modes.	5-28
0x0004	GMACn_FRAME_FILTER	The MAC Frame Filter register contains the filter controls for receiving frames.	5-31
0x0010	GMACn_GMII_ADDR	The GMII Address register controls the management cycles to the external PHY through the management interface.	5-34
0x0014	GMACn_GMII_DATA	The GMII Data register stores Write data to be written to the PHY register located at the address specified in Register 4.	5-36
0x0040	GMACn_ADDR0_HIGH	The MAC address 0 High register holds the upper 16 bits of the 6-byte first MAC address of the station.	5-36
0x0044	GMACn_ADDR0_LOW	The MAC address 0 low register holds the lower 32 bits of the 6-byte first MAC address of the station.	5-37
0x0040+ x x 0x8	GMACn_ADDRx_HIGH	The MAC address x high register contains the higher 16 bits of the MAC address x(1–15).	5-37
0x0044+ x x 0x8	GMACn_ADDRx_LOW	The MAC address x low register holds the lower 32 bits of the 6-byte MAC address x(1–15) of the station.	5-38
0x0780+ y x 0x8	GMACn_ADDRy_HIGH	The MAC address y high register contains the higher 16 bits of the MAC address y(16–31).	5-39
0x078 + y x 0x8	GMACn_ADDRy_LOW	The MAC address y low register holds the lower 32 bits of the 6-byte MAC address y(16–31) of the station.	5-40

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Offset Address	Name	Description	Page
0x0100	GMACn_MMC_CTRL	The MMC control register establishes the operating mode of the management counters.	5-40
0x0114	GMACn_MMC_txoctetcount_gb	The register for number of bytes transmitted,	5-42
0x0118	GMACn_MMC_txframecount_gb	The register for number of good and bad frames transmitted,	5-42
0x011C	GMACn_MMC_txbroadcastframes_g	The register for number of good broadcast frames transmitted.	5-42
0x0120	GMACn_MMC_txmulticastframes_g	The register for number of good multicast frames transmitted..	5-43
0x0124	GMACn_MMC_tx64octets_gb	The register for number of good and bad frames transmitted with length 64 bytes,	5-43
0x0128	GMACn_MMC_tx65to127octets_gb	The register for number of good and bad frames transmitted with length between 65 and 127 (inclusive) bytes, exclusive of preamble and retried frames.	5-44
0x012C	GMACn_MMC_tx128to255octets_gb	The register for number of good and bad frames transmitted with length between 128 and 255 (inclusive) bytes, exclusive of preamble and retried frames.	5-44
0x0130	GMACn_MMC_tx256to511octets_gb	The register for number of good and bad frames transmitted with length between 256 and 511 (inclusive) bytes, exclusive of preamble and retried frames.	5-44
0x0134	GMACn_MMC_tx512to1023octets_gb	The register for number of good and bad frames transmitted with length between 512 and 1,023 (inclusive) bytes, exclusive of preamble and retried frames.	5-45
0x0138	GMACn_MMC_tx1024tomaxoctets_gb	The register for number of good and bad frames transmitted with length between 1,024 and maxsize (inclusive) bytes, exclusive of preamble and retried frames.	5-45
0x013C	GMACn_MMC_txunicastframes_gb	The register for number of good and bad unicast frames transmitted.	5-46
0x0140	GMACn_MMC_txmulticastframes_gb	The register for number of good and bad multicast frames transmitted.	5-46
0x0144	GMACn_MMC_txbroadcastframes_gb	The register for number of good and bad broadcast frames transmitted.	5-47

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Offset Address	Name	Description	Page
0x0148	GMACn_MMC_txunderflowerror	The register for number of frames aborted because of frame underflow error.	5-47
0x014C	GMACn_MMC_txsinglecol_g	The register for number of successfully transmitted frames after a single collision in Half-duplex mode.	5-47
0x0150	GMACn_MMC_txmulticol_g	The register for number of successfully transmitted frames after more than a single collision in Half-duplex mode.	5-48
0x0154	GMACn_MMC_txdeferred	The register for number of successfully transmitted frames after a deferral in Halfduplex mode.	5-48
0x0158	GMACn_MMC_txlatecol	The register for number of frames aborted because of late collision error.	5-48
0x015C	GMACn_MMC_txexesscol	The register for number of frames aborted because of excessive (16) collision errors.	5-49
0x0160	GMACn_MMC_txcarriererror	The register for number of frames aborted because of carrier sense error (no carrier or loss of carrier).	5-49
0x0164	GMACn_MMC_txoctetcount_g	The register for number of bytes transmitted, exclusive of preamble, in good frames only.	5-50
0x0168	GMACn_MMC_txframecount_g	The register for number of good frames transmitted.	5-50
0x016C	GMACn_MMC_txexcessdef	The register for number of frames aborted because of excessive deferral error (deferred for more than two max-sized frame times).	5-50
0x0170	GMACn_MMC_txpauseframes	The register for number of good PAUSE frames transmitted.	5-51
0x0174	GMACn_MMC_txvlanframes_g	The register for number of good VLAN frames transmitted, exclusive of retried frames.	5-51
0x0180	GMACn_MMC_rxframecount_gb	The register for number of good and bad frames received.	5-51
0x0184	GMACn_MMC_rxoctetcount_gb	The register for number of bytes received, exclusive of preamble, in good and bad frames.	5-52
0x0188	GMACn_MMC_rxoctetcount_g	The register for number of bytes received, exclusive of preamble, only in good frames.	5-52

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Offset Address	Name	Description	Page
0x018C	GMACn_MMC_rxbroadcastframes_g	The register for number of good broadcast frames received.	5-52
0x0190	GMACn_MMC_rxmulticastframes_g	The register for number of good multicast frames received.	5-53
0x0194	GMACn_MMC_rxcrcerror	The register for number of frames received with CRC error.	5-53
0x0198	GMACn_MMC_rxalignmenterror	The register for number of frames received with alignment (dribble) error. Valid only in 10/100 mode.	5-54
0x019C	GMACn_MMC_rxrunterror	The register for number of frames received with runt (<64 bytes and CRC error) error.	5-54
0x01A0	GMACn_MMC_rxjabbererror	The register for number of giant frames received with length (including CRC) greater than 1,518 bytes (1,522 bytes for VLAN tagged) and with CRC error.	5-54
0x01A4	GMACn_MMC_rxundersize_g	The register for number of frames received with length less than 64 bytes, without any errors.	5-55
0x01A8	GMACn_MMC_rxoversize_g	The register for number of frames received with length greater than the maxsize (1,518 or 1,522 for VLAN tagged frames), without errors.	5-55
0x01AC	GMACn_MMC_rx64octets_gb	Number of good and bad frames received with length 64 bytes, exclusive of preamble.	5-56
0x01B0	GMACn_MMC_rx65to127octets_gb	The register for number of good and bad frames received with length between 65 and 127 (inclusive) bytes, exclusive of preamble.	5-56
0x01B4	GMACn_MMC_rx128to255octets_gb	The register for number of good and bad frames received with length between 128 and 255 (inclusive) bytes, exclusive of preamble.	5-56
0x01B8	GMACn_MMC_rx256to511octets_gb	The register for number of good and bad frames received with length between 256 and 511 (inclusive) bytes, exclusive of preamble.	5-57
0x01BC	GMACn_MMC_rx512to1023octets_gb	The register for rx512to1023octets_gb number of good and bad frames received with length between 512 and 1,023 (inclusive) bytes, exclusive of preamble.	5-57

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Offset Address	Name	Description	Page
0x01C0	GMACn_MMC_rx1024tomaxoctets_gb	The register for number of good and bad frames received with length between 1,024 and maxsize (inclusive) bytes, exclusive of preamble and retried frames.	5-58
0x01C4	GMACn_MMC_rxunicastframes_g	The register for number of good unicast frames received.	5-58
0x01C8	GMACn_MMC_rxlengtherror	The register for number of frames received with length error (Length type field ≠ frame size), for all frames with valid length field.	5-58
0x01CC	GMACn_MMC_rxoutofrangetype	The register for number of frames received with length field not equal to the valid frame size (greater than 1,500 but less than 1,536).	5-59
0x01D0	GMACn_MMC_rxpauseframes	The register for number of good and valid PAUSE frames received.	5-59
0x01D4	GMACn_MMC_rxfifooverflow	The register for number of missed received frames because of FIFO overflow.	5-60
0x01D8	GMACn_MMC_rxvlanframes_gb	The register for number of good and bad VLAN frames received.	5-60
0x01DC	GMACn_MMC_rxwatchdogerror	The register for number of frames received with error because of watchdog timeout error (frames with a data load larger than 2,048 bytes).	5-60
0x1000 + p x 0x100	DMAp_BUS_MODE	The bus mode register establishes the bus operating modes for the DMA.	5-61
0x1004 + p x 0x100	DMAp_XMT_POLL_DEMAND	The transmit poll demand register enables the Transmit DMA to check whether or not the current descriptor is owned by DMA.	5-64
0x1008 + p x 0x100	DMAp_RCV_POLL_DEMAND	The receive poll demand register enables the receive DMA to check for new descriptors.	5-64
0x100C + p x 0x100	DMAp_RCV_BASE_ADDR	The receive descriptor list address register points to the start of the Receive Descriptor List.	5-65
0x1010 + p x 0x100	DMAp_TX_BASE_ADDR	The transmit descriptor list address register points to the start of the Transmit Descriptor List.	5-65
0x1014 + p x 0x100	DMAp_STATUS	The status register contains all the status bits that the DMA reports to the host.	5-65

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Offset Address	Name	Description	Page
0x1018 + p x 0x100	DMAp_CONTROL	The operation mode register establishes the Transmit and Receive operating modes and commands.	5-69
0x101C + p x 0x100	DMAp_INTR_ENA	The interrupt enable register enables the interrupts reported by DMAp_STATUS.	5-74
0x1020 + p x 0x100	DMAp_MISSED_FRAME_CTR	The register reports the current value of two counters to track the number of missed frames during reception.	5-77
0x1050 + p x 0x100	DMAp_CUR_TX_BUF_ADDR	The current host yransmit buffer address register points to the current Transmit Buffer Address being read by the DMA.	5-77
0x1054 + p x 0x100	DMAp_CUR_RX_BUF_ADDR	The current host receive buffer address register points to the current Receive Buffer address being read by the DMA.	5-78
0x8100	CT_LOCAL_MACADDR0_U16	Local Mac address register for port 0, upper 16 bits.	5-78
0x8104	CT_LOCAL_MACADDR0_L32	Local Mac address registerfor port 0, lower 32 bits.	5-79
0x8108	CT_LOCAL_IPADDR0	Local IP address register for port 0.	5-79
0x814C	TOE_CTRL	The register for TOE number of Retries Allowed and ms Timer Reset Value.	5-79
0x9000	TNK_INTR_STAT	Interrupt status register.	5-80
0x09004	TNK_INTR_EN	Interrupt enables register.	5-81
0x09008	TNK_RESET_STAT	MAC reset status register.	5-81
0x0900C	TNK_ID	The register for number of connections supported and HW release ID	5-82

5.6 Register Description

GMACn_CTRL_REG

The MAC Configuration register establishes receive and transmit operating modes.

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Offset Address	Register Name	Total Reset Value
0x0000	GMACn_CTRL_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ps	fes	do	lm	dm	reserved	dr	reserved	acs	bl		dc	te	re	reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RW	ps	PS: Port Select Selects between GMII and MII: 0: GMII (1000 Mbps) 1: MII (10/100 Mbps) This bit is read-only with the appropriate value in the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, and R_W in the default 10/100/1000 Mbps configuration.
[14]	RW	fes	FES: Speed Indicates the speed in Fast Ethernet (MII) mode: 0: 10 Mbps 1: 100 Mbps This bit is reserved (RO) by default and is enabled only when RGMII is enabled during configuration. This bit generates link speed encoding when TC (Bit 24) is set in RGMII mode. If the core is configured with an RGMII PHY interface, this signal can optionally be driven as an output signal (mac_speed_o[0]).
[13]	RW	do	DO: Disable Receive Own When this bit is set, the GMAC disables the reception of frames when the gmii_txen_o is asserted in Half-Duplex mode. When this bit is reset, the GMAC receives all packets that are given by the PHY while transmitting. This bit is not applicable if the GMAC is operating in Full-Duplex mode. This bit is reserved (RO with default value) if the GMAC is configured for Full-Duplex- only operation during configuration.
[12]	RW	lm	LM: Loopback Mode When this bit is set, the GMAC operates in loopback mode at GMII/MII. The (G)MII Receive clock input (clk_rx_i) is required for the loopback to work properly, as the Transmit clock is not looped-back internally.

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[11]	RW	dm	DM: Duplex Mode When this bit is set, the GMAC operates in a Full-Duplex mode where it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in Full-Duplex-only configuration.
[10]	RW	reserved	Reserved
[9]	RW	dr	DR: Disable Retry When this bit is set, the GMAC attempts only 1 transmission. When a collision occurs on the GMII/MII, the GMAC ignores the current frame transmission and report a Frame Abort with excessive collision error in the transmit frame status. When this bit is reset, the GMAC attempts retries based on the settings of BL (bit [6:5]). This bit is applicable only to Half-Duplex mode and is reserved (RO with default value) in Full-Duplex-only configuration.
[8]	RW	reserved	Reserved
[7]	RW	acs	ACS: Automatic Pad/CRC Stripping When this bit is set, the GMAC strips the Pad/FCS field on incoming frames only if the length's field value is less than or equal to 1,500 bytes. All received frames with length field greater than or equal to 1,501 bytes are passed to the application without stripping the Pad/FCS field. When this bit is reset, the GMAC passes all incoming frames to the Host unmodified.
[6:5]	RW	bl	BL: Back-Off Limit The Back-Off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000 Mbps and 512 bit times for 10/100 Mbps) the GMAC waits before rescheduling a transmission attempt during retries after a collision. This bit is applicable only to Half-Duplex mode and is reserved (RO) in Full-Duplex-only configuration. 00 k = min (n, 10) 01 k = min (n, 8) 10 k = min (n, 4) 11 k = min (n, 1) where n = retransmission attempt. The random integer r takes the value in the range $0 \leq r < 2^k$

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[4]	RW	dc	DC: Deferral Check When this bit is set, the deferral check function is enabled in the GMAC. The GMAC issues a Frame Abort status, along with the excessive deferral error bit set in the transmit frame status when the transmit state machine is deferred for more than 24,288 bit times in 10/100-Mbps mode. If the Core is configured for 1000 Mbps operation, or if the Jumbo frame mode is enabled in 10/100-Mbps mode, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but is prevented because of an active CRS (carrier sense) signal on the GMII/MII. Defer time is not cumulative. If the transmitter defers for 10,000 bit times, then transmits, collides, backs off, and then has to defer again after completion of back-off, the deferral timer resets to 0 and restarts. When this bit is reset, the deferral check function is disabled and the GMAC defers until the CRS signal goes inactive. This bit is applicable only in Half-Duplex mode and is reserved (RO) in Full-Duplex-only configuration.
[3]	RW	te	TE: Transmitter Enable When this bit is set, the transmit state machine of the GMAC is enabled for transmission on the GMII/MII. When this bit is reset, the GMAC transmit state machine is disabled after the completion of the transmission of the current frame, and does not transmit any further frames.
[2]	RW	re	RE: Receiver Enable When this bit is set, the receiver state machine of the GMAC is enabled for receiving frames from the GMII/MII. When this bit is reset, the GMAC receive state machine is disabled after the completion of the reception of the current frame, and does not receive any further frames from the GMII/MII.
[1:0]	RO	reserved	Reserved

GMACn_FRAME_FILTER

The MAC Frame Filter register contains the filter controls for receiving frames.

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Offset Address	Register Name	Total Reset Value
0x0004	GMACn_FRAME_FILTER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ra	reserved																				hpf	saf	saif	pcf		dbf	pm	daif	hmc	huc	pr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	ra	RA: Receive All When this bit is set, the GMAC Receiver module passes to the Application all frames received irrespective of whether they pass the address filter. The result of the SA/DA filtering is updated (pass or fail) in the corresponding bits in the Receive Status Word. When this bit is reset, the Receiver module passes to the Application only those frames that pass the SA/DA address filter.
[30:11]	RO	reserved	Reserved
[10]	RW	hpf	HPF: Hash or Perfect Filter When set, this bit configures the address filter to pass a frame if it matches either the perfect filtering or the hash filtering as set by HMC or HUC bits. When low and if the HUC/HMC bit is set, the frame is passed only if it matches the Hash filter. This bit is reserved (and RO) if the Hash filter is not selected during core configuration.
[9]	RW	saf	SAF: Source Address Filter Enable The GMAC core compares the SA field of the received frames with the values programmed in the enabled SA registers. If the comparison matches, then the SAMatch bit of RxStatus Word is set high. When this bit is set high and the SA filter fails, the GMAC drops the frame. When this bit is reset, then the GMAC Core forwards the received frame to the application and with the updated SA Match bit of the RxStatus depending on the SA address comparison.
[8]	RW	saif	SAIF: SA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the SA address comparison. The frames whose SA matches the SA registers are marked as failing the SA Address filter. When this bit is reset, frames whose SA does not match the SA registers are marked as failing the SA Address filter.

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[7:6]	RW	pcf	PCF: Pass Control Frames These bits control the forwarding of all control frames (including unicast and multicast PAUSE frames). Note that the processing of PAUSE control frames depends only on RFE of Flow Control Register[2]. depends only on RFE of Flow Control Register[2]. 00: GMAC filters all control frames from reaching the application. 01: GMAC forwards all control frames except PAUSE control frames to application even if they fail the Address filter. 10: GMAC forwards all control frames to application even if they fail the Address Filter. 11: GMAC forwards control frames that pass the Address Filter.
[5]	RW	dbf	DBF: Disable Broadcast Frames When this bit is set, the AFM module filters all incoming broadcast frames. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast frames.
[4]	RW	pm	PM: Pass All Multicast When set, this bit indicates that all received frames with a multicast destination address (first bit in the destination address field is '1') are passed. When reset, filtering of multicast frame depends on HMC bit.
[3]	RW	daif	DAIF: DA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast frames. When reset, normal filtering of frames is performed.
[2]	RW	hmc	HMC: Hash Multicast When set, MAC performs destination address filtering of received multicast frames according to the hash table. When reset, the MAC performs a perfect destination address filtering for multicast frames, that is, it compares the DA field with the values programmed in DA registers. If Hash Filter is not selected during coreConsultant configuration, this bit is reserved (and RO).
[1]	RW	huc	HUC: Hash Unicast When set, MAC performs destination address filtering of unicast frames according to the hash table. When reset, the MAC performs a perfect destination address filtering for unicast frames, that is, it compares the DA field with the values programmed in DA registers. If Hash Filter is not selected during coreConsultant configuration, this bit is reserved (and RO).

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[0]	RW	pr	PR: Promiscuous Mode When this bit is set, the Address Filter module passes all incoming frames regardless of its destination or source address. The SA/DA Filter Fails status bits of the Receive Status Word are always cleared when PR is set.

GMACn_GMII_ADDR

The GMII Address register controls the management cycles to the external PHY through the management interface.

Offset Address	Register Name	Total Reset Value
0x0010	GMACn_GMII_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																pa				gr								cr				gw	gb
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserved
[15:11]	RW	pa	PA: Physical Layer Address This field tells which of the 32 possible PHY devices are being accessed. For RevMII, this field gives the PHY Address of the RevMII module.
[10:6]	RW	gr	GR: GMII Register These bits select the desired GMII register in the selected PHY device. For RevMII, these bits select the desired CSR register in RevMII Registers set.

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[5:2]	RW	cr	CR: CSR Clock Range The CSR Clock Range selection determines the frequency of the MDC clock as per the clk_csr_i frequency used in your design. The suggested range of clk_csr_i frequency applicable for each value below (when Bit[5] = 0) ensures that the MDC clock is approximately between the frequency range 1.0 MHz - 2.5 MHz. Selection clk_csr_i MDC Clock 0000 60-100 MHz clk_csr_i/42 0001 100-150 MHz clk_csr_i/62 0010 20-35 MHz clk_csr_i/16 0011 60-100 MHz clk_csr_i/26 0100 60-100 MHz clk_csr_i/102 0101 60-100 MHz clk_csr_i/124 0110,0111 Reserved When bit 5 is set, you can achieve MDC clock of frequency higher than the IEEE 802.3 specified frequency limit of 2.5 MHz and program a clock divider of lower value. For example, when clk_csr_i is of frequency 100 Mhz and you program these bits as "1010", then the resultant MDC clock is of 12.5 Mhz which is outside the limit of IEEE 802.3 specified range. Please program the values given below only if the interfacing chips supports faster MDC clocks. Selection MDC Clock 1000 clk_csr_i/4 1001 clk_csr_i/6 1010 clk_csr_i/8 1011 clk_csr_i/10 1100 clk_csr_i/12 1101 clk_csr_i/14 1110 clk_csr_i/16 1111 clk_csr_i/18 These bits are not used for accesssing RevMII. These bits are read-only if the RevMII interface is selected as single PHY interface in coreConsultant.
[1]	RW	gw	GW: GMII Write When set, this bit tells the PHY/RevMII that this is a Write operation using the GMII Data register. If this bit is not set, this is a Read operation, placing the data in the GMII Data register.

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[0]	RWSC	gb	GB: GMII Busy This bit should read a logic 0 before writing to Register 4 and Register 5. During a PHY/RevMII register access, the Software sets this bit to 1'b1 to indicate that a Read or Write access is in progress. The Register 5 is invalid until this bit is cleared by the GMAC. Therefore, Register 5 (GMII Data) should be kept valid until the GMAC clears this bit during a PHY Write operation. Similarly for read operation, Register 5 contents are not valid until this bit is cleared. The subsequent read/write operation should happen only after the previous operation is complete.

GMACn_GMII_DATA

The GMII Data register stores Write data to be written to the PHY register located at the address specified in Register 4. Register 5 also stores Read data from the PHY register located at the address specified by Register 4.

Offset Address	Register Name	Total Reset Value
0x0014	GMACn_GMII_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																gd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	gd	GD: GMII Data This contains the 16-bit data value read from the PHY/RevMII after a Management Read operation or the 16-bit data value to be written to the PHY/RevMII before a Management Write operation.

GMACn_ADDR0_HIGH

The MAC address 0 High register holds the upper 16 bits of the 6-byte first MAC address of the station.

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Offset Address	Register Name	Total Reset Value
0x0040	GMACn_ADDR0_HIGH	0x8000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mo	reserved															a_47_32															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31]	RO	mo	MO: Always 1
[30:16]	RO	reserved	Reserved
[15:0]	RW	a_47_32	A[47:32]: bit[47:32] of MAC Address0 This field contains the upper 16 bits (47:32) of the 6-byte first MAC address. This is used by the MAC for filtering for received frames and for inserting the MAC address in the Transmit Flow Control (PAUSE) Frames.

GMACn_ADDR0_LOW

The MAC address 0 low register holds the lower 32 bits of the 6-byte first MAC address of the station.

Offset Address	Register Name	Total Reset Value
0x0044	GMACn_ADDR0_LOW	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	A_31_0																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	A_31_0	A[31:0]: MAC Address0 [31:0] This field contains the lower 32 bits of the 6-byte first MAC address. This is used by the MAC for filtering for received frames and for inserting the MAC address in the Transmit Flow Control (PAUSE) Frames.

GMACn_ADDRx_HIGH

The MAC address x high register contains the higher 16 bits of the MAC address x(1–15).

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Offset Address	Register Name	Total Reset Value
0x0040 + x x 0x8 (x = 1–15)	GMACn_ADDRx_HIGH	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ae	sa	mbc						reserved								mac_addr_h16															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31]	RW	ae[1]	AE: Address Enable When this bit is set, the Address filter module uses the MAC address x(1-15) for perfect filtering. When reset, the address filter module ignores the address for filtering.
[30]	RW	sa	SA: Source Address When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received frame. When this bit is reset, the MAC address1 [47:0] is used to compare with the DA fields of the received frame.
[29:24]	RW	mbc	MBC: Mask Byte Control These bits are mask control bits for comparison of each of the MAC Address bytes. When set high, the GMAC core does not compare the corresponding byte of received DA/SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: Bit 29 Register 18[15:8] Bit 28 Register 18[7:0] Bit 27 Register 19[31:24] ... Bit 24 Register 19[7:0]
[23:16]	RO	reserved	Reserved
[15:0]	RW	mac_addr_h16	A[47:32]: MAC Address1 [47:32] This field contains the upper 16 bits (47:32) of the 6-byte second MAC address.

1

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GMACn_ADDRx_LOW

The MAC address x low register holds the lower 32 bits of the 6-byte MAC address x(1–15) of the station.

Offset Address	Register Name	Total Reset Value
0x0044 + x x 0x8 (x = 1–15)	GMACn_ADDRx_LOW	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	A_31_0																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	A_31_0	A[31:0]: MAC Address x(1~15) [31:0] This field contains the lower 32 bits of the 6-byte second MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

GMACn_ADDRy_HIGH

The MAC address y high register contains the higher 16 bits of the MAC address y(16–31).

Offset Address	Register Name	Total Reset Value
0x0780 + y x 0x8 (y = 16–31)	GMACn_ADDRy_HIGH	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ae	sa	mbc						reserved								mac_addr_h16															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	ae	AE: Address Enable When this bit is set, the Address filter module uses the MAC address y(16~31) for perfect filtering. When reset, the address filter module ignores the address for filtering.
[30]	RW	sa	SA: Source Address When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received frame. When this bit is reset, the MAC address1 [47:0] is used to compare with the DA fields of the received frame.

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[29:24]	RW	mbc	MBC: Mask Byte Control These bits are mask control bits for comparison of each of the MAC Address bytes. When set high, the GMAC core does not compare the corresponding byte of received DA/SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: Bit 29 Register 18[15:8] Bit 28 Register 18[7:0] Bit 27 Register 19[31:24] ... Bit 24 Register 19[7:0]
[23:16]	RO	reserved	Reserved
[15:0]	RW	mac_addr_h16	A[47:32]: MAC Address y(16~31) [47:32] This field contains the upper 16 bits (47:32) of the 6-byte second MAC address.

GMACn_ADDRy_LOW

The MAC address y low register holds the lower 32 bits of the 6-byte MAC address y(16–31) of the station.

Offset Address	Register Name	Total Reset Value
0x0784 + y x 0x8 (y = 16–31)	GMACn_ADDRy_LOW	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	A_31_0																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	A_31_0	A[31:0]: MAC Address y(16~31) [31:0] This field contains the lower 32 bits of the 6-byte second MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

GMACn_MMC_CTRL

The MMC control register establishes the operating mode of the management counters.**When Bit 0 and Bit 4 are set in the same cycle, Counters get preset immediately after getting cleared.**

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Offset Address	Register Name	Total Reset Value
0x0100	GMACn_MMC_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										fh_pre	cnt_pre	mmc_cf	rst_on_rd	cnt_sr	cnt_rst
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	RW	fh_pre	Full-Half preset When low and bit4 is set, all MMC counters get preset to almost-half value. All octet counters get preset to 0x7FFF_F800 (half - 2KBytes) and all frame-counters gets preset to 0x7FFF_FFF0 (half - 16). When high and bit4 is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (full - 2KBytes) and all frame-counters gets preset to 0xFFFF_FFF0 (full - 16). For 16-bit counters, the almost-half preset values are 0x7800 and 0x7FF0 for the respective octet and frame counters. Similarly, the almost-full preset values for the 16-bit counters are 0xF800 and 0xFFF0.
[4]	RWSC	cnt_pre	Counters Preset When set, all counters are initialized or preset to almost full or almost half as per Bit 5. This bit is cleared automatically after 1 clock cycle. This bit along with bit5 is useful for debugging and testing the assertion of interrupts because of MMC counter becoming half-full or full.
[3]	RW	mmc_cf	MMC Counter Freeze When set, this bit freezes all the MMC counters to their current value. (None of the MMC counters are updated because of any transmitted or received frame until this bit is reset to 0. If any MMC counter is read with the Reset on Read bit set, then that counter is also cleared in this mode.)
[2]	RW	rst_on_rd	Reset on Read When set, the MMC counters are reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (bits[7:0]) is read.
[1]	RW	cnt_sr	Counter Stop Rollover When set, counter after reaching maximum value does not roll over to zero.

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[0]	RWSC	cnt_rst	Counters Reset When set, all counters are reset. This bit is cleared automatically after 1 clock cycle

GMACn_MMC_txoctetcount_gb

The register for number of bytes transmitted, exclusive of preamble and retried bytes, in good and bad frames.

Offset Address	Register Name	Total Reset Value
0x0114	GMACn_MMC_txoctetcount_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txoctetcount_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txoctetcount_gb	Number of bytes transmitted, exclusive of preamble and retried bytes, in good and bad frames.

GMACn_MMC_txframecount_gb

The register for number of good and bad frames transmitted, exclusive of retried frames.

Offset Address	Register Name	Total Reset Value
0x0118	GMACn_MMC_txframecount_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txframecount_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txframecount_gb	Number of good and bad frames transmitted, exclusive of retried frames.

GMACn_MMC_txbroadcastframes_g

The register for number of good broadcast frames transmitted.

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Offset Address	Register Name	Total Reset Value
0x011C	GMACn_MMC_txbroadcastframes_g	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txbroadcastframes_g																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txbroadcastframes_g	Number of good broadcast frames transmitted.

GMACn_MMC_txmulticastframes_g

The register for number of good multicast frames transmitted.

Offset Address	Register Name	Total Reset Value
0x0120	GMACn_MMC_txmulticastframes_g	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txmulticastframes_g																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txmulticastframes_g	Number of good multicast frames transmitted.

GMACn_MMC_tx64octets_gb

The register for number of good and bad frames transmitted with length 64 bytes,exclusive of preamble and retried frames.

Offset Address	Register Name	Total Reset Value
0x0124	GMACn_MMC_tx64octets_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx64octets_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	tx64octets_gb	Number of good and bad frames transmitted with length 64 bytes, exclusive of preamble and retried frames.

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GMACn_MMC_tx65to127octets_gb

The register for number of good and bad frames transmitted with length between 65 and 127 (inclusive) bytes, exclusive of preamble and retried frames.

Offset Address	Register Name	Total Reset Value
0x0128	GMACn_MMC_tx65to127octets_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx65to127octets_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	tx65to127octets_gb	Number of good and bad frames transmitted with length between 65 and 127 (inclusive) bytes, exclusive of preamble and retried frames.

GMACn_MMC_tx128to255octets_gb

The register for number of good and bad frames transmitted with length between 128 and 255 (inclusive) bytes, exclusive of preamble and retried frames.

Offset Address	Register Name	Total Reset Value
0x012C	GMACn_MMC_tx128to255octets_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx128to255octets_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	tx128to255octets_gb	Number of good and bad frames transmitted with length between 128 and 255 (inclusive) bytes, exclusive of preamble and retried frames.

GMACn_MMC_tx256to511octets_gb

The register for number of good and bad frames transmitted with length between 256 and 511 (inclusive) bytes, exclusive of preamble and retried frames.

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Offset Address	Register Name	Total Reset Value
0x0130	GMACn_MMC_tx256to511octets_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx256to511octets_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	tx256to511octets_gb	Number of good and bad frames transmitted with length between 256 and 511 (inclusive) bytes, exclusive of preamble and retried frames.

GMACn_MMC_tx512to1023octets_gb

The register for number of good and bad frames transmitted with length between 512 and 1,023 (inclusive) bytes, exclusive of preamble and retried frames.

Offset Address	Register Name	Total Reset Value
0x0134	GMACn_MMC_tx512to1023octets_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx512to1023octets_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	tx512to1023octets_gb	Number of good and bad frames transmitted with length between 512 and 1,023 (inclusive) bytes, exclusive of preamble and retried frames.

GMACn_MMC_tx1024tomaxoctets_gb

The register for number of good and bad frames transmitted with length between 1,024 and maxsize (inclusive) bytes, exclusive of preamble and retried frames.

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Offset Address	Register Name	Total Reset Value
0x0138	GMACn_MMC_tx1024tomaxoctets_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx1024tomaxoctets_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	tx1024tomaxoctets_gb	Number of good and bad frames transmitted with length between 1,024 and maxsize (inclusive) bytes, exclusive of preamble and retried frames.

GMACn_MMC_txunicastframes_gb

The register for number of good and bad unicast frames transmitted.

Offset Address	Register Name	Total Reset Value
0x013C	GMACn_MMC_txunicastframes_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txunicastframes_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txunicastframes_gb	Number of good and bad unicast frames transmitted.

GMACn_MMC_txmulticastframes_gb

The register for number of good and bad multicast frames transmitted.

Offset Address	Register Name	Total Reset Value
0x0140	GMACn_MMC_txmulticastframes_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txmulticastframes_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txmulticastframes_gb	Number of good and bad multicast frames transmitted.

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GMACn_MMC_txbroadcastframes_gb

The register for number of good and bad broadcast frames transmitted.

Offset Address	Register Name	Total Reset Value
0x0144	GMACn_MMC_txbroadcastframes_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txbroadcastframes_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txbroadcastframes_gb	Number of good and bad broadcast frames transmitted.

GMACn_MMC_txunderflowerror

The register for number of frames aborted because of frame underflow error.

Offset Address	Register Name	Total Reset Value
0x0148	GMACn_MMC_txunderflowerror	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txunderflowerror																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txunderflowerror	Number of frames aborted because of frame underflow error.

GMACn_MMC_txsinglecol_g

The register for number of successfully transmitted frames after a single collision in Half-duplex mode.

Offset Address	Register Name	Total Reset Value
0x014C	GMACn_MMC_txsinglecol_g	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txsinglecol_g																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txsinglecol_g	Number of successfully transmitted frames after a single collision in Half-duplex mode.

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GMACn_MMC_txmulticol_g

The register for number of successfully transmitted frames after more than a single collision in Half-duplex mode.

Offset Address	Register Name	Total Reset Value
0x0150	GMACn_MMC_txmulticol_g	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txmulticol_g																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txmulticol_g	Number of successfully transmitted frames after more than a single collision in Half-duplex mode.

GMACn_MMC_txdeferred

The register for number of successfully transmitted frames after a deferral in Halfduplex mode.

Offset Address	Register Name	Total Reset Value
0x0154	GMACn_MMC_txdeferred	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txdeferred																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txdeferred	Number of successfully transmitted frames after a deferral in Halfduplex mode.

GMACn_MMC_txlatecol

The register for number of frames aborted because of late collision error.

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Offset Address	Register Name	Total Reset Value
0x0158	GMACn_MMC_txlatecol	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txlatecol																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txlatecol	Number of frames aborted because of late collision error.

GMACn_MMC_txexesscol

The register for number of frames aborted because of excessive (16) collision errors.

Offset Address	Register Name	Total Reset Value
0x015C	GMACn_MMC_txexesscol	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txexesscol																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txexesscol	Number of frames aborted because of excessive (16) collision errors.

GMACn_MMC_txcarriererror

The register for number of frames aborted because of carrier sense error (no carrier or loss of carrier).

Offset Address	Register Name	Total Reset Value
0x0160	GMACn_MMC_txcarriererror	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txcarriererror																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txcarriererror	Number of frames aborted because of carrier sense error (no carrier or loss of carrier).

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GMACn_MMC_txoctetcount_g

The register for number of bytes transmitted, exclusive of preamble, in good frames only.

Offset Address	Register Name	Total Reset Value
0x0164	GMACn_MMC_txoctetcount_g	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txoctetcount_g																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txoctetcount_g	Number of bytes transmitted, exclusive of preamble, in good frames only.

GMACn_MMC_txframecount_g

The register for number of good frames transmitted.

Offset Address	Register Name	Total Reset Value
0x0168	GMACn_MMC_txframecount_g	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txframecount_g																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txframecount_g	Number of good frames transmitted.

GMACn_MMC_txexcessdef

The register for number of frames aborted because of excessive deferral error (deferred for more than two max-sized frame times).

Offset Address	Register Name	Total Reset Value
0x016C	GMACn_MMC_txexcessdef	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txexcessdef																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txexcessdef	Number of frames aborted because of excessive deferral error (deferred for more than two max-sized frame times).

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GMACn_MMC_txpauseframes

The register for number of good PAUSE frames transmitted.

Offset Address	Register Name	Total Reset Value
0x0170	GMACn_MMC_txpauseframes	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txpauseframes																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txpauseframes	Number of good PAUSE frames transmitted.

GMACn_MMC_txvlanframes_g

The register for number of good VLAN frames transmitted, exclusive of retried frames.

Offset Address	Register Name	Total Reset Value
0x0174	GMACn_MMC_txvlanframes_g	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txvlanframes_g																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	txvlanframes_g	Number of good VLAN frames transmitted, exclusive of retried frames.

GMACn_MMC_rxframecount_gb

The register for number of good and bad frames received.

Offset Address	Register Name	Total Reset Value
0x0180	GMACn_MMC_rxframecount_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxframecount_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxframecount_gb	Number of good and bad frames received.

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GMACn_MMC_rxoctetcount_gb

The register for number of bytes received, exclusive of preamble, in good and bad frames.

Offset Address	Register Name	Total Reset Value
0x0184	GMACn_MMC_rxoctetcount_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxoctetcount_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxoctetcount_gb	Number of bytes received, exclusive of preamble, in good and bad frames.

GMACn_MMC_rxoctetcount_g

The register for number of bytes received, exclusive of preamble, only in good frames.

Offset Address	Register Name	Total Reset Value
0x0188	GMACn_MMC_rxoctetcount_g	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxoctetcount_g																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxoctetcount_g	Number of bytes received, exclusive of preamble, only in good frames.

GMACn_MMC_rxbroadcastframes_g

The register for number of good broadcast frames received.

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Offset Address	Register Name	Total Reset Value
0x018C	GMACn_MMC_rxbroadcastframes_g	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxbroadcastframes_g																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxbroadcastframes_g	Number of good broadcast frames received.

GMACn_MMC_rxmulticastframes_g

The register for number of good multicast frames received.

Offset Address	Register Name	Total Reset Value
0x0190	GMACn_MMC_rxmulticastframes_g	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxmulticastframes_g																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxmulticastframes_g	Number of good multicast frames received.

GMACn_MMC_rxcrcerror

The register for number of frames received with CRC error.

Offset Address	Register Name	Total Reset Value
0x0194	GMACn_MMC_rxcrcerror	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxcrcerror																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxcrcerror	Number of frames received with CRC error.

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GMACn_MMC_rxalignmenterror

The register for number of frames received with alignment (dribble) error. Valid only in 10/100 mode.

Offset Address	Register Name	Total Reset Value
0x0198	GMACn_MMC_rxalignmenterror	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxalignmenterror																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxalignmenterror	Number of frames received with alignment (dribble) error. Valid only in 10/100 mode.

GMACn_MMC_rxrunterror

The register for number of frames received with runt (<64 bytes and CRC error) error.

Offset Address	Register Name	Total Reset Value
0x019C	GMACn_MMC_rxrunterror	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxrunterror																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxrunterror	Number of frames received with runt (<64 bytes and CRC error) error.

GMACn_MMC_rxjabbererror

The register for number of giant frames received with length (including CRC) greater than 1,518 bytes (1,522 bytes for VLAN tagged) and with CRC error. If Jumbo Frame mode is enabled, then frames of length greater than 9,018 bytes (9,022 for VLAN tagged) are considered as giant frames.

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Offset Address	Register Name	Total Reset Value
0x01A0	GMACn_MMC_rxjabbererror	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxjabbererror																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxjabbererror	Number of giant frames received with length (including CRC) greater than 1,518 bytes (1,522 bytes for VLAN tagged) and with CRC error.

GMACn_MMC_rxundersize_g

The register for number of frames received with length less than 64 bytes, without any errors.

Offset Address	Register Name	Total Reset Value
0x01A4	GMACn_MMC_rxundersize_g	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxundersize_g																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxundersize_g	Number of frames received with length less than 64 bytes, without any errors.

GMACn_MMC_rxoversize_g

The register for number of frames received with length greater than the maxsize (1,518 or 1,522 for VLAN tagged frames), without errors.

Offset Address	Register Name	Total Reset Value
0x01A8	GMACn_MMC_rxoversize_g	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxoversize_g																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxoversize_g	Number of frames received with length greater than the maxsize (1,518 or 1,522 for VLAN tagged frames), without errors.

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GMACn_MMC_rx64octets_gb

Number of good and bad frames received with length 64 bytes, exclusive of preamble.

Offset Address	Register Name	Total Reset Value
0x01AC	GMACn_MMC_rx64octets_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx64octets_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rx64octets_gb	Number of good and bad frames received with length 64 bytes, exclusive of preamble.

GMACn_MMC_rx65to127octets_gb

The register for number of good and bad frames received with length between 65 and 127 (inclusive) bytes, exclusive of preamble.

Offset Address	Register Name	Total Reset Value
0x01B0	GMACn_MMC_rx65to127octets_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx65to127octets_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rx65to127octets_gb	Number of good and bad frames received with length between 65 and 127 (inclusive) bytes, exclusive of preamble.

GMACn_MMC_rx128to255octets_gb

The register for number of good and bad frames received with length between 128 and 255 (inclusive) bytes, exclusive of preamble.

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Offset Address	Register Name	Total Reset Value
0x01B4	GMACn_MMC_rx128to255octets_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx128to255octets_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rx128to255octets_gb	Number of good and bad frames received with length between 128 and 255 (inclusive) bytes, exclusive of preamble.

GMACn_MMC_rx256to511octets_gb

The register for number of good and bad frames received with length between 256 and 511 (inclusive) bytes, exclusive of preamble.

Offset Address	Register Name	Total Reset Value
0x01B8	GMACn_MMC_rx256to511octets_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx256to511octets_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rx256to511octets_gb	Number of good and bad frames received with length between 256 and 511 (inclusive) bytes, exclusive of preamble.

GMACn_MMC_rx512to1023octets_gb

The register for rx512to1023octets_gb number of good and bad frames received with length between 512 and 1,023 (inclusive) bytes, exclusive of preamble.

Offset Address	Register Name	Total Reset Value
0x01BC	GMACn_MMC_rx512to1023octets_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx512to1023octets_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rx512to1023octets_gb	rx512to1023octets_gb Number of good and bad frames received with length between 512 and 1,023 (inclusive) bytes, exclusive of preamble.

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GMACn_MMC_rx1024tomaxoctets_gb

The register for number of good and bad frames received with length between 1,024 and maxsize (inclusive) bytes, exclusive of preamble and retried frames.

Offset Address	Register Name	Total Reset Value
0x01C0	GMACn_MMC_rx1024tomaxoctets_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx1024tomaxoctets_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rx1024tomaxoctets_gb	Number of good and bad frames received with length between 1,024 and maxsize (inclusive) bytes, exclusive of preamble and retried frames.

GMACn_MMC_rxunicastframes_g

The register for number of good unicast frames received.

Offset Address	Register Name	Total Reset Value
0x01C4	GMACn_MMC_rxunicastframes_g	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxunicastframes_g																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxunicastframes_g	Number of good unicast frames received.

GMACn_MMC_rxlengtherror

The register for number of frames received with length error (Length type field ≠ frame size), for all frames with valid length field.

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Offset Address	Register Name	Total Reset Value
0x01C8	GMACn_MMC_rxlengtherror	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxlengtherror																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxlengtherror	Number of frames received with length error (Length type field ≠ frame size), for all frames with valid length field.

GMACn_MMC_rxoutofrangetype

The register for number of frames received with length field not equal to the valid frame size (greater than 1,501 but less than 1,536).

Offset Address	Register Name	Total Reset Value
0x01CC	GMACn_MMC_rxoutofrangetype	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxoutofrangetype																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxoutofrangetype	Number of frames received with length field not equal to the valid frame size (greater than 1,500 but less than 1,536).

GMACn_MMC_rxpauseframes

The register for number of good and valid PAUSE frames received.

Offset Address	Register Name	Total Reset Value
0x01D0	GMACn_MMC_rxpauseframes	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxpauseframes																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxpauseframes	Number of good and valid PAUSE frames received.

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GMACn_MMC_rxfifooverflow

The register for number of missed received frames because of FIFO overflow. This counter is not present in the GMAC-CORE configuration.

Offset Address	Register Name	Total Reset Value
0x01D4	GMACn_MMC_rxfifooverflow	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxfifooverflow																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxfifooverflow	Number of missed received frames because of FIFO overflow. This counter is not present in the GMAC-CORE configuration.

GMACn_MMC_rxvlanframes_gb

The register for number of good and bad VLAN frames received.

Offset Address	Register Name	Total Reset Value
0x01D8	GMACn_MMC_rxvlanframes_gb	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxvlanframes_gb																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxvlanframes_gb	Number of good and bad VLAN frames received.

GMACn_MMC_rxwatchdogerror

The register for number of frames received with error because of watchdog timeout error (frames with a data load larger than 2,048 bytes).

Offset Address	Register Name	Total Reset Value
0x01DC	GMACn_MMC_rxwatchdogerror	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxwatchdogerror																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxwatchdogerror	Number of frames received with error because of watchdog timeout error (frames with a data load larger than 2,048 bytes).

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DMAp_BUS_MODE

The bus mode register establishes the bus operating modes for the DMA.

Offset Address	Register Name	Total Reset Value
0x1000 + p x 0x100 (p = 0 or 2)	DMAp_BUS_MODE	0x0002_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				reserved				aal	pblx8	usp	rpbl				fb	reserved				pbl				atds	dsl					reserved	swr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:26]	RO	reserved	Reserved
[25]	RW	aal	AAL: Address-Aligned Beats When this bit is set high and the FB bit equals 1, the AXI interface generates all bursts aligned to the start address LS bits. If the FB bit is equal to 0, the first burst (accessing the data buffer's start address) is not aligned, but subsequent bursts are aligned to the address.
[24]	RW	pblx8	8xPBL Mode When set high, this bit multiplies the PBL value programmed (bits [22:17] and bits [13:8]) eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. Note: This bit function is not backward compatible. Before release 3.50a, this bit was 4xPBL.
[23]	RW	usp	USP: Use Separate PBL When set high, this bit configures the RxDMA to use the value configured in bits [22:17] as PBL while the PBL value in bits [13:8] is applicable to TxDMA operations only. When reset to low, the PBL value in bits [13:8] is applicable for both DMA engines.

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[22:17]	RW	rpbl	RPBL: RxDMA PBL These bits indicate the maximum number of beats to be transferred in one RxDMA transaction. This is the maximum value that is used in a single block Read/Write. The RxDMA always attempts to burst as specified in RPBL every time it starts a Burst transfer on the host bus. RPBL can be programmed with permissible values of 1, 2, 4, 8, 16, and 32. Any other value results in undefined behavior. These bits are valid and applicable only when USP is set high.
[16]	RW	fb	FB: Fixed Burst This bit controls whether the AXI Master interface performs fixed burst transfers or not. When set, the AHB uses only SINGLE, INCR4, INCR8, or INCR16 during start of normal burst transfers. When reset, the AXI uses SINGLE and INCR burst transfer operations.
[15:14]	RW	reserved	Reserved
[13:8]	RW	pbl	PBL: Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA transaction. This is the maximum value that is used in a single block Read/Write. The DMA always attempts to burst as specified in PBL each time it starts a Burst transfer on the host bus. PBL can be programmed with permissible values of 1, 2, 4, 8, 16, and 32. Any other value results in undefined behavior. When USP is set high, this PBL value is applicable for TxDMA transactions only. If the number of beats to be transferred is more than 32, then perform the following steps: 1. Set the 8xPBL mode. 2. Set the PBL. For example, if the maximum number of beats to be transferred is 64, then first set 8xPBL to 1 and then set PBL to 8. The PBL values have the following limitation: The maximum number of possible beats (PBL) is limited by the size of the Tx FIFO and Rx FIFO in the MTL layer and the data bus width on the DMA. The FIFO has a constraint that the maximum beat supported is half the depth of the FIFO, except when specified. For different data bus widths and FIFO sizes, the valid PBL range (including x8 mode) is provided in the following table. If the PBL is common for both transmit and receive DMA, the minimum Rx FIFO and Tx FIFO depths must be considered. Data Bus FIFO Depth Valid PBL Range Valid PBL Range Width in Full Duplex Mode (for TxFIFO only) in Half Duplex Mode 32 128 bytes 16 or less 8 or less (10/100 Mbps only) 256 bytes 32 or less 32 or less (10/100 Mbps only)512 bytes 64 or less 64 or less (10/100 Mbps only)1 KB 128 or less 128 or less in 10/100 Mbps, 64 or less in 1000-Mbps 2 KB and above All All 64 128 bytes 8 or less 4 or less (10/100 Mbps only)

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			256 bytes 16 or less 16 or less(10/100 Mbps only) 512 bytes 32 or less 32 or less (10/100 Mbps only) 1 KB 64 or less 64 in 10/100-Mbps operation, 32 or less in 1000-Mbps 2 KB 128 or less 128 or less 4 KB and above All All 128 128 bytes 4 or less 2 or less(10/100 Mbps only) 256 bytes 8 or less 8 or less(10/100 Mbps only) 512 bytes 16 or less 16 or less(10/100 Mbps only) 1KB 32 or less 32 in 10/100-Mbps operation, 16 or less in 1000-Mbps 2KB 64 or less 64 or less 4KB 128 or less 128 or less 8KB and above All All
[7]	RW	atds	ATDS: Alternate Descriptor Size When set, the size of the alternate descriptor increases to 32 bytes (8 DWORDS). This is required when the Advanced Timestamp feature or Full IPC Offload Engine is enabled in the receiver. This bit is present only when you select the Alternate Descriptor feature and any one of the following features during configuration: • Advanced Timestamp feature • IPC Full Checksum Offload (type 2) feature Otherwise, this bit is reserved and is read-only. When reset, the descriptor size reverts back to 4 DWORDs (16 bytes)
[6:2]	RW	dsl	DSL: Descriptor Skip Length This bit specifies the number of Word/Dword/Lword (depending on 32/64/128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of current descriptor to the start of next descriptor. When DSL value is equal to zero, then the descriptor table is taken as contiguous by the DMA, in Ring mode.
[1]	RW	reserved	Reserved
[0]	RWSC	swr	SWR: Software Reset When this bit is set, the MAC DMA Controller resets all GMAC Subsystem internal registers and logic. It is cleared automatically after the reset operation has completed in all of the core clock domains. Read a 0 value in this bit before re-programming any register of the core. Note: The reset operation is completed only when all the resets in all the active clock domains are de-asserted. Therefore, it is essential that all the PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion.

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DMAp_XMT_POLL_DEMAND

The transmit poll demand register enables the Transmit DMA to check whether or not the current descriptor is owned by DMA. The Transmit Poll Demand command is given to wake up the TxDMA if it is in Suspend mode. The TxDMA can go into Suspend mode because of an Underflow error in a transmitted frame or because of the unavailability of descriptors owned by Transmit DMA. You can give this command anytime and the TxDMA resets this command once it starts re-fetching the current descriptor from host memory.

Offset Address	Register Name	Total Reset Value
0x1004 + p x 0x100	DMAp_XMT_POLL_DEMAND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tpd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	ROWT	tpd	TPD: Transmit Poll Demand When these bits are written with any value, the DMA reads the current descriptor pointed to by Register 18. If that descriptor is not available (owned by Host), transmission returns to the Suspend state and DMA DMAp_STATUS[2] is asserted. If the descriptor is available, transmission resumes.

DMAp_RCV_POLL_DEMAND

The receive poll demand register enables the receive DMA to check for new descriptors.This command is given to wake up the RxDMA from SUSPEND state. The RxDMA can go into SUSPEND state only because of the unavailability of descriptors owned by it.

Offset Address	Register Name	Total Reset Value
0x1008 + p x 0x100 (p = 0 or 2)	DMAp_RCV_POLL_DEMAND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rpd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	ROWT	rpd	RPD: Receive Poll Demand When these bits are written with any value, the DMA reads the current descriptor pointed to by Register 19. If that descriptor is not available (owned by Host), reception returns to the Suspended state and DMAp_STATUS[7] is not asserted. If the descriptor is available, the Receive DMA returns to the active state.

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DMAp_RCV_BASE_ADDR

The receive descriptor list address register points to the start of the Receive Descriptor List.

Offset Address	Register Name	Total Reset Value
0x100C + p x 0x100 (p = 0 or 2)	DMAp_RCV_BASE_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rba																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rba	Start of Receive List This field contains the base address of the First Descriptor in the Receive

DMAp_TX_BASE_ADDR

The transmit descriptor list address register points to the start of the Transmit Descriptor List.

Offset Address	Register Name	Total Reset Value
0x1010 + p x 0x100 (p = 0 or 2)	DMAp_TX_BASE_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tba																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tba	Start of Transmit List This field contains the base address of the First Descriptor in the Transmit Descriptor list.

DMAp_STATUS

The status register contains all the status bits that the DMA reports to the host.The Software driver reads this register during an interrupt service routine or polling. Most of the fields in this register cause the host to be interrupted. DMAp_STATUS bits are not cleared when read. Writing 1'b1 to (unreserved) bits in DMAp_STATUS[16:0] clears these bits and writing 1'b0 has no effect. Each field (bits[16:0]) can be masked by masking the appropriate bit in Register 7.

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Offset Address	Register Name	Total Reset Value
0x1014 + p x 0x100 (p = 0 or 2)	DMAp_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				gmi	gli	eb		ts				rs			nis	ais	eri	fbi	reserved	eti	rwt	rps		ru	ri	unf	ovf	tjt	tu	tps	ti
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RO	gmi	GMI: GMAC MMC Interrupt This bit reflects an interrupt event in the MMC module of the GMAC core. The software must read the corresponding registers in the GMAC core to get the exact cause of interrupt and clear the source of interrupt to make this bit as 1'b0. The interrupt signal from the GMAC subsystem (sbd_intr_o) is high when this bit is high.
[26]	RO	gli	GLI: GMAC Line interface Interrupt This bit reflects an interrupt event in the GMAC Core's PCS interface block. The software must read the corresponding registers in the GMAC core to get the exact cause of interrupt and clear the source of interrupt to make this bit as 1'b0. The interrupt signal from the GMAC subsystem (sbd_intr_o) is high when this bit is high.
[25:23]	RO	eb	EB: Error Bits These bits indicate the type of error that caused a Bus Error (e.g., error response on the AXI interface). These bits are valid only when bit 13 (FBI: Fatal Bus Error Interrupt) is set. This field does not generate an interrupt. Bit 23: 0: Error during data transfer by RxDMA 1: Error during data transfer by TxDMA Bit 24: 0: Error during write transfer 1: Error during read transfer Bit 25: 0: Error during data buffer access 1: Error during descriptor access

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[22:20]	RO	ts	TS: Transmit Process State These bits indicate the Transmit DMA FSM state. This field does not generate an interrupt. 000: Stopped; Reset or Stop Transmit Command issued. 001: Running; Fetching Transmit Transfer Descriptor. 010: Running; Waiting for status. 011: Running; Reading Data from host memory buffer and queuing it to transmit buffer (Tx FIFO). 100: TIME_STAMP write state. 101: Reserved for future use. 110: Suspended; Transmit Descriptor Unavailable or Transmit Buffer Underflow. 111: Running; Closing Transmit Descriptor.
[19:17]	RO	rs	RS: Receive Process State These bits indicate the Receive DMA FSM state. This field does not generate an interrupt. 000: Stopped: Reset or Stop Receive Command issued. 001: Running: Fetching Receive Transfer Descriptor. 010: Reserved for future use. 011: Running: Waiting for receive packet. 100: Suspended: Receive Descriptor Unavailable. 101: Running: Closing Receive Descriptor. 110: TIME_STAMP write state. 111: Running: Transferring the receive packet data from receive buffer to host memory.
[16]	RWC	nis	NIS: Normal Interrupt Summary Normal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in DMA Register 7: • DMAp_STATUS[0]: Transmit Interrupt • DMAp_STATUS[2]: Transmit Buffer Unavailable • DMAp_STATUS[6]: Receive Interrupt • DMAp_STATUS[14]: Early Receive Interrupt Only unmasked bits affect the Normal Interrupt Summary bit. This is a sticky bit and must be cleared (by writing a 1 to this bit) each time a corresponding bit that causes NIS to be set is cleared.

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[15]	RWC	ais	AIS: Abnormal Interrupt Summary Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in DMA Register 7: DMAp_STATUS[1]: Transmit Process Stopped DMAp_STATUS[3]: Transmit Jabber Timeout DMAp_STATUS[4]: Receive FIFO Overflow DMAp_STATUS[5]: Transmit Underflow DMAp_STATUS[7]: Receive Buffer Unavailable DMAp_STATUS[8]: Receive Process Stopped DMAp_STATUS[9]: Receive Watchdog Timeout DMAp_STATUS[10]: Early Transmit Interrupt DMAp_STATUS[13]: Fatal Bus Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared.
[14]	RWC	eri	ERI: Early Receive Interrupt This bit indicates that the DMA had filled the first data buffer of the packet. Receive Interrupt DMAp_STATUS[6] automatically clears this bit.
[13]	RWC	fbi	FBI: Fatal Bus Error Interrupt This bit indicates that a bus error occurred, as detailed in [25:23]. When this bit is set, the corresponding DMA engine disables all its bus accesses.
[12:11]	RO	reserved	Reserved
[10]	RWC	eti	ETI: Early Transmit Interrupt This bit indicates that the frame to be transmitted was fully transferred to the MTL Transmit FIFO.
[9]	RWC	rwt	RWT: Receive Watchdog Timeout This bit is asserted when a frame with a length greater than 2,048 bytes is received (10, 240 when Jumbo Frame mode is enabled).
[8]	RWC	rps	RPS: Receive Process Stopped This bit is asserted when the Receive Process enters the Stopped state.
[7]	RWC	ru	RU: Receive Buffer Unavailable This bit indicates that the Next Descriptor in the Receive List is owned by the host and cannot be acquired by the DMA. Receive Process is suspended. To resume processing Receive descriptors, the host should change the ownership of the descriptor and issue a Receive Poll Demand command. If no Receive Poll Demand is issued, Receive Process resumes when the next recognized incoming frame is received. DMAp_STATUS[7] is set only when the previous Receive Descriptor was owned by the DMA.

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[6]	RWC	ri	RI: Receive Interrupt This bit indicates the completion of frame reception. Specific frame status information has been posted in the descriptor. Reception remains in the Running state.
[5]	RWC	unf	UNF: Transmit Underflow This bit indicates that the Transmit Buffer had an Underflow during frame transmission. Transmission is suspended and an Underflow Error TDES0[1] is set.
[4]	RWC	ovf	OVF: Receive Overflow This bit indicates that the Receive Buffer had an Overflow during frame reception. If the partial frame is transferred to application, the overflow status is set in RDES0[11].
[3]	RWC	tjt	TJT: Transmit Jabber Timeout This bit indicates that the Transmit Jabber Timer expired, meaning that the transmitter had been excessively active. The transmission process is aborted and placed in the Stopped state. This causes the Transmit Jabber Timeout TDES0[14] flag to assert
[2]	RWC	tu	TU: Transmit Buffer Unavailable This bit indicates that the Next Descriptor in the Transmit List is owned by the host and cannot be acquired by the DMA. Transmission is suspended. Bits[22:20] explain the Transmit Process state transitions. To resume processing transmit descriptors, the host should change the ownership of the bit of the descriptor and then issue a Transmit Poll Demand command.
[1]	RWC	tps	TPS: Transmit Process Stopped This bit is set when the transmission is stopped.
[0]	RWC	ti	TI: Transmit Interrupt This bit indicates that frame transmission is finished and TDES1[31] is set in the First Descriptor.

DMAp_CONTROL

The operation mode register establishes the Transmit and Receive operating modes and commands.Register 6 should be the last CSR to be written as part of DMA initialization.

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Offset Address	Register Name	Total Reset Value
0x1018 + p x 0x100 (p = 0 or 2)	DMAp_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						rsf	dff	rfa2	rfd2	tsf	ftf	reserved				ttc			st	rfd		rfa		efc	fef	fuf	reserved	rtc			osf	sr	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25]	RW	rsf	RSF: Receive Store and Forward When this bit is set, the MTL only reads a frame from the Rx FIFO after the complete frame has been written to it, ignoring RTC bits. When this bit is reset, the Rx FIFO operates in Cut-Through mode, subject to the threshold specified by the RTC bits.
[24]	RW	dff	DFF: Disable Flushing of Received Frames When this bit is set, the RxDMA does not flush any frames because of the unavailability of receive descriptors/buffers as it does normally when this bit is reset. (See “Receive Process Suspended” on page 66.) This bit is reserved (and RO) in GMAC-MTL configuration.
[23]	RW	rfa2	RFA[2]: MSB of Threshold for Activating Flow Control If the GMAC-UNIV is configured for an Rx FIFO depth of 8 KB or more, this bit (when set) provides additional threshold levels for activating the Flow Control in both Half- Duplex and Full-Duplex modes. This bit (as Most Significant Bit) along with the RFA (bits [10:9]) give the following thresholds for activating flow control. 100: Full minus 5 KB 101: Full minus 6 KB 110: Full minus 7 KB 111: Reserved This bit is reserved (and RO) if the Rx FIFO is 4 KB or less deep.

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[22]	RW	rfd2	RFD[2]: MSB of Threshold for Deactivating Flow Control If the GMAC-UNIV is configured for an Rx FIFO depth of 8 KB or more, this bit (when set) provides additional threshold levels for deactivating the Flow Control in both Half- Duplex and Full-Duplex modes. This bit (as Most Significant Bit) along with the RFD (bits [12:11]) give the following thresholds for deactivating flow control. 100: Full minus 5 KB 101: Full minus 6 KB 110: Full minus 7 KB 111: Reserved This bit is reserved (and RO) if the Rx FIFO is 4 KB or less deep.
[21]	RW	tsf	TSF: Transmit Store and Forward When this bit is set, transmission starts when a full frame resides in the MTL Transmit FIFO. When this bit is set, the TTC values specified in Register 6[16:14] are ignored. This bit should be changed only when transmission is stopped.
[20]	RWC	ftf	FTF: Flush Transmit FIFO When this bit is set, the transmit FIFO controller logic is reset to its default values and thus all data in the Tx FIFO is lost/flushed. This bit is cleared internally when the flushing operation is completed fully. The Operation Mode register should not be written to until this bit is cleared. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt frame transmission. Note: The flush operation completes only after emptying the TxFIFO of its contents and all the pending Transmit Status of the transmitted frames are accepted by the host. In order to complete this flush operation, the PHY transmit clock (clk_tx_i) is required to be active.
[19:17]	RO	reserved	Reserved
[16:14]	RW	ttc	TTC: Transmit Threshold Control These three bits control the threshold level of the MTL Transmit FIFO. Transmission starts when the frame size within the MTL Transmit FIFO is larger than the threshold. In addition, full frames with a length less than the threshold are also transmitted. These bits are used only when the TSF bit (Bit 21) is reset. 000: 64 001: 128 010: 192 011: 256 100: 40 101: 32 110: 24 111: 16

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[13]	RW	st	ST: Start/Stop Transmission Command When this bit is set, transmission is placed in the Running state, and the DMA checks the Transmit List at the current position for a frame to be transmitted. Descriptor acquisition is attempted either from the current position in the list, which is the Transmit List Base Address set by Register 4, or from the position retained when transmission was stopped previously. If the current descriptor is not owned by the DMA, transmission enters the Suspended state and Transmit Buffer Unavailable (DMAp_STATUS[2]) is set. The Start Transmission command is effective only when transmission is stopped. If the command is issued before setting DMA Register 4, then the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current frame. The Next Descriptor position in the Transmit List is saved, and becomes the current position when transmission is restarted. The stop transmission command is effective only when the transmission of the current frame is complete or the transmission is in the Suspended state.
[12:11]	RW	rfd	RFD: Threshold for deactivating flow control (in both HD and FD) These bits control the threshold (Fill-level of Rx FIFO) at which the flow-control is de- asserted after activation. 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Note that the de-assertion is effective only after flow control is asserted. If the Rx FIFO is 8 KB or more, an additional bit (RFD[2]) is used for more threshold levels as described in bit [22]. These bits are reserved and read-only when RxFIFO depth is less than 4 KB.
[10:9]	RW	rfa	RFA: Threshold for activating flow control (in both HD and FD) These bits control the threshold (Fill level of Rx FIFO) at which flow control is activated. 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Note that the above only applies to Rx FIFOs of 4 KB or more when the EFC bit is set high. If the Rx FIFO is 8 KB or more, an additional bit (RFA[2]) is used for more threshold levels as described in bit [23]. These bits are reserved and read-only when RxFIFO depth is less than 4 KB.

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[8]	RW	efc	EFC: Enable HW flow control When this bit is set, the flow control signal operation based on fill-level of Rx FIFO is enabled. When reset, the flow control operation is disabled. This bit is not used (reserved and always reset) when the Rx FIFO is less than 4 KB.
[7]	RW	fef	FEF: Forward Error Frames When this bit is reset, the Rx FIFO drops frames with error status (CRC error, collision error, GMII_ER, giant frame, watchdog timeout, overflow). However, if the frame's start byte (write) pointer is already transferred to the read controller side (in Threshold mode), then the frames are not dropped. In GMAC-MTL configuration in which the Frame Length FIFO is also enabled during coreConsultant configuration, the Rx FIFO drops the error frames if that frame's start byte is not transferred (output) on the ARI bus. When FEF bit is set, all frames except runt error frames are forwarded to the DMA. But when RxFIFO overflows when a partial frame is written, then such frames are dropped even when FEF is set.
[6]	RW	fuf	FUF: Forward Undersized Good Frames When set, the Rx FIFO forwards Undersized frames (frames with no Error and length less than 64 bytes) including pad-bytes and CRC). When reset, the Rx FIFO drops all frames of less than 64 bytes, unless it is already transferred because of lower value of Receive Threshold (e.g., RTC = 01).
[5]	RO	reserved	Reserved
[4:3]	RW	rtc	RTC: Receive Threshold Control These two bits control the threshold level of the MTL Receive FIFO. Transfer (request) to DMA starts when the frame size within the MTL Receive FIFO is larger than the threshold. In addition, full frames with a length less than the threshold are transferred automatically. Note that value of 11 is not applicable if the configured Receive FIFO size is 128 bytes. These bits are valid only when the RSF bit is zero, and are ignored when the RSF bit is set to 1. 00: 64 01: 32 10: 96 11: 128
[2]	RW	osf	OSF: Operate on Second Frame When this bit is set, this bit instructs the DMA to process a second frame of Transmit data even before status for first frame is obtained.

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[1]	RW	sr	SR: Start/Stop Receive When this bit is set, the Receive process is placed in the Running state. The DMA attempts to acquire the descriptor from the Receive list and processes incoming frames. Descriptor acquisition is attempted from the current position in the list, which is the address set by DMA Register 3 or the position retained when the Receive process was previously stopped. If no descriptor is owned by the DMA, reception is suspended and Receive Buffer Unavailable (DMAp_STATUS[7]) is set. The Start Receive command is effective only when reception has stopped. If the command was issued before setting DMA Register 3, DMA behavior is unpredictable. When this bit is cleared, RxDMA operation is stopped after the transfer of the current frame. The next descriptor position in the Receive list is saved and becomes the current position after the Receive process is restarted. The Stop Receive command is effective only when the Receive process is in either the Running (waiting for receive packet) or in the Suspended state.
[0]	RO	reserved	Reserved

DMAp_INTR_ENA

The interrupt enable register enables the interrupts reported by DMAp_STATUS.Setting a bit to 1'b1 enables a corresponding interrupt. After a hardware or software reset, all interrupts are disabled.

Offset Address	Register Name	Total Reset Value
0x101C + p x 0x100 (p = 0 or 2)	DMAp_INTR_ENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																nie	aie	ere	fbe	reserved				ete	rwe	rse	rue	rie	une	ove	tje	tue	tse	tie
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved

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[16]	RW	nie	NIE: Normal Interrupt Summary Enable When this bit is set, a normal interrupt is enabled. When this bit is reset, a normal interrupt is disabled. This bit enables the following bits: • DMAp_STATUS[0] Transmit Interrupt • DMAp_STATUS[2] Transmit Buffer Unavailable • DMAp_STATUS[6] Receive Interrupt • DMAp_STATUS[14] Early Receive Interrupt
[15]	RW	aie	AIE: Abnormal Interrupt Summary Enable When this bit is set, an Abnormal Interrupt is enabled. When this bit is reset, an Abnormal Interrupt is disabled. This bit enables the following bits • DMAp_STATUS[1] Transmit Process Stopped • DMAp_STATUS[3] Transmit Jabber Timeout • DMAp_STATUS[4] Receive Overflow • DMAp_STATUS[5] Transmit Underflow • DMAp_STATUS[7] Receive Buffer Unavailable • DMAp_STATUS[8] Receive Process Stopped • DMAp_STATUS[9] Receive Watchdog Timeout • DMAp_STATUS[10] Early Transmit Interrupt • DMAp_STATUS[13] Fatal Bus Error
[14]	RW	ere	ERE: Early Receive Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Register 7[16]), Early Receive Interrupt is enabled. When this bit is reset, Early Receive Interrupt is disabled.
[13]	RW	fbe	FBE: Fatal Bus Error Enable When this bit is set with Abnormal Interrupt Summary Enable (Register 7[15]), the Fatal Bus Error Interrupt is enabled. When this bit is reset, Fatal Bus Error Enable Interrupt is disabled.
[12:11]	RO	reserved	Reserved
[10]	RW	ete	ETE: Early Transmit Interrupt Enable When this bit is set with an Abnormal Interrupt Summary Enable (Register 7[15]), Early Transmit Interrupt is enabled. When this bit is reset, Early Transmit Interrupt is disabled.
[9]	RW	rwe	RWE: Receive Watchdog Timeout Enable When this bit is set with Abnormal Interrupt Summary Enable (Register 7[15]), the Receive Watchdog Timeout Interrupt is enabled. When this bit is reset, Receive Watchdog Timeout Interrupt is disabled.

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[8]	RW	rse	RSE: Receive Stopped Enable When this bit is set with Abnormal Interrupt Summary Enable (Register 7[15]), Receive Stopped Interrupt is enabled. When this bit is reset, Receive Stopped Interrupt is disabled.
[7]	RW	rue	RUE: Receive Buffer Unavailable Enable When this bit is set with Abnormal Interrupt Summary Enable (Register 7[15]), Receive Buffer Unavailable Interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable Interrupt is disabled.
[6]	RW	rie	RIE: Receive Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Register 7[16]), Receive Interrupt is enabled. When this bit is reset, Receive Interrupt is disabled.
[5]	RW	une	UNE: Underflow Interrupt Enable When this bit is set with Abnormal Interrupt Summary Enable (Register 7[15]), Transmit Underflow Interrupt is enabled. When this bit is reset, Underflow Interrupt is disabled.
[4]	RW	ove	OVE: Overflow Interrupt Enable When this bit is set with Abnormal Interrupt Summary Enable (Register 7[15]), Receive Overflow Interrupt is enabled. When this bit is reset, Overflow Interrupt is disabled
[3]	RW	tje	TJE: Transmit Jabber Timeout Enable When this bit is set with Abnormal Interrupt Summary Enable (Register 7[15]), Transmit Jabber Timeout Interrupt is enabled. When this bit is reset, Transmit Jabber Timeout Interrupt is disabled.
[2]	RW	tue	TUE: Transmit Buffer Unavailable Enable When this bit is set with Normal Interrupt Summary Enable (Register 7[16]), Transmit Buffer Unavailable Interrupt is enabled. When this bit is reset, Transmit Buffer Unavailable Interrupt is disabled.
[1]	RW	tse	TSE: Transmit Stopped Enable When this bit is set with Abnormal Interrupt Summary Enable (Register 7[15]), Transmission Stopped Interrupt is enabled. When this bit is reset, Transmission Stopped Interrupt is disabled.
[0]	RW	tie	TIE: Transmit Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Register 7[16]), Transmit Interrupt is enabled. When this bit is reset, Transmit Interrupt is disabled.

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DMAp_MISSED_FRAME_CTR

The register reports the current value of two counters to track the number of missed frames during reception. The counter is used for diagnostic purposes. Bits[15:0] indicate missed frames because of the host buffer being unavailable. Bits[27:17] indicate missed frames because of buffer overflow conditions (MTL and GMAC) and runt frames (good frames of less than 64 bytes) dropped by the MTL.

Offset Address	Register Name	Total Reset Value
0x1020 + p x 0x100 (p = 0 or 2)	DMAp_MISSED_FRAME_CTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ob_fifo_overflow_cnt	app_miss_frms										ob_miss_frms_cnt	ctrl_miss_frms															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28]	RC	ob_fifo_overflow_cnt	Overflow bit for FIFO Overflow Counter
[27:17]	RC	app_miss_frms	Indicates the number of frames missed by the application. This counter is incremented each time the MTL asserts the sideband signal mtl_rxoverflow_o. The counter is cleared when this register is read with mci_be_i[2] at 1'b1.
[16]	RC	ob_miss_frms_cnt	Overflow bit for Missed Frame Counter
[15:0]	RC	ctrl_miss_frms	Indicates the number of frames missed by the controller because of the Host Receive Buffer being unavailable. This counter is incremented each time the DMA discards an incoming frame. The counter is cleared when this register is read with mci_be_i[0] at 1'b1.

DMAp_CUR_TX_BUF_ADDR

The current host yransmit buffer address register points to the current Transmit Buffer Address being read by the DMA.

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Offset Address	Register Name	Total Reset Value
0x1050 + p x 0x100 (p = 0 or 2)	DMAp_CUR_TX_BUF_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	curr_tx_buf_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	curr_tx_buf_addr	Host Transmit Buffer Address Pointer Cleared on Reset. Pointer updated by DMA during operation.

DMAp_CUR_RX_BUF_ADDR

The current host receive buffer address register points to the current Receive Buffer address being read by the DMA.

Offset Address	Register Name	Total Reset Value
0x1054 + p x 0x100 (p = 0 or 2)	DMAp_CUR_RX_BUF_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	curr_rx_buff_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	curr_rx_buff_addr	Host Receive Buffer Address Pointer Cleared on Reset. Pointer updated by DMA during operation.

CT_LOCAL_MACADDR0_U16

Local Mac address register for port 0, upper 16 bits. This is the devices Mac Address.

Offset Address	Register Name	Total Reset Value
0x8100	CT_LOCAL_MACADDR0_U16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mac0_addr_u16															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

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Offset Address	Register Name	Total Reset Value
0x8100	CT_LOCAL_MACADDR0_U16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mac0_addr_u16															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	mac0_addr_u16	Upper 16 bits of mac0 address stored in canonical format

CT_LOCAL_MACADDR0_L32

Local Mac address registerfor port 0, lower 32 bits. This is the devices Mac Address.

Offset Address	Register Name	Total Reset Value
0x8104	CT_LOCAL_MACADDR0_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mac0_addr_l32																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mac0_addr_l32	Lower 32 bits of mac address stored in canonical format

CT_LOCAL_IPADDR0

Local IP address register for port 0. This is the devices IP Address for port 0.

Offset Address	Register Name	Total Reset Value
0x8108	CT_LOCAL_IPADDR0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mac0_ip_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mac0_ip_addr	32 bits of IP address of mac1 stored in canonical format

TOE_CTRL

The register for TOE number of Retries Allowed and ms Timer Reset Value.

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Offset Address	Register Name	Total Reset Value
0x814C	TOE_CTRL	0x25D7_80FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer_rst_val																				num_entries											
Reset	0	0	1	0	0	1	0	1	1	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:12]	RW	timer_rst_val	Value in counter divided by system clock gives millisecond reset value (current value based on system clock of 155MHz).
[11:0]	RW	num_entries	Number of entries allowed

TNK_INTR_STAT

Interrupt status register.The Synopsys GMAC Databook recommends reading the DMA 'Status Register' for each channel to determine which channel generated an interrupt. Alternatively the TNK_INTR_STAT can be read to determine which channel asserted an interrupt.

Offset Address	Register Name	Total Reset Value
0x9000	TNK_INTR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								toe_int	reserved	gmac0_int	dma_ch2_int	reserved	dma_ch0_int	dma_ttx_err_int	dma_ttx_ack_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	toe_int	An interrupt is asserted by the toe engine.
[6]	RW	reserved	Reserved
[5]	RW	gmac0_int	GMAC0 interrupt. Note that it is not necessary to use this interrupt as it is also reflected through dma_ch0_int.
[4]	RW	dma_ch2_int	An interrupt is asserted for channel 2 DMA Rx or Tx.
[3]	RW	reserved	Reserved
[2]	RW	dma_ch0_int	An interrupt is asserted for channel 0 DMA Rx or Tx

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[1]	RW	dma_ttx_err_int	An error was detected by the Toe Transmit DMA engine. See CSR DMA_TTX_ERR.
[0]	RW	dma_ttx_ack_int	This interrupt when one or more descriptors are being returned to software after data is acknowledged by TCP. See CSR DMA_TTX_ACKD_CID.

TNK_INTR_EN

Interrupt enables register.

Offset Address	Register Name	Total Reset Value
0x09004	TNK_INTR_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								toe_ien	reserved	gmac0_ien	dma_ch2_ien	reserved	dma_ch0_ien	dma_ttx_err_ien	dma_ttx_ack_ien
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	toe_ien	Interrupt enable for toe_int.
[6]	RW	reserved	Reserved
[5]	RW	gmac0_ien	Interrupt enable for all interrupts from the gmac0 instance.
[4]	RW	dma_ch2_ien	Interrupt enable for all interrupts from DMA channel 2.
[3]	RW	reserved	Reserved
[2]	RW	dma_ch0_ien	Interrupt enable for all interrupts from DMA channel 0.
[1]	RW	dma_ttx_err_ien	Interrupt enable for dma_ttx_err_int.
[0]	RW	dma_ttx_ack_ien	Interrupt enable for dma_ttx_ack_int.

TNK_RESET_STAT

MAC reset status register.

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Offset Address	Register Name	Total Reset Value
0x09008	TNK_RESET_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mac0_in_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	mac0_in_reset	If 1 then the reset to MAC 0 is asserted. Note that the MAC will not come out of reset until the MAC Rx clock and MAC Tx clock are both toggling.

TNK_ID

The register for number of connections supported and HW release ID

Offset Address	Register Name	Total Reset Value
0x0900C	TNK_ID	0x00FF_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	num_conn																tnk_id															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	num_conn	Number of connections supported.
[15:0]	RO	tnk_id	HW Release ID.

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Contents

6 Video Decoder 6-1
6.1 VDH 6-1
6.1.1 Overview 6-1
6.1.2 Function Description 6-1
6.1.3 Operating Mode 6-1
6.2 JPGD 6-3
6.2.1 Overview 6-3
6.2.2 Function Description 6-3
6.2.3 Operating Mode 6-5

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Figures

Figure 6-1 Architecture of the video decoder 6-2
Figure 6-2 JPGD architecture 6-4
Figure 6-3 Structure of JPEG streams 6-5

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Tables

Table 6-1 Internal modules of the JPGD.....6-4

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6 Video Decoder

6.1 VDH

6.1.1 Overview

The video decoder consists of a video firmware (VFMW) running on the ARM processor and an embedded video decoding module for high definition (VDH). The VFMW obtains streams from the upper-layer software, parses the streams, and calls the VDH to generate the sequences of decoded pictures. Under the control of the upper-layer software, the video display (VDP) module outputs the sequences to a monitor or other devices.

6.1.2 Function Description

The video decoder has the following features:

- H.264 baseline profile level 5.0 decoding
- H.264 main profile (MP) level 5.0 decoding
- H.264 high profile (HP) level 5.0 decoding
- MPEG4 simple profile (SP) levels 0–3 decoding
- MPEG4 advanced simple profile (ASP) levels 0–5/MPEG4 short head decoding
- Maximum resolution: 5632x4224 (for the H.264 format) or 1920x1088 (for other formats)
- Decoding performance: 1080P@60fps

6.1.3 Operating Mode

Figure 6-1 shows the architecture of the video decoder.

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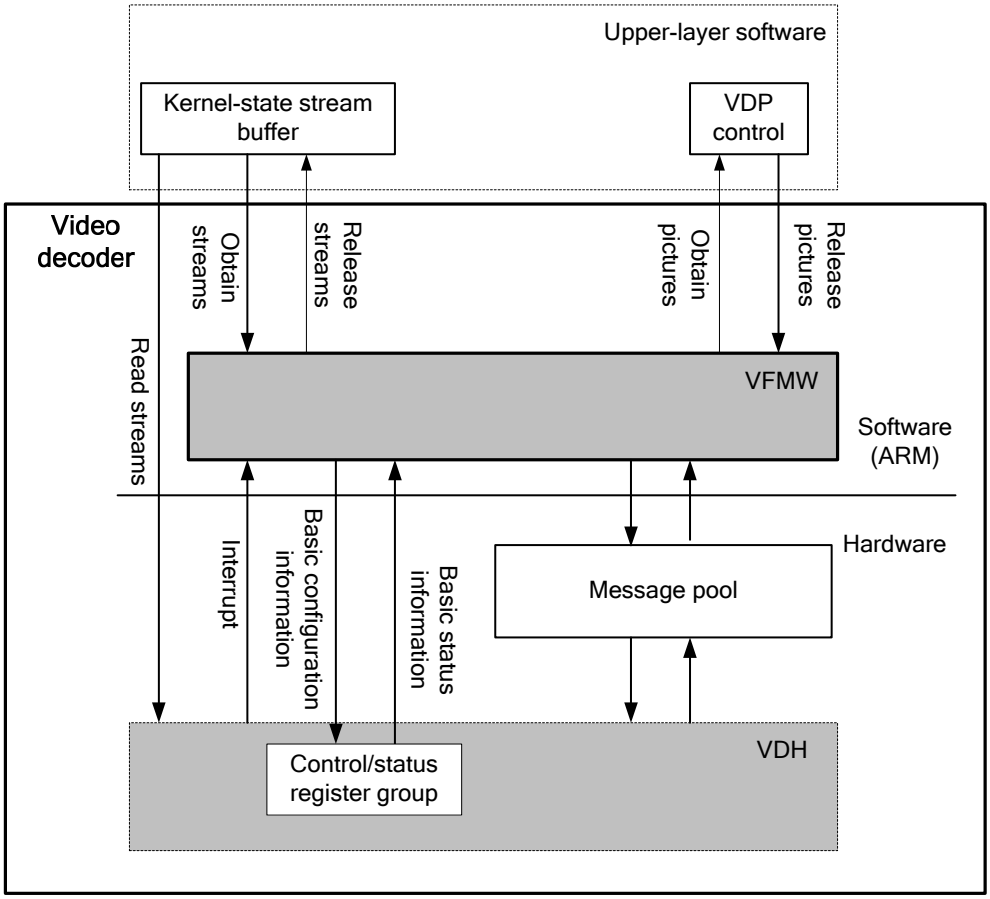
Figure 6-1 Architecture of the video decoder



NOTE

- VDH: a video decoding module for high definition supporting multiple protocols.
- VFMW: a software component running on the primary processor for scheduling the VDH.
- Message pool: a memory located in the external synchronous dynamic random access memory (SDRAM) for exchanging the messages between the VFMW and the VDH. It can be read and written by both the VDH and the VFMW.

The VDH and VFMW interact with each other in the following two modes:

- The VDH and VFMW interact with each other to decode streams complying with the H.264 protocol by slices. To be specific, the VFMW decodes the slice header and the streams before the slice header, and the VDH decodes the slice data and the streams after the slice data.
- The VDH and VFMW interact with each other by frames for the streams complying with other protocols. The VFMW decodes picture headers and the streams before picture headers, and the VDH decodes other streams. To support multi-channel decoding, the VFMW enables the VDH by frames in time-division multiplexing (TDM) mode.

To decode videos, perform the following steps:

Step 1 Create a decoder, and initialize it.

Step 2 Store streams in the stream buffer.

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Step 3 Obtain pictures over the picture output interface of the VFMW.

Step 4 Release the pictures over the frame recycle interface of the VFMW after the pictures are displayed.

Step 5 Repeat step 2 through step 4 until all streams are decoded.

Step 6 Destroy the video decoder after all streams are played.

----End

6.2 JPGD

6.2.1 Overview

The JPEG decoder (JPGD) decodes static JPEG and Motion-JPEG pictures.

6.2.2 Function Description

The JPGD has the following features:

- Supports the advanced eXtensible interface (AXI).
- Supports interrupts.
- Supports ITU-T81 baseline profile decoding.
  - JPEG picture decoding of YUV components in five formats including YUV 4:0:0, YUV4:2:0, YUV4:2:2 1x2, YUV4:2:2 2x1, and YUV 4:4:4.
  - A maximum of four Huffman tables including two direct coefficient (DC) tables and two alternating coefficient (AC) tables.
  - A maximum of three quantization tables.
  - Sequential decoding.
  - Discrete cosine transform-based (DCT-based) JPEG decoding.
  - 8-bit depth.
  - Interleaved scanning.
- Supports 1/2, 1/4, or 1/8 frequency domain scaling.
- Decodes the static pictures with the maximum resolution 8192x8192 and with the minimum resolution 1x1.
- Supports the semi-planar output storage format with the maximum resolution 8192x8192.
- Supports segment decoding of compressed streams.
- Provides the decoding rate of 40 megapixel/s or 3-channel MJPEG D1 30 frames/s, satisfying the strict real-time requirements of various decoding systems.
- Supports frequency domain scaling to reduce the usage of the memory and bandwidth during decoding.

Figure 6-2 shows the JPGD architecture.

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Figure 6-2 JPGD architecture

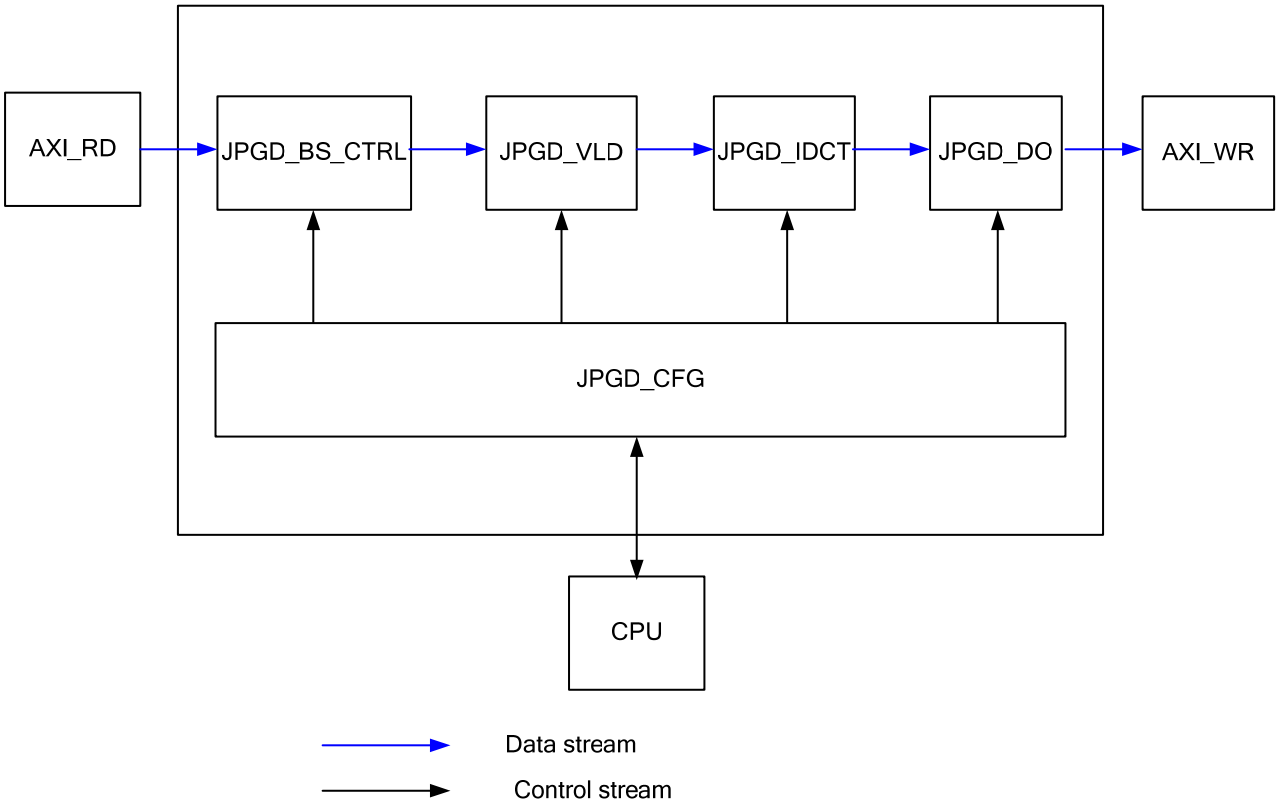

Table 6-1 describes the internal modules of the JPGD.

Table 6-1 Internal modules of the JPGD

Module	Description
JPGD_BS_CTRL	This module reads and shifts streams. It contains a shift barrel that sends valid streams to downstream modules for decoding.
JPGD_VLD	This module decodes Huffman variable-length codes and performs inverse scanning and dequantization on coefficients after decoding.
JPGD_IDCT	This module performs inverse discrete cosine transform (IDCT) and scales the frequency domain.
JPGD_DO	This module stores the decoded data in the specified DDR.
JPGD_CFG	This module receives the configuration information about the host, and configures each functional modules based on the configuration information. In addition, this module starts the decoder, generates interrupts, and reports the internal status information about the decoder to the host.

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6.2.3 Operating Mode

6.2.3.1 Classification of Software and Hardware

Figure 6-3 shows the structure of JPEG streams.

Figure 6-3 Structure of JPEG streams

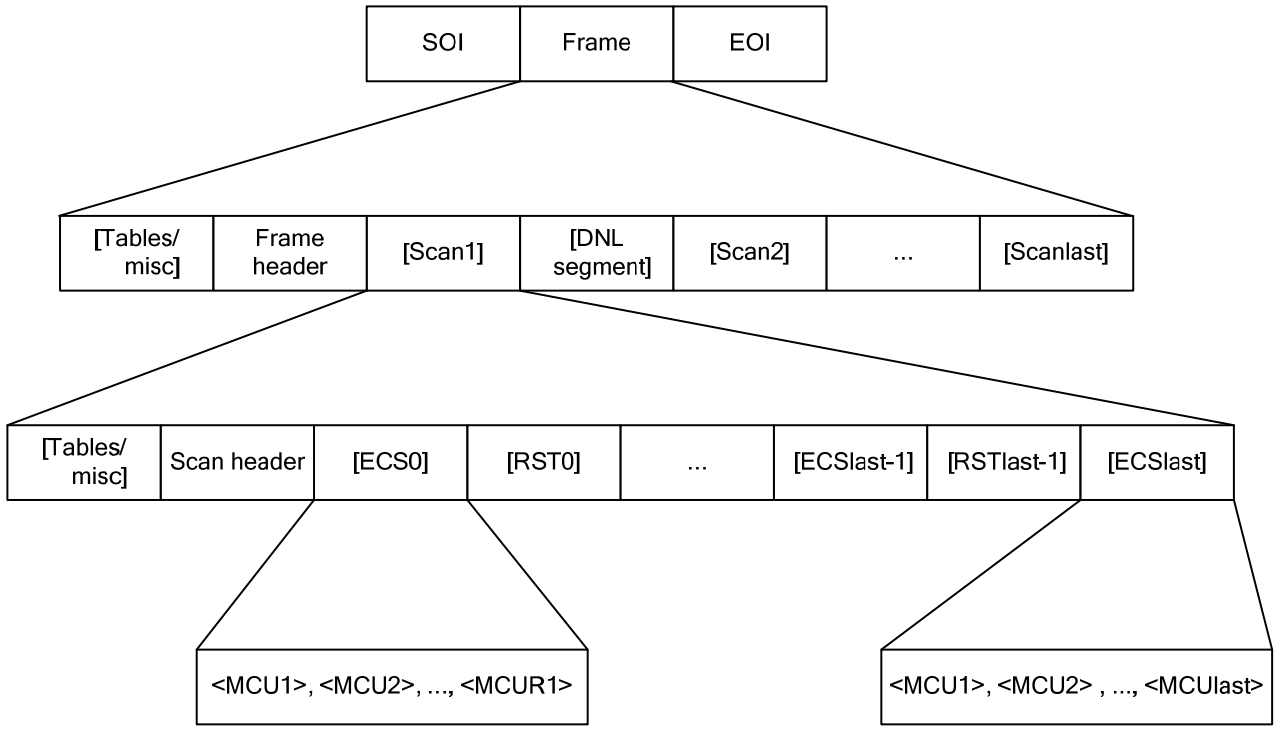

Figure 6-3 is a generalized structure diagram. For the JPEG streams, the scan header and its upper layer are parsed by software; the ECS layer and RSTn flags are parsed by hardware.

6.2.3.2 Interaction Between Software and Hardware

The JPEG decoding is performed by software and hardware, and the software and hardware interact with each other during decoding.

- Except the process of resuming streams, software and hardware interact by frames.
  - Software and hardware interact once for each JPEG frame.
  - Software and hardware also interact once for each Motion-JPEG frame.
- Software and hardware can interact in query mode or in interrupt mode. Interrupts are generated in any of the following ways:
  - An interrupt is generated after the current picture is decoded. This interrupt indicates that the current picture is decoded completely and stored in the external memory and the JPEG decoding is complete. As the baseline picture has only one scan layer, when the decoding of the scan layer is complete, it indicates that a picture is decoded.
  - An interrupt is generated when the currently configured streams are used up. This interrupt indicates that an error occurs during the current decoding process. Therefore, the JPGD cannot continue to decode pictures and the decoding process ends.

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– After the currently configured streams are used up, the decoder is started to continue to perform decoding when new streams are configured by software–.

6.2.3.3 Refilling Streams

Because of the limits on the memory, not all the streams can be read and stored in the DDR at one time during picture decoding. Therefore, the stream refilling mechanism is used. In this way, only a segment of streams is read at one time. When the streams are used up, the next segment of streams are read and stored in the DDR through stream refilling.

To simplify the interaction between software and hardware during stream refilling, streams are refilled as follows:

Step 1 The JPGD receives only a segment of consecutive streams at one time. That is, before the JPGD is started for decoding, the VFMW only needs to configure a physical storage start address and a physical storage end address (in byte) for the JPGD.

Step 2 After the JPGD decodes the current streams, decoding stops and a stream refilling interrupt is reported.

Step 3 After software receives the stream refilling interrupt, the JPGD can be restarted when the start address and end address for storing the next segment of streams are configured. To be specific, the JPGD is started when the value 1 is written to the JPGD_RESUME_START register. Note that the streams cannot be less than 64 bytes each time the JPGD is started.

Step 4 The JPGD obtains new streams for decoding until the current pictures are decoded.

----End

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Contents

7 Video Encoder 7-1
7.1 Introduction 7-1
7.2 VEDU 7-1
7.2.1 Overview 7-1
7.2.2 Features 7-1
7.2.3 Function Description 7-2
7.3 JPGE 7-4
7.3.1 Overview 7-4
7.3.2 Features 7-4
7.3.3 Function Description 7-5

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Figures

Figure 7-1 Encoding function block diagram of the VEDU 7-3

Figure 7-2 Decoding function block diagram of the VEDU 7-4

Figure 7-3 Functional block diagram of the JPGE 7-6

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7 Video Encoder

7.1 Introduction

The video codec consists of the video encoding/decoding unit (VEDU) and JPEG encoder (JPGE). The VEDU supports H.264 encoding and decoding, and the JPGE supports JPEG encoding.

7.2 VEDU

7.2.1 Overview

The VEDU is a codec that supports H.264 protocol and performs encoding by using hardware. It features low CPU usage, low bus bandwidth, low delay, and low power consumption.

7.2.2 Features

The VEDU has the following features

- Supports ITU-T H.264 main profile/baseline profile@ level 4.1 encoding.
  - Motion compensation with 1/2 or 1/4 pixel precision
  - Four subblock types of 16x16, 16x8, 8x16, and 8x8
  - Prediction modes of intra 4x4 and intra 16x16
  - Trans4x4
  - Context-based adaptive binary arithmetic coding (CABAC) and context-based adaptive variable-length coding (CAVLC) entropy encoding
  - De-blocking filtering
  - IPCM encoding
- Supports multiple input picture formats:
  - Semi-planar YCbCr4:2:0
  - Semi-planar YCbCr4:2:2
- Supports 1x960H decoding and the the maximum encoding performance of 8x960H+8x480x240
- Supports configurable picture resolutions.
  - Minimum picture resolution: 160x64

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  - Maximum picture resolution: 1920x2048
  - Step of the picture width or height: 4
- Supports region of interest (ROI) encoding.
  - A maximum of eight ROIs
  - ROI encoding control
- Supports on-screen display (OSD) encoding protection.

  OSD encoding protection control
- Supports OSD front-end overlaying.
  - OSD overlaying before encoding for a maximum of eight regions
  - OSD overlaying at the maximum picture size anywhere
  - 129-level alpha blending
  - OSD overlaying control
- Supports constant bit rate (CBR) mode and variable bit rate (VBR) mode.
- Supports the output bit rate ranging from 32 kbit/s to 40 Mbit/s.

The Hi3521 VEDU can decode only the streams encoded by the VEDU.

7.2.3 Function Description

Figure 7-1 shows the encoding functional block diagram of the VEDU.

Based on related protocols and algorithms, the VEDU supports motion estimation, inter-prediction, intra-prediction, motion vector prediction, transform/quantization, inverse transform/inverse quantization, variable length code (VLC) encoding, stream generation, and de-blocking filtering. The video firmware (FMW) controls the bit rate and handles interrupts.

Before the VEDU is enabled for video encoding, the software allocates three types of buffers for the VEDU in the external DDR SDRAM:

- Input picture buffer

  The VEDU reads the source pictures to be encoded from this buffer during encoding. This buffer is generally written by the VICAP module.
- Reconstruction/reference picture buffer

  The VEDU writes reconstruction pictures to this buffer during encoding. These reconstruction pictures are used as the reference pictures of subsequent pictures. During the encoding of P frames, reference pictures are read from this buffer.
- Stream buffer

  This buffer stores encoded streams. The VEDU writes streams to this buffer during encoding. This buffer is read by software.

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Figure 7-1 Encoding function block diagram of the VEDU

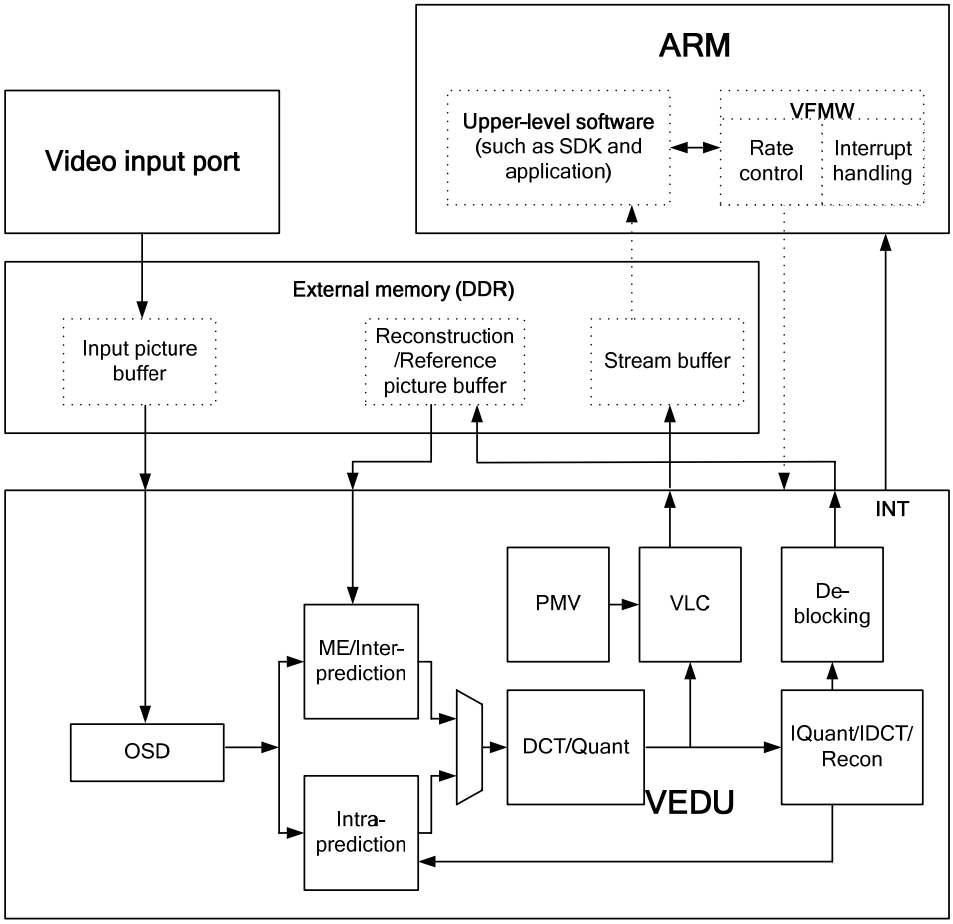

Figure 7-2 shows the decoding functional block diagram of the VEDU.

The VEDU decodes H.264 streams by slice. To be specific, the VFMW decodes the slice header and the streams before the slice header, and the VEDU hardware decodes the slice data and the streams after the slice data.

Before the VEDU starts encoding, the software allocates three types of buffers for the VEDU in the external DDR SDRAM:

- Reconstruction/Reference picture buffer

  The VEDU writes reconstruction pictures to this buffer during encoding. These reconstruction pictures are used as the reference pictures of subsequent pictures to be decoded. When P frames are being decoded, reference pictures are read from this buffer.
- Stream buffer

  This buffer stores the streams to be decoded. These streams are from the start code detect (SCD) module.
- Downlink information buffer

  This buffer stores the streams to be decoded and the streams before the slice data.

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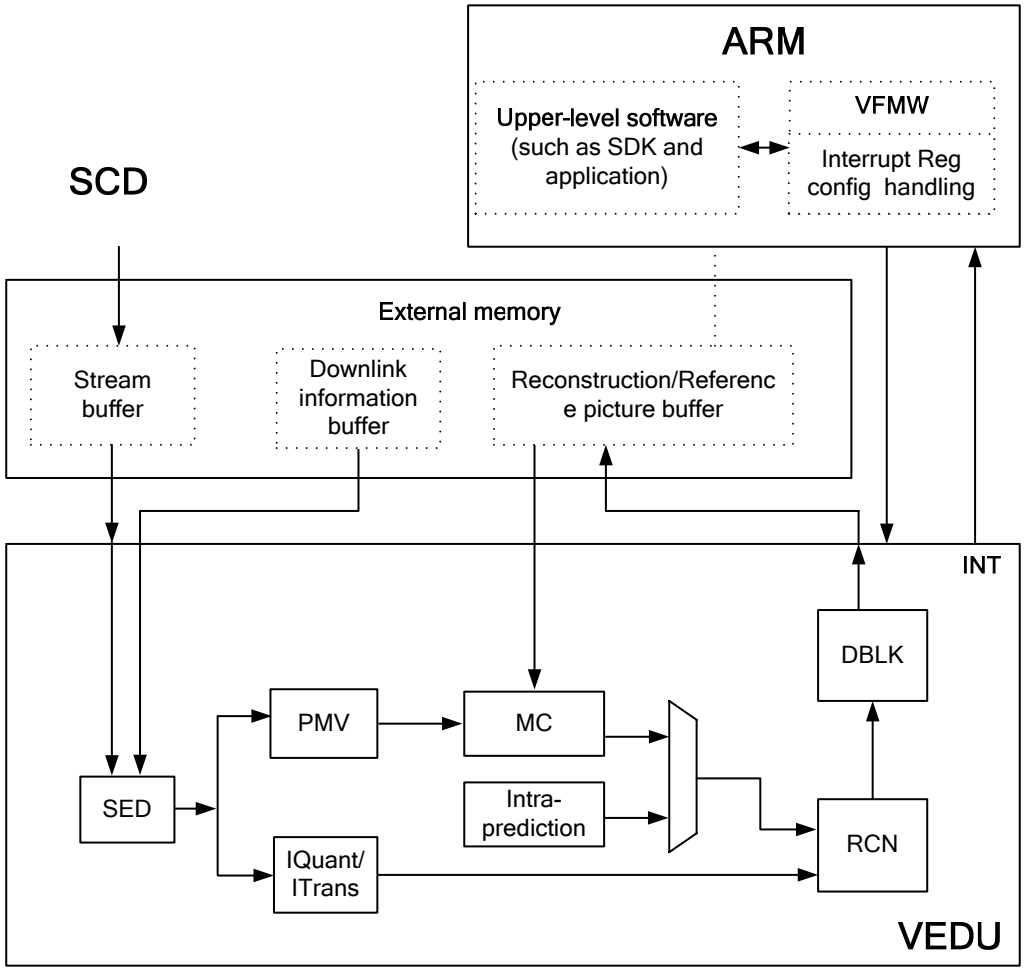
Figure 7-2 Decoding function block diagram of the VEDU



7.3 JPGE

7.3.1 Overview

The JPGE provides high-performance encoding performance by using hardware. It supports 67.1-megapixel snapshot or HD MJPEG encoding.

7.3.2 Features

The JPGE has the following features:

- Supports ISO/IEC 10918-1 (CCITT T.81) baseline process (DCT sequential) encoding.
- Encodes the pictures in the chrominance sampling format of YCbCr4:2:0, YCbCr4:2:2, or YCbCr4:4:4.
- Supports the microprogrammed control unit (MCU) using the interleaved sequence.
- Supports multiple input picture formats.
  - Planar YCbCr4:2:0

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  - Planar YCbCr4:2:2
  - Planar YCbCr4:4:4
  - Semi-planar YCbCr4:2:0
  - Semi-planar YCbCr4:2:2
  - Package YUYV
- Supports at most 67.1-megapixel/s (8192x8192).
- Supports configurable picture resolutions.
  - Minimum picture resolution: 64x64
  - Maximum picture resolution: 8192x8192
- Supports the picture width or height step of 4.
- Supports configurable quantization tables.

  An independent quantization table for the Y component, Cb component, and Cr component respectively
- Supports OSD front-end overlaying.
  - OSD overlaying before encoding for a maximum of eight regions
  - OSD overlapping with the maximum size of the source picture and within the picture position range
  - 129-level alpha blending
  - OSD overlaying control

7.3.3 Function Description

Figure 7-3 shows the functional block diagram of the JPGE.

Based on the protocols that require a large number of operands, the JPGE supports OSD, level shift, discrete cosine transform (DCT), quantization, scanning, VLC encoding, and stream generation. The VFMW configures quantization tables and handles interrupts.

Before the JPGE is enabled for video encoding, the software allocates two types of buffers for the JPGE in the external DDR SDRAM:

- Input picture buffer

  The JPGE reads the source pictures to be encoded from this buffer during encoding. This buffer is generally written by the VICAP module.
- Stream buffer

  This buffer stores encoded streams. The JPGE writes streams to this buffer during encoding. This buffer is read by software.

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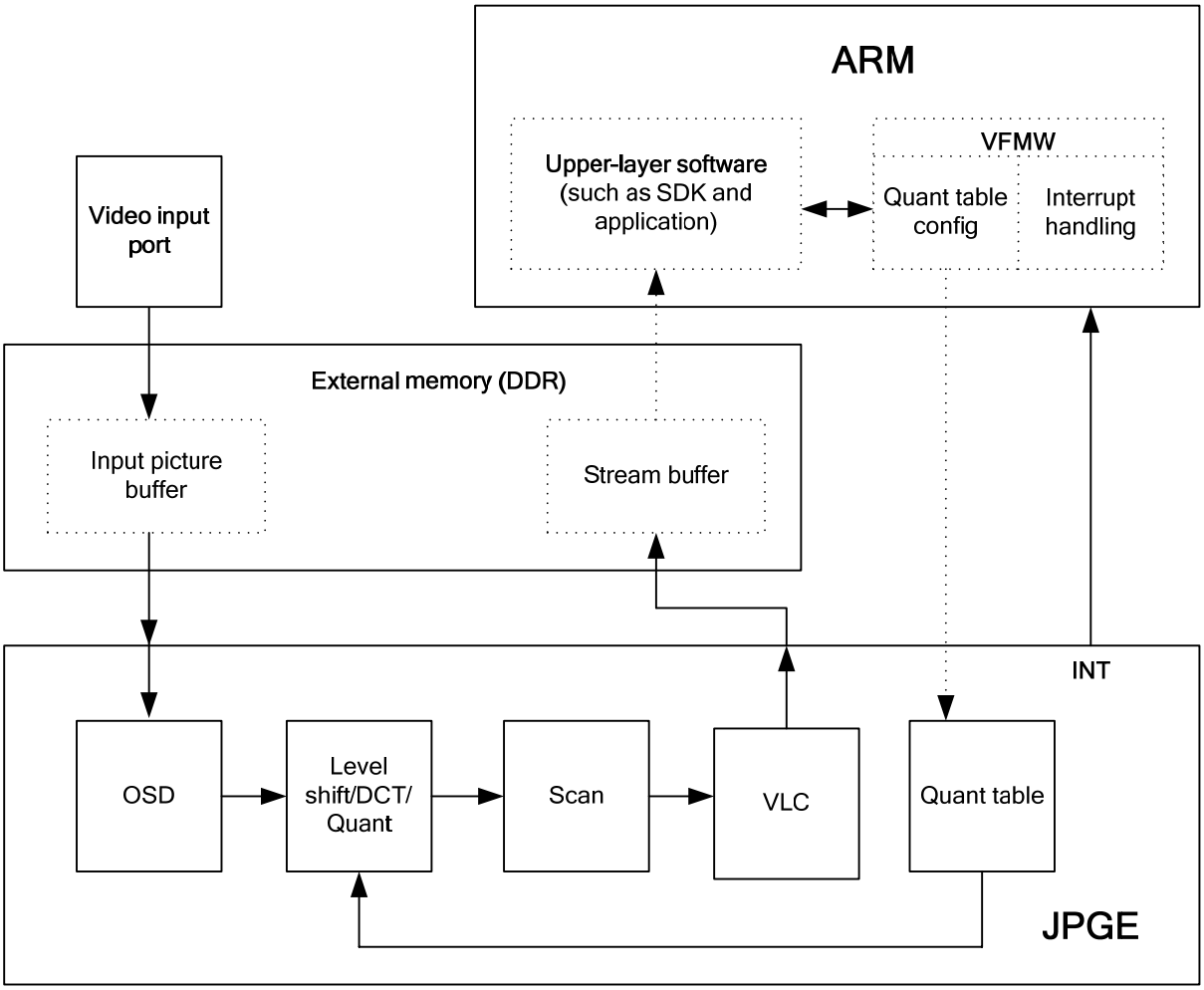
Figure 7-3 Functional block diagram of the JPGE



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Contents

8 Video and Graphics Processing 8-1
8.1 TDE 8-1
8.1.1 Overview 8-1
8.1.2 Function Description 8-1
8.2 VPSS 8-2
8.2.1 Overview 8-2
8.2.2 Features 8-2
8.3 VCMP 8-3
8.3.1 Overview 8-3
8.3.2 Features 8-3
8.3.3 Register Configuration Limitations 8-4

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8 Video and Graphics Processing

8.1 TDE

8.1.1 Overview

The two-dimensional engine (TDE) draws graphics using hardware. This significantly reduces the CPU usage and improves the utilization of the memory bandwidth. The TDE reads and writes the information about the bitmap data, filtering/scaling coefficients, parameters of linked list nodes, and linked list over the advanced eXtensible bus (AXI) master interface. By using the advanced peripheral bus (AHB) interface, the TDE obtains the CPU register configuration information.

The graphics data interface includes two channels: source channel 1 and source channel 2. Their functions are as follows:

- Source channel 1 implements direct copy and direct filling during a single-source operation.
- Source channel 2 implements complicated functions such as scaling and anti-flicker during a single-source operation.
- Source channel 1 works with source channel 2 to implement color blending and raster operations (ROPs) and process the images in microblock format.

8.1.2 Function Description

The TDE has the following features:

- Source bitmap 1 supports the formats of RGB444, RGB555, RGB565, RGB888, ARGB4444, ARGB1555, ARGB8565, ARGB8888, CLUT1, CLUT2, CLUT4, CLUT8, ACLUT44, ACLUT88, A1, A8, YCbCr888, AYCbCr8888, YCbCr422, byte, halfword, YCbCr400MB, YCbCr422MBH, YCbCr422MBV, YCbCr420MB, and YCbCr444MB.
  Source bitmap 2 supports the formats of RGB444, RGB555, RGB565, RGB888, ARGB4444, ARGB1555, ARGB8565, ARGB8888, CLUT1, CLUT2, CLUT4, CLUT8, ACLUT44, ACLUT88, A1, A8, YCbCr888, AYCbCr8888, YCbCr422, YCbCr400MB, YCbCr422MBH, YCbCr422MBV, YCbCr420MB, and YCbCr444MB.
- The output bitmap supports the formats of RGB444, RGB555, RGB565, RGB888, ARGB4444, ARGB1555, ARGB8565, ARGB8888, CLUT1, CLUT2, CLUT4, CLUT8, ACLUT44, ACLUT88, A1, A8, YCbCr888, AYCbCr8888, YCbCr422, byte, halfword, YCbCr400MB, YCbCr422MBH, YCbCr422MBV, YCbCr420MB, and YCbCr444MB.
- Supports only the little-endian system.

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- Allows the formats of source bitmap 1, source bitmap 2, and output bitmaps to be configured separately.
- Supports gamma correction and adjustable contrast and luminance.
- Supports the color look-up table (CLUT).
- Supports the conversion between RGB and YCbCr.
- Supports direct copy.
- Supports direct filling.
- Supports 2D resize.
- Supports anti-flicker.
- Supports clip.
- Supports alpha blending.
- Supports ROP.
- Supports colorkey.
- Supports programmable scanning.
- Supports clip mask.
- Supports the software interface in synchronous/asynchronous linked list mode.
- Provides status interrupts.

8.2 VPSS

8.2.1 Overview

The video processing subsystem (VPSS) implements video processing before encoding. The video processing functions includes 3D Gaussian noise adaptive reduction, image details enhancement before encoding, de-interlace, great ratio scaling, sharpening, contrast, luminance, chrominance, saturation, graphics pane processing, and block processing.

The VPSS has the following functions:

- Supports the processing of 960H video sources for a single frame.
- Supports same source preview for the encoding channel.
- Supports the simultaneous output of the major/minor streams and preview of the encoding channel.
- Supports the separate configuration function of the image border size and color.
- Supports 1080i/1080p processing by block.
- Supports register linked list configuration.
- Supports the span of 4 KB boundary.
- Supports input/output data formats of YUV420 and YUV422 (conversion from YUV420 to YUV422 is not supported).
- Supports outstanding configuration.
- Supports the low-power mode by using clock gating for memory

8.2.2 Features

The VPSS has the following features:

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- Gaussian noise reduction: The noise reduction (NR) module removes the Gaussian noise of the graphics by configuring the parameters. This makes the graphics become smooth and reduces the encoding bit rate.
- Image enhancement: The image enhancement (IE) module distinguishes the detail areas of the image and enhances the image details. In this way, the image becomes clearer and the image contrast is enhanced.
- De-interlace: The de-interlace (DEI) module restores the interlaced video source to the progressive video source.
- Image sharpening: The LTI and CTI modules extract high-frequency components from pictures before scaling and compensate frequencies for the pictures processed by the scaler. In this way, pictures have sharp edges and clear contours.
- Adjustment of image contrast, luminance, saturation, and color bar.
- Image border addition: Borders can be added to image edges. The widths and color of an image border can be set separately.
- Image processing by block: When the width of an image in a frame is greater than 960, the image is processed by block. In this mode, the maximum width is ∞ in theory.
- Scaling: Low-frequency filtering is supported even though the input and output resolutions are different.

8.3 VCMP

8.3.1 Overview

The video compress (VCMP) module compresses image data based on the graphics bandwidth compression algorithm. The video display (VDP) module reads, decompresses, and displays the compressed streams to reduce the usage of the system bandwidth. Over the AXI master interface, the VCMP module reads the bitmap data and writes compressed streams. Over the AHB slave interface, the VCMP module reads the CPU register configuration information.

The graphics data interface includes one read channel and four write channels. Their functions are as follows:

- The read channel reads the image data to be compressed from the DDR.
- The write channels write the compressed streams to the DDR to A, R, G, and B channels respectively.

8.3.2 Features

The VCMP module has the following features:

- Supports ARGB1555 and ARGB8888 image data to be compressed.
- Stores the compressed streams by A, R, G, and B components in different addresses.
- Supports the variable-length code compression algorithm.
- Supports the data amount output of compressed four components, in the unit of byte.
- Supports direct transfer that acts as a self test mode.
- Provides task completion interrupts.

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8.3.3 Register Configuration Limitations

Note the following limitations when configuring VCMP registers:

- All the working registers of the VCMP module can be configured only when the VCMP module reports interrupts. That is, when the VCMP module is working, the corresponding registers cannot be configured.
- The start address (SRC_ADDR) and stride (SRC_STRIDE) of an image to be compressed support 128-bit alignment.
- The strides and writeback addresses VCMP_A_ADDR, VCMP_R_ADDR, VCMP_G_ADDR, and VCMP_B_ADDR corresponding to compressed A, R, G, and B components support 128-bit alignment.
- The writeback width of the compressed data must be an integral multiple of 256 minus 1, for example, 255, 511, 767, or 1023. In addition, the width must be less than or equal to the writeback stride of the compressed data.

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Contents

9 Motion Detect Unit 9-1
9.1 Overview 9-1
9.2 Function Description 9-1
9.3 Operating Mode 9-1
9.3.1 Software and Hardware for Motion Detection 9-1
9.3.2 Software and Hardware for Video Occlusion Detection 9-2
9.4 Register Summary 9-2
9.5 Register Description 9-3

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Tables

Table 9-1 Summary of the MDU registers (base address: 0x206C_0000) 9-2

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9 Motion Detect Unit

9.1 Overview

As a high-performance hardware acceleration intellectual property (IP), the motion detect unit (MDU) is used to detect the motion status and video occlusion, implement modeling on the video background, and calculate the information about the object (OBJ) region. The OBJ region is a rectangular motion part of the current frame. By using the advanced eXtensible interface (AXI) master bus, the MDU reads picture information, and writes the updated information about the background, sum of absolute differences (SADs), and OBJ regions. By using the slave advanced high-performance bus (APB), the MDU obtains register configurations.

9.2 Function Description

The MDU provides the following features:

- Calculates and outputs the SAD in the unit of 8x8 or 16x16.
- Detects OBJ regions and outputs the information about the OBJ regions.
- Refreshes the background.

9.3 Operating Mode

9.3.1 Software and Hardware for Motion Detection

The software performs the following operations for the pictures to be encoded:

- Allocates the storage space in the double-data rate (DDR).
- Calls the hardware to capture videos or perform scaling.
- Schedules multiple motion detection operations, specifies and divides the regions to be detected, and generates addresses.

The hardware calculates the SADs of input pictures. The details are as follows:

- Detects OBJ regions based on the SAD and threshold, and refreshes the background.

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- Outputs the information about OBJ regions, background, and SADs based on the settings of the software.

9.3.2 Software and Hardware for Video Occlusion Detection

Based on the size of OBJ regions output by the hardware, the software checks whether the occlusion threshold is reached. If the threshold is reached, the background is forbidden to refresh, but motion detection is still performed. When the size of OBJ regions is greater than the occlusion threshold, an occlusion alarm is generated.

9.4 Register Summary

Table 9-1 describes the MDU registers.

Table 9-1 Summary of the MDU registers (base address: 0x206C_0000)

Offset Address	Register	Description	Page
0x0000	MDU_INTSTAT	Interrupt status register	9-3
0x0004	MDU_INTEN	Interrupt enable register	9-4
0x0008	MDU_RAWINT	Raw interrupt register	9-5
0x000C	MDU_INTCLR	Interrupt clear register	9-5
0x0020	MDU_VEDIMGSIZE	Picture size configuration register	9-6
0x0024	MDU_MODE	Mode configuration register	9-7
0x0028	MDU_START	MDU start register	9-8
0x002C	MDU_AXI_OUTSTD_NUM	AXI outstanding configuration register	9-8
0x0040	MDU_REF_YADDR	Luminance storage address register of the reference picture	9-9
0x0044	MDU_REF_YSTRIDE	Luminance stride register of the reference picture	9-9
0x0048	MDU_CUR_YADDR	Luminance storage address register of the current picture	9-10
0x004C	MDU_CUR_YSTRIDE	Luminance stride register of the current picture	9-10
0x0060	MDU_MBSAD_ADDR	Macroblock SAD storage address register	9-11
0x0064	MDU_MBSAD_STRIDE	Macroblock SAD storage stride register	9-11
0x0070	MDU_BACKGROUND_ADDR	Luminance storage address register of the background	9-12

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Offset Address	Register	Description	Page
0x0074	MDU_BACKGROUND_STRIDE	Luminance stride register of the background	9-12
0x0078	MDU_OBJ_ADDR	OBJ region storage address register	9-12
0x007C	MDU_BG_UP_WEIGHT	Background refresh weight register	9-13
0x0080	MDU_MBSAD_TH	Macroblock motion detection threshold register	9-14
0x0084	MDU_TIMEOUT	Timeout upper limit register	9-14
0x0090	MDU_WND_SIZE	SAD output window configuration register	9-14
0x0094	MDU_MIN_OBJ_SIZE	Minimum window configuration register for boundary search	9-15
0x0098	MDU_MAX_OBJ_CNT	Maximum window configuration register for boundary search	9-16
0x009C	MDU_OBJ_CNT	OBJ region information readback register	9-16
0x00A0	MDU_MAX_OBJ_SIZE	Maximum OBJ region readback register	9-16
0x00A4	MDU_TOTAL_OBJ_SIZE	All OBJ region information readback register	9-17
0x00A8	MDU_MOVE_PIX_CNT	Motion pixel statistics register for an entire frame	9-18
0x00AC	MDU_OBJ_CNT1	OBJ region information readback register based on the background	9-18
0x00B0	MDU_MAX_OBJ_SIZE1	Maximum OBJ region readback register based on the background	9-18
0x00B4	MDU_TOTAL_OBJ_SIZE1	All OBJ region information readback register based on the background	9-19
0x00B8	MDU_MOVE_PIX_CNT1	Motion pixel statistics register for an entire frame based on the background	9-19

9.5 Register Description

MDU_INTSTAT

MDU_INTSTAT is an interrupt status register.

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Offset Address	Register Name	Total Reset Value
0x0000	MDU_INTSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_bus_err	mdu_cfg_err	reserved																												mdu_timeout	mdu_endofpic
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	mdu_bus_err	Bus read/write error.
[30]	RO	mdu_cfg_err	Register configuration error.
[29:2]	RO	reserved	Reserved.
[1]	RO	mdu_timeout	MDU timeout interrupt. This interrupt is valid when the timeout detection mode of the MDU is enabled and the working cycle of the MDU is greater than the threshold configured by MDU_TIMEOUT.
[0]	RO	mdu_endofpic	End of picture indicator of the MDU, active high.

MDU_INTEN

MDU_INTEN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0004	MDU_INTEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_bus_err_en	mdu_cfg_err_en	reserved																												mdu_timeout_en	mdu_endofpic_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	mdu_bus_err_en	BUS read/write error interrupt enable. 0: disabled 1: enabled

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[30]	RW	mdu_cfg_err_en	Register configuration error interrupt enable. 0: disabled 1: enabled
[29:2]	RO	reserved	Reserved.
[1]	RW	mdu_timeout_en	MDU timeout interrupt enable. When the timeout detection mode of the MDU is enabled and the working cycle of the MDU is greater than the threshold configured by MDU_TIMEOUT, this interrupt is valid. 0: disabled 1: enabled
[0]	RW	mdu_endofpic_en	End of picture interrupt enable of the MDU 0: disabled 1: enabled

MDU_RAWINT

MDU_RAWINT is a raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x0008	MDU_RAWINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_bus_err_raw	mdu_cfg_err_raw	reserved																												mdu_timeout_raw	mdu_endofpic_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	mdu_bus_err_raw	Raw bus read/write error interrupt, active high.
[30]	RO	mdu_cfg_err_raw	Raw register configuration error interrupt, active high.
[29:2]	RO	reserved	Reserved.
[1]	RO	mdu_timeout_raw	Raw MDU timeout interrupt, active high.
[0]	RO	mdu_endofpic_raw	Raw end of picture interrupt of the MDU, active high.

MDU_INTCLR

MDU_INTCLR is an interrupt clear register.

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Offset Address	Register Name	Total Reset Value
0x000C	MDU_INTCLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_bus_err_clr	mdu_cfg_err_clr	reserved																												mdu_timeout_clr	mdu_endofpic_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	mdu_bus_err_clr	Bus read/write error clear, active high.
[30]	RW	mdu_cfg_err_clr	Register configuration error clear, active high.
[29:2]	RO	reserved	Reserved.
[1]	RW	mdu_timeout_clr	MDU timeout interrupt clear. When the timeout detection mode of the MDU is enabled and the working cycle of the MDU is greater than the threshold configured by MDU_TIMEOUT, this interrupt is valid.
[0]	RW	mdu_endofpic_clr	End of picture indicator clear of the MDU, active high.

MDU_VEDIMGSIZE

MDU_VEDIMGSIZE is a picture size configuration register.

Offset Address	Register Name	Total Reset Value
0x0020	MDU_VEDIMGSIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				imgheightinpixelsminus1												reserved				imgwidthinpixelsminus1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	imgheightinpixelsminus1	Picture height. The value is in the unit of pixel, and the configured value is obtained by subtracting 1 from the actual height. For example, if the picture height is 352 pixels, this field must be set to 351 pixels.
[15:13]	RO	reserved	Reserved.

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[12:0]	RW	imgwidthinpixelsminus1	Picture width. The value is in the unit of pixel, and the configured value is obtained by subtracting 1 from the actual width. For example, if the picture width is 288 pixels, this field must be set to 287 pixels.

MDU_MODE

MDU_MODE is a mode configuration register.

Offset Address	Register Name	Total Reset Value
0x0024	MDU_MODE	0x0000_019C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							mcpi_clkgate_en	mcpi_wrlock_en	timeout_en	md_mod	bg_update_en	eg_find_en	obj_out_en	sad_out_en	sad_mad_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved.
[8]	RW	mcpi_clkgate_en	Clock gating enable.
[7]	RW	mcpi_wrlock_en	Register configuration lock enable. If this field is enabled, registers cannot be configured even if the MDU is started until the detection ends. This avoids modifications made to registers.
[6]	RW	timeout_en	MDU timeout detection enable. If this field is enabled, the upper limits of the working cycle that is configured using MDU_TIMEOUT by the software can be automatically queried. 0: disabled 1: enabled
[5]	RW	md_mod	Motion detection mode. 0: background algorithm 1: frame reference algorithm
[4]	RW	bg_update_en	Background refresh enable. 0: disabled 1: enabled This field is valid only when md_mod is set to 0 (background algorithm).

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[3]	RW	eg_find_en	Joint detection enable for OBJ regions. 0: disabled 1: enabled If the background algorithm is selected, only the last joint detection based on the background is disabled.
[2]	RW	obj_out_en	OBJ region output enable. If this field is enabled, MDU_OBJ_ADDR must be configured. 0: disabled 1: enabled
[1]	RW	sad_out_en	SAD output enable. If this field is enabled, MDU_MBSAD_ADDR and MDU_MBSAD_STRIDE must be configured. 0: disabled 1: enabled
[0]	RW	sad_mad_sel	Number of SAD output bits. 0: 8 bits 1: 16 bits

MDU_START

MDU_START is an MDU start register.

Offset Address	Register Name	Total Reset Value
0x0028	MDU_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mdu_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	WO	mdu_start	MDU start control. 0: The MDU does not work. 1: The MDU is started.

MDU_AXI_OUTSTD_NUM

MDU_AXI_OUTSTD_NUM is an AXI outstanding configuration register.

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Offset Address	Register Name	Total Reset Value
0x002C	MDU_AXI_OUTSTD_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														axi_outstd_num	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2:0]	RW	axi_outstd_num	AXI outstanding configuration. The count value is numbered from 0 and the actual value is obtained by adding 1 to the count value.

MDU_REF_YADDR

MDU_REF_YADDR is a luminance storage address register of the reference picture.

Offset Address	Register Name	Total Reset Value
0x0040	MDU_REF_YADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_ref_yaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mdu_ref_yaddr	Storage address of the Y component of the reference picture. The input raw picture must be Qword-aligned (128 bits). That is, the lower four bits of the address are 0. The hardware automatically sets the lower four bits of the address to 0.

MDU_REF_YSTRIDE

MDU_REF_YSTRIDE is a luminance stride register of the reference picture.

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Offset Address	Register Name	Total Reset Value
0x0044	MDU_REF_YSTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mdu_ref_ystride																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	mdu_ref_ystride	Luminance stride, in bytes. The lower four bits of Ystride must be set to 0. This is to ensure that the address is 128-bit-aligned after the picture is wrapped. The hardware automatically sets the lower four bits of Ystride to 0. The stride must be an integral multiple of 64 bytes.

MDU_CUR_YADDR

MDU_CUR_YADDR is a luminance storage address register of the current picture.

Offset Address	Register Name	Total Reset Value
0x0048	MDU_CUR_YADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_cur_yaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mdu_cur_yaddr	Storage address of the Y component of the raw picture. The input raw picture must be Qword-aligned (128 bits). That is, the lower four bits of the address are 0. The hardware automatically sets the lower four bits of the address to 0.

MDU_CUR_YSTRIDE

MDU_CUR_YSTRIDE is a luminance stride register of the current picture.

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Offset Address	Register Name	Total Reset Value
0x004C	MDU_CUR_YSTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mdu_cur_ystride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	mdu_cur_ystride	Luminance stride, in bytes. The lower four bits of Ystride must be set to 0. This is to ensure that the address is 128-bit-aligned after the picture is wrapped. The hardware automatically sets the lower four bits of Ystride to 0. The stride must be an integral multiple of 64 bytes.

MDU_MBSAD_ADDR

MDU_MBSAD_ADDR is a macroblock SAD storage address register.

Offset Address	Register Name	Total Reset Value
0x0060	MDU_MBSAD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_mbsad_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mdu_mbsad_addr	Address for storing the macroblock SAD. The address must be Qword-aligned. Therefore, the lower four bits must be 0.

MDU_MBSAD_STRIDE

MDU_MBSAD_STRIDE is a macroblock SAD storage stride register.

Offset Address	Register Name	Total Reset Value
0x0064	MDU_MBSAD_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mdu_mbsad_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.

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[15:0]	RW	mdu_mbsad_stride	Macroblock SAD stride, in bytes. The stride must be 128-bit-aligned. Therefore, the lower four bits must be 0.

MDU_BACKGROUND_ADDR

MDU_BACKGROUND_ADDR is a luminance storage address register of the background.

Offset Address	Register Name	Total Reset Value
0x0070	MDU_BACKGROUND_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bg_yaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	bg_yaddr	Background address. The address must be Qword-aligned. Therefore, the lower four bits must be 0.

MDU_BACKGROUND_STRIDE

MDU_BACKGROUND_STRIDE is a luminance stride register of the background.

Offset Address	Register Name	Total Reset Value
0x0074	MDU_BACKGROUND_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																bg_ystride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	bg_ystride	Background stride, in bytes. The stride must be 128-bit-aligned. Therefore, the lower four bits must be 0.

MDU_OBJ_ADDR

MDU_OBJ_ADDR is an OBJ region storage address register.

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Offset Address	Register Name	Total Reset Value
0x0078	MDU_OBJ_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	obj_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	obj_addr	Address for storing OBJ regions. The address must be Qword-aligned. Therefore, the lower four bits must be 0. An OBJ region is stored as follows: The coordinates of the left, top, right, and bottom points of the OBJ region are stored in sequence in four 16-bit spaces. Therefore, two 32-bit DDRs are used to store an OBJ region. When the DDR is allocated by using the software, the minimum DDR size is calculated as follows: 2 x 32 bits x Maximum number of OBJ regions

MDU_BG_UP_WEIGHT

MDU_BG_UP_WEIGHT is a background refresh weight register.

Offset Address	Register Name	Total Reset Value
0x007C	MDU_BG_UP_WEIGHT	0x0000_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																src_weight								weight_sum_exp_2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:8]	RW	src_weight	New picture weight.
[7:0]	RW	weight_sum_exp_2	Exponent of 2 to the weighted sum. When the MDU generates a new background by overlaying the source picture with the existing background, the following formula is used: (Background pixel x ((1<<weight_sum_exp_2) – src_weight) + Pixel of source picture x bg_weight) >> weight_sum_exp_2) The background weight bg_weight is calculated as follows: ((1<<weight_sum_exp_2) – src_weight) The greater the value obtained from background weight bg_weight minus source weight src_weight, the more slowly the background is refreshed. The default value is 0x1, and the maximum value is 0x8.

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MDU_MBSAD_TH

MDU_MBSAD_TH is a macroblock motion detection threshold register.

Offset Address	Register Name	Total Reset Value
0x0080	MDU_MBSAD_TH	0x0000_001E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mdu_mbsad_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	mdu_mbsad_th	Threshold for detecting the motion status of the 4x4 macroblock. All calculations of the MDU are based on the 4x4 macroblock.

MDU_TIMEOUT

MDU_TIMEOUT is a timeout upper limit register.

Offset Address	Register Name	Total Reset Value
0x0084	MDU_TIMEOUT	0x0360_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_timeout																															
Reset	0	0	0	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mdu_timeout	Maximum number of working cycles.

MDU_WND_SIZE

MDU_WND_SIZE is a SAD output window configuration register.

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Offset Address	Register Name	Total Reset Value
0x0090	MDU_WND_SIZE	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															sad_wnd_size
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	sad_wnd_size	Size of the SAD output window. The calculations of the MDU are based on the 4x4 macroblock. After the sad_out_en bit of the mode register is enabled, the MDU adds the values of multiple 4x4 macroblocks based on the settings of sad_wnd_size, and outputs the value to the DDR. 0: 8x8 1: 16x16 (default)

MDU_MIN_OBJ_SIZE

MDU_MIN_OBJ_SIZE is the minimum window configuration register for boundary search.

Offset Address	Register Name	Total Reset Value
0x0094	MDU_MIN_OBJ_SIZE	0x0300_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	egsearch_timeout																min_obj_size_h								min_obj_size_w							
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	egsearch_timeout	Boundary search timeout. If the number of points of an OBJ region is greater than the value, the boundary search of the OBJ region stops, and the search for the next region starts.
[15:8]	RW	min_obj_size_h	Minimum height of the OBJ region. The OBJ region whose height is smaller than this value is not reported. The value 1 of min_obj_size_h indicates a 4x4 macroblock.
[7:0]	RW	min_obj_size_w	Minimum width of the OBJ region. The OBJ region whose width is smaller than this value is not reported. The value 1 of min_obj_size_w indicates a 4x4 macroblock.

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MDU_MAX_OBJ_CNT

MDU_MAX_OBJ_CNT is the maximum window configuration register for boundary search.

Offset Address	Register Name	Total Reset Value
0x0098	MDU_MAX_OBJ_CNT	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																max_obj_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	max_obj_cnt	Maximum value for detecting the OBJ regions.

MDU_OBJ_CNT

MDU_OBJ_CNT is an OBJ region information readback register.

Offset Address	Register Name	Total Reset Value
0x009C	MDU_OBJ_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_index																obj_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	max_obj_index	Maximum OBJ region index. For the statistics register whose name does not contain the digital suffix, the statistics are obtained when the SAD is calculated and the OBJ region is searched for the first time based on the frame reference algorithm or background algorithm.
[15:0]	RO	obj_cnt	Number of detected OBJ regions.

MDU_MAX_OBJ_SIZE

MDU_MAX_OBJ_SIZE is a maximum OBJ region readback register.

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Offset Address	Register Name	Total Reset Value
0x00A0	MDU_MAX_OBJ_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_size																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	max_obj_size	Maximum size of the OBJ region. This value is used to detect video occlusion. The value is in the unit of pixel. The software calculates the percentage of OBJ regions based on this value and compares the value with the size threshold of the OBJ region. If the value is greater than the threshold, the frame occlusion is considered, and the subsequent frames for detecting video occlusion are not used to refresh the background. In addition, the system checks whether the size of the OBJ region is greater than the threshold for consecutive times. If the occlusion time is greater than the time threshold, video occlusion is considered, and an alarm is generated.

MDU_TOTAL_OBJ_SIZE

MDU_TOTAL_OBJ_SIZE is an all OBJ region information readback register.

Offset Address	Register Name	Total Reset Value
0x00A4	MDU_TOTAL_OBJ_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	total_obj_size																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	total_obj_size	Total size of all OBJ regions. This value is used to detect whether a camera is sprayed. The working principle is the same as that of the max_obj_size field. The MDU adds the sizes of all OBJ regions. The size is in the unit of pixel. The size of each OBJ region is calculated as follows: number of 4x4 macroblocks x 16 **NOTE** • In some cases, the OBJ regions may overlap, and the total size of OBJ regions may be greater than the size of the original picture. • Based on the 4x4 macroblock, the height and width of each OBJ region are calculated as follows: Width = (Horizontal coordinate of the right point – Horizontal coordinate of the left point) + 1 Height = (Vertical coordinate of the bottom point – Vertical coordinate of the top point) + 1

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MDU_MOVE_PIX_CNT

MDU_MOVE_PIX_CNT is a motion pixel statistics register for an entire frame.

Offset Address	Register Name	Total Reset Value
0x00A8	MDU_MOVE_PIX_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	move_pix_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	move_pix_cnt	Number of motion pixels of an entire frame. This value can be used to detect video occlusion. The working principle is the same as that of the max_obj_size field. Note: The value of this register is based on pixels. Therefore, the register value may be different from the value of total_obj_size.

MDU_OBJ_CNT1

MDU_OBJ_CNT1 is an OBJ region information readback register based on the background.

Offset Address	Register Name	Total Reset Value
0x00AC	MDU_OBJ_CNT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_index1																obj_cnt1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	max_obj_index1	Index of the maximum OBJ region based on the background. The registers with the suffix 1 indicate statistics registers. The statistics are obtained when the background algorithm is used and the SAD is calculated and the OBJ region is searched for the second time.
[15:0]	RO	obj_cnt1	Number of detected OBJ regions based on the background.

MDU_MAX_OBJ_SIZE1

MDU_MAX_OBJ_SIZE1 is a maximum OBJ region readback register based on the background.

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Offset Address	Register Name	Total Reset Value
0x00B0	MDU_MAX_OBJ_SIZE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_size1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	max_obj_size1	Maximum size of the OBJ region based on the background. This value is used to detect video occlusion, and is in the unit of pixel. The software calculates the percentage of OBJ regions based on this value and compares the value with the size threshold of the OBJ region. If the value is greater than the threshold, the frame occlusion is considered, and the subsequent frames for detecting video occlusion are not used to refresh the background. In addition, the system checks whether the size of the OBJ region is greater than the threshold for consecutive times. If the occlusion time is greater than the time threshold, video occlusion is considered, and an alarm is generated.

MDU_TOTAL_OBJ_SIZE1

MDU_TOTAL_OBJ_SIZE1 is a all OBJ region information readback register based on the background.

Offset Address	Register Name	Total Reset Value
0x00B4	MDU_TOTAL_OBJ_SIZE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	total_obj_size1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	total_obj_size1	Sum of the sizes of all OBJ regions based on the background. This value is used to detect whether a camera is sprayed. The working principle is the same as that of the max_obj_size field.

MDU_MOVE_PIX_CNT1

MDU_MOVE_PIX_CNT1 is a motion pixel statistics register for an entire frame based on the background.

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Offset Address	Register Name	Total Reset Value
0x00B8	MDU_MOVE_PIX_CNT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	move_pix_cnt1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	move_pix_cnt1	Number of motion pixels of an entire frame based on the background. This value can be used to detect video occlusion. The working principle is the same as that of the max_obj_size field.

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Contents

10 Intelligent Video Engine 10-4
10.1 Overview 10-4
10.2 Features 10-4
10.3 Operating Mode 10-5
10.3.1 Hardware Usage 10-5
10.3.2 Interrupt 10-9
10.3.3 Clock Reset 10-9
10.3.4 Input and Output Data Formats 10-10
10.4 Register Summary 10-25
10.5 Register Description 10-25

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Figures

Figure 10-1 Structure of a linked list node of the IVE 10-6
Figure 10-2 Schematic diagram of the IVE linked list 10-9
Figure 10-3 Storage of pixels in the memory when the data format is SemPlanar YCbCr422 10-10
Figure 10-4 Storage of pixels in the memory when the data format is SemPlanar YCbCr420 10-10
Figure 10-5 Storage of pixels in the memory when the data format is gray image 10-11
Figure 10-6 Storage of pixels in the memory when the data format is RGB package 10-11
Figure 10-7 Storage of pixels in the memory when the data format is RGB planar 10-12
Figure 10-8 Storage of output results in the memory for the sobel operator 10-13
Figure 10-9 Storage of results in the memory for the canny operator 10-13
Figure 10-10 Storage of output results in the memory for the integral operator (INTEGRAL_OUT) 10-14
Figure 10-11 Storage of output results in the memory for the histogram operator (HIST_OUT) 10-14
Figure 10-12 Mod operation when the stride of the operator uses the minimum value 10-15
Figure 10-13 Application of DMA data transfer (1) 10-16
Figure 10-14 Computation formula for 3x3 template filter 10-16
Figure 10-15 Sobel calculation formulas 10-19
Figure 10-16 Definition of canny angle quantization 10-20
Figure 10-17 Formula for calculating the 3x3 dilate operator 10-21
Figure 10-18 Formula for calculating the 3x3 erode operator 10-21

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Tables

Table 10-1 Parameters of the IVE linked list node 10-6
Table 10-2 Video matrix of the conversion from YCbCr to RGB (BT.601) 10-17
Table 10-3 Video matrix of the conversion from YCbCr to RGB (BT.709) 10-18
Table 10-4 Image matrix of the conversion from YCbCr to RGB (BT.601) 10-18
Table 10-5 Image matrix of the conversion from YCbCr to RGB (BT.709) 10-18
Table 10-6 Summary of IVE registers (base address: 0x205E_0000) 10-25

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10 Intelligent Video Engine

10.1 Overview

The intelligent video engine (IVE) is a hardware acceleration module in the intelligent analysis system. It implements various functions such as template filter, dilate, erode, image sobel and canny edge extraction, subtract, AND, and OR of images, thresh, integral and histogram statistics. The IVE reads and writes data and linked list node parameters through the AXI Master bus interface. It configures the registers required for the IVE startup and obtains the register status information during IVE running through the APB Slave bus interface.

10.2 Features

The IVE has the following features:

- Supports the DMA.
- Supports 3x3 template filter.
- Supports color space conversion (CSC) from YUV to RGB.
- Supports the compound function of 3x3 template filter + CSC from YUV to RGB.
- Supports gradient computation of operators (such as sobel and scharr) in X/Y direction.
- Supports the computation of canny gradient magnitude and direction.
- Supports 3x3 erode.
- Supports 3x3 dilate.
- Supports image thresh.
- Supports the AND operation of two images.
- Supports subtract of two images.
- Supports the OR operation of two images.
- Supports integral computation.
- Supports histogram statistics.
- Supports a maximum running frequency of 300 MHz.
- Supports independent soft reset.
- Supports 64-bit AXI Master bus and 32-bit APB Slave bus.
- Supports linked list interrupts and node interrupts.

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- Supports the query mode.
- Supports gray images in input formats such as SP420 (semi-planar420) and SP422 (semi-planar422).
- Supports gray images in output formats such as SP420, SP422, RGBpackage, and RGBplanar.
- Supports non 8-byte alignment of read/write address of some operators.

10.3 Operating Mode

10.3.1 Hardware Usage

To use the IVE in query mode, perform the following steps:

Step 1 Create task linked lists in the memory.

Step 2 Configure the internal registers LIST_POINTER and INT_EN of the IVE.

Step 3 Configure the internal register IVE_START of the IVE to start the IVE.

Step 4 Check the status of IVE_STATUS during the running to obtain the running status of the IVE. If the IVE is idle, linked list tasks are complete. To continue using the IVE, repeat Step 1 through Step 3.

----End

To use the IVE in interrupt mode, perform the following steps:

Step 1 Create task linked lists in the memory.

Step 2 Configure the internal registers LIST_POINTER and INT_EN of the IVE.

Step 3 Configure the internal register IVE_START of the IVE to start the IVE.

Step 4 In the interrupt service program, determine the interrupt type based on INT_STATUS and configure the internal register INT_RW of the IVE to clear the interrupt of INT_STATUS. Determine the status of the IVE based on IVE_STATUS. The status of IVE_STATUS is idle, indicating that linked list tasks are completed. Go back to Step 1 to start the next linked list operation.

----End

The IVE task linked list adopts the linked list node format at the fixed length and at fixed position. Each node is 8x8 bytes in size, and the number of linked list nodes can be any value.

Figure 10-1 shows the structure of a linked list node.

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Figure 10-1 Structure of a linked list node of the IVE

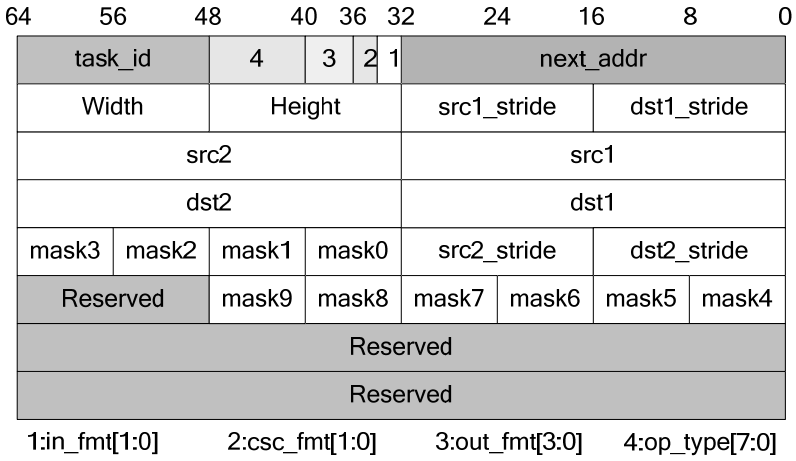

Table 10-1 describes the meanings of the parameters of the IVE linked list node.

Table 10-1 Parameters of the IVE linked list node

Parameter Register	Description
next_addr	Address of the next node in the memory. The value is 0x00000000, indicating the last node of the current linked list.
in_fmt	Input format of an image. 00: gray image 01: SP420 10: SP422 11: reserved
csc_fmt	CSC mode select. 00: BT601&BT656, ranging from 16 to 235. 01: BT701, ranging from 16 to 235. 10: BT601&BT656, ranging from 0 to 255. 11: BT701 ranging from 0 to 255.

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Parameter Register	Description
out_fmt	Output format of an image. CSC: 0000: package 0001: planar Canny: 0000: Output the amplitude only. 0001: Output the amplitude and angle. Thresh: 0000: Set the value to maxvalue when it is greater than the threshold and minvalue when it is smaller than the threshold. 0001: Set the value to maxvalue when it is greater than the threshold and retain the value when it is smaller than the threshold. 0010: Retain the value when it is greater than the threshold and set the value to minvalue when it is smaller than the threshold. Subtract: 0000: Output the absolute difference value. 0001: Move one bit right and then output the difference value.
op_type	Operator type selected by the current node. 0x00: DMA 0x01: filter 0x02: CSC 0x03: filter+CSC 0x04: sobel 0x05: canny 0x06: dilate 0x07: erode 0x08: thresh 0x09: AND 0x0A: subtract 0x0B: OR 0x0C: integral 0x0D: histogram
task_id	Task ID of the current node.
dst1_stride	Output stride signal of destination address 1. Eight bytes are aligned.
src1_stride	Stride signal of source image 1. Eight bytes are aligned.
height	Actual height of the source image.

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Parameter Register	Description
width	Actual width of the source image. When the input format is 420 or 422, the value is an even number.
src1	Start address of source image 1. For operators such as filter, CSC, filter+CSC, sobel, canny, dilate, erode, integral, and histogram, eight bytes are aligned.
src2	Start address of source image 2.
dst1	Start address of destination 1. For operators such as start address, filter, CSC, filter+CSC, sobel, canny, dilate, erode, integral, and histogram, eight bytes need to be aligned.
dst2	Start address of destination 2.
dst2_stride	Stride of destination address 2. Eight bytes need to be aligned.
src2_stride	Stride of source image 2. Eight bytes are aligned.
mask0	Template coefficient 00 or threshold of the thresh operator.
mask1	Template coefficient 01 or min_value of the thresh operator.
mask2	Template coefficient 02 or max_value of the thresh operator.
mask3	Template coefficient 10.
mask4	Template coefficient 11.
mask5	Template coefficient 12.
mask6	Template coefficient 20.
mask7	Template coefficient 21.
mask8	Template coefficient 22.
mask9	Sum of the filter operator coefficients.
reserved	Reserved bit.

NOTE

The template coefficient indicates the coefficient of the operation template used by 3x3 operators such as filter, filter+CSC, sobel, canny, dilate, and erode.

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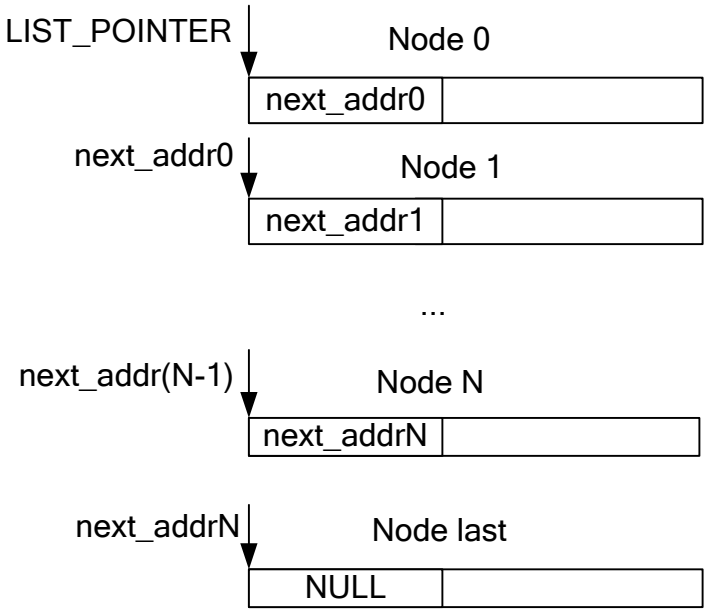
Figure 10-2 Schematic diagram of the IVE linked list



10.3.2 Interrupt

The IVE generates two types of interrupts:

- Interrupt over the completion of all nodes of the current linked list
- Interrupt over the completion of operations of the current node

10.3.3 Clock Reset

Clock Disable Policy

You can disable the input clock of the IVE to reduce the power consumption. Before disabling the IVE clock, ensure that the IVE is idle by checking the register IVE_STATUS. If IVE_STATUS[0] is 0, the IVE is idle. The configuration of the IVE register is not affected by the clock disable policy. You need to enable the clock before operating internal registers of the IVE.

Clock Reset Policy

The IVE must be reset independently at a specific time; otherwise, bus exceptions may occur. The IVE can be reset independently only when the status register IVE_STATUS of the IVE is idle.

When the system is reset, all internal registers of the IVE are cleared.

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10.3.4 Input and Output Data Formats

10.3.4.1 Storage Sequence

In the following descriptions, the data storage sequence is the storage sequence of data in the memory of the little endian system. For convenient description, word and double word are uniformly used as storage units. In actual applications, different operators have special requirements on data storage alignment formats. For details, see section 10.3.4.2 "Functions."

Figure 10-3 Storage of pixels in the memory when the data format is SemPlanar YCbCr422

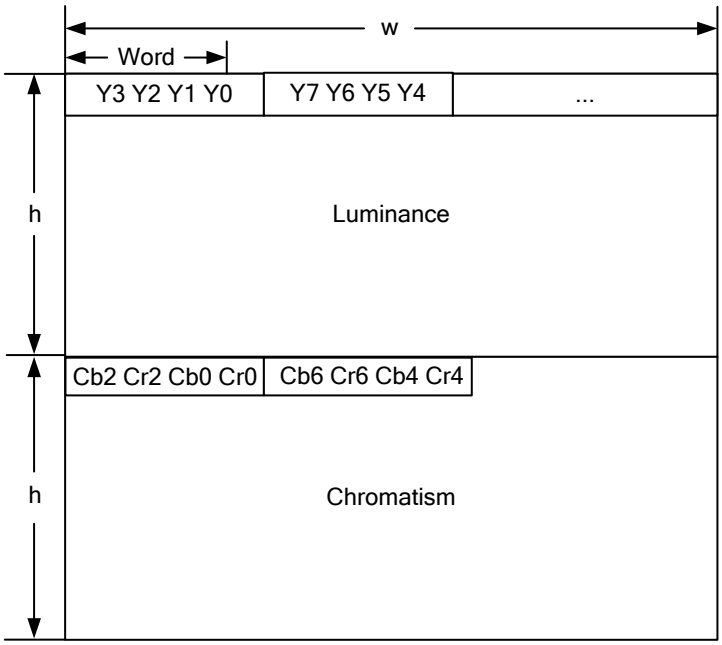

Figure 10-4 Storage of pixels in the memory when the data format is SemPlanar YCbCr420

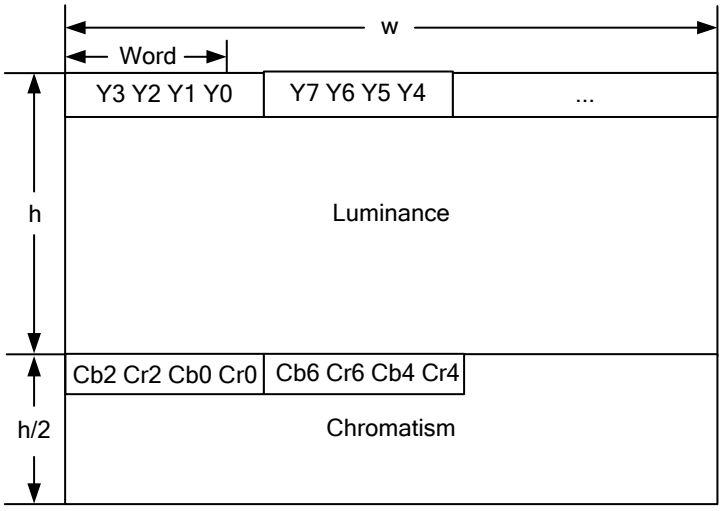

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Figure 10-5 Storage of pixels in the memory when the data format is gray image

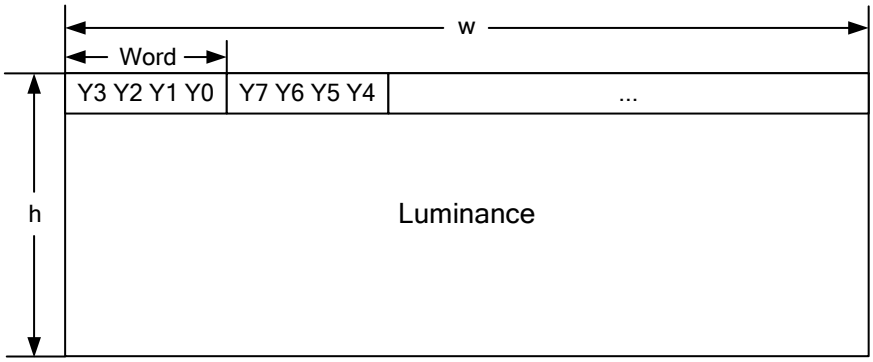

Figure 10-6 Storage of pixels in the memory when the data format is RGB package

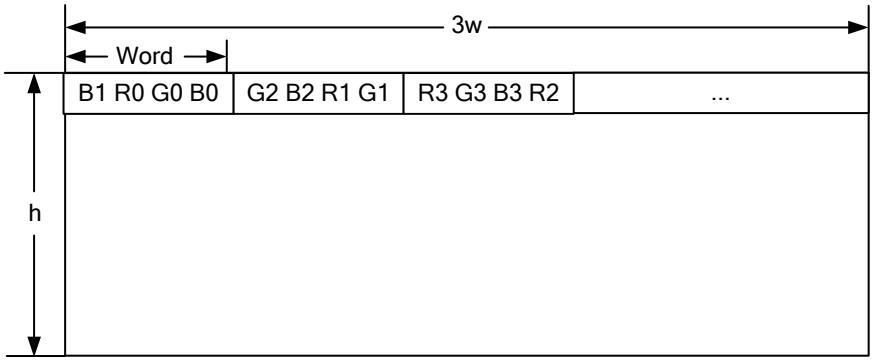

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Figure 10-7 Storage of pixels in the memory when the data format is RGB planar

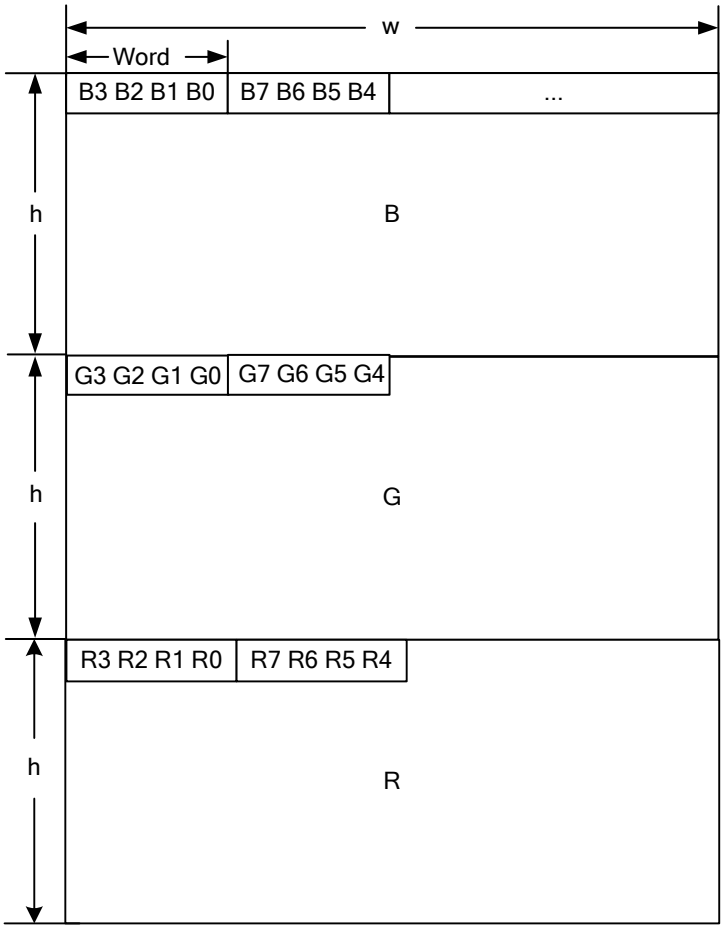

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Figure 10-8 Storage of output results in the memory for the sobel operator

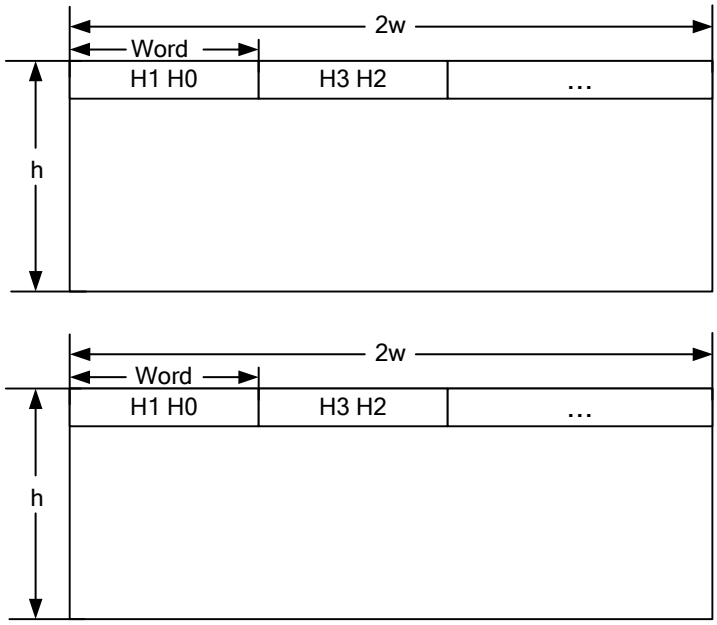

Figure 10-9 Storage of results in the memory for the canny operator

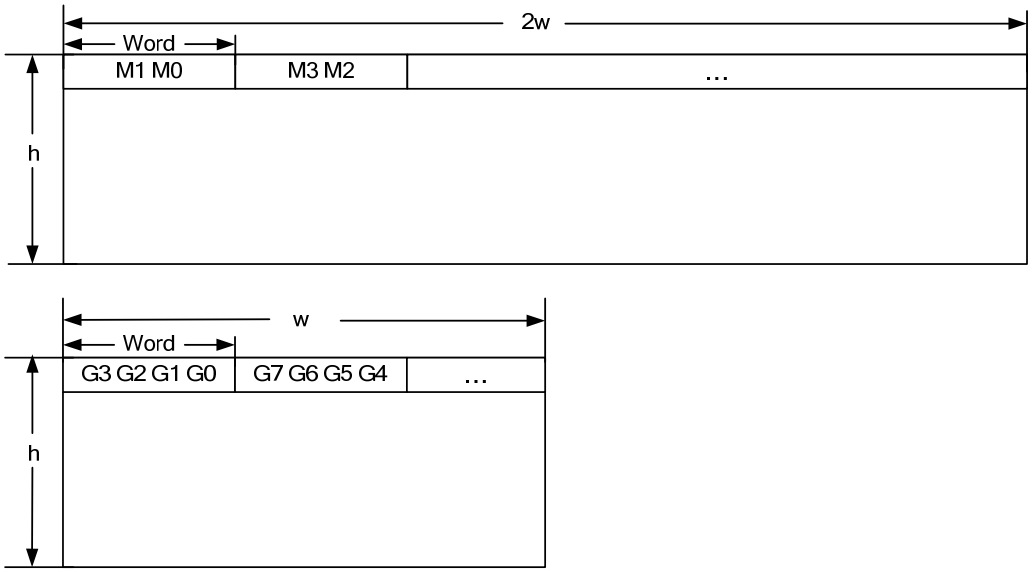

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Figure 10-10 Storage of output results in the memory for the integral operator (INTEGRAL_OUT)

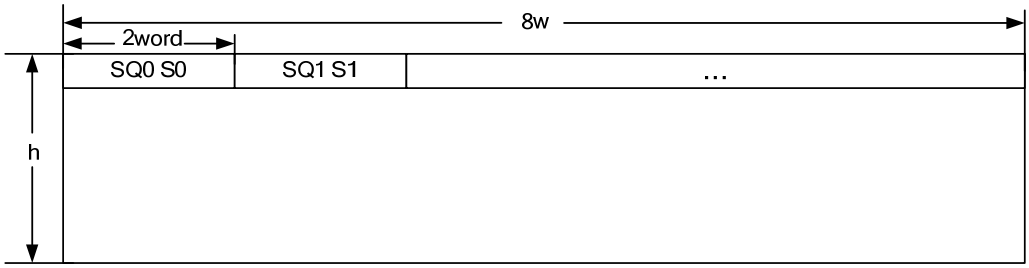
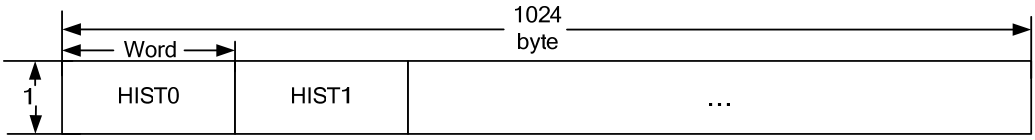


Figure 10-11 Storage of output results in the memory for the histogram operator (HIST_OUT)



10.3.4.2 Functions

The stride of all operators of the IVE needs to meet the following conditions:

When $((src\%8) == 0) \,\&\, \&((width\%8) == 0)$:

$$\begin{cases} stride \geq width \\ stride\%8 = 0 \end{cases}$$

Else:

$$\begin{cases} \{(8 - ((width + (src\%8))\%8)) + (src\%8) + width\} \leq stride \\ stride\%8 = 0 \end{cases}$$

% indicates the mod operation. See Figure 10-12.

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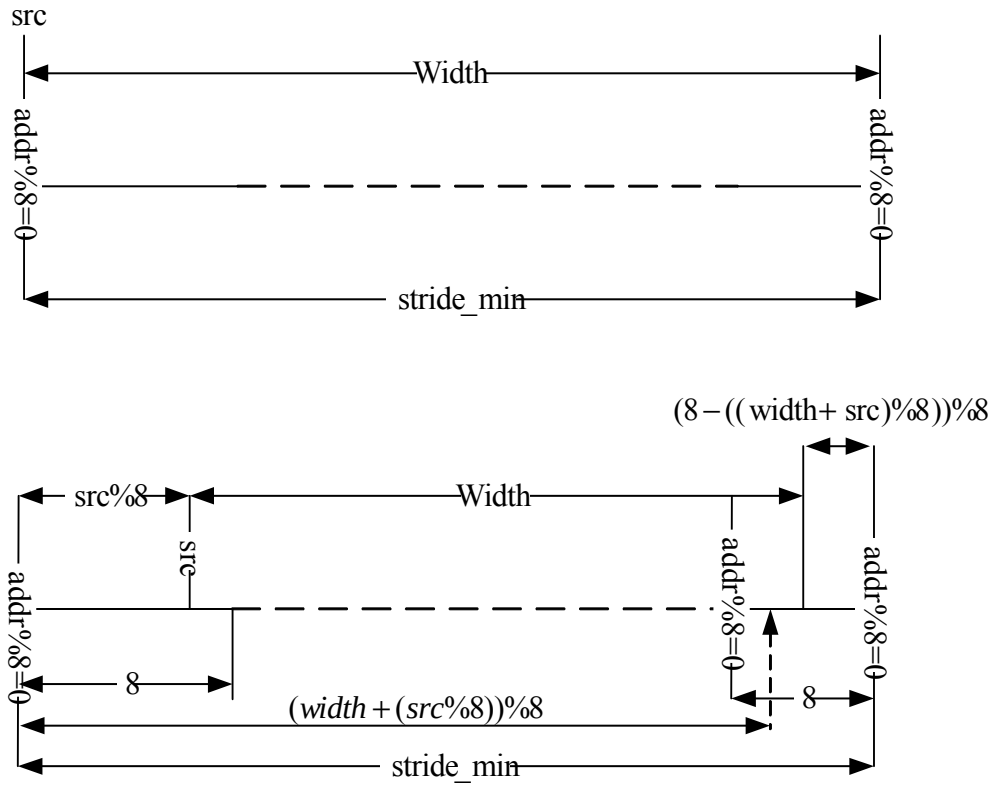
Figure 10-12 Mod operation when the stride of the operator uses the minimum value



DMA

DMA is used to fast transfer data from the rectangular image area. In DMA mode, source data is directly transferred to the target area to overwrite the data in the target area through the internal fast channel.

Image resolution: 32x1 to 1920x1080

Address alignment mode: Bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> gray image

Usage: Set op_type of the node in the linked list to 0x00.

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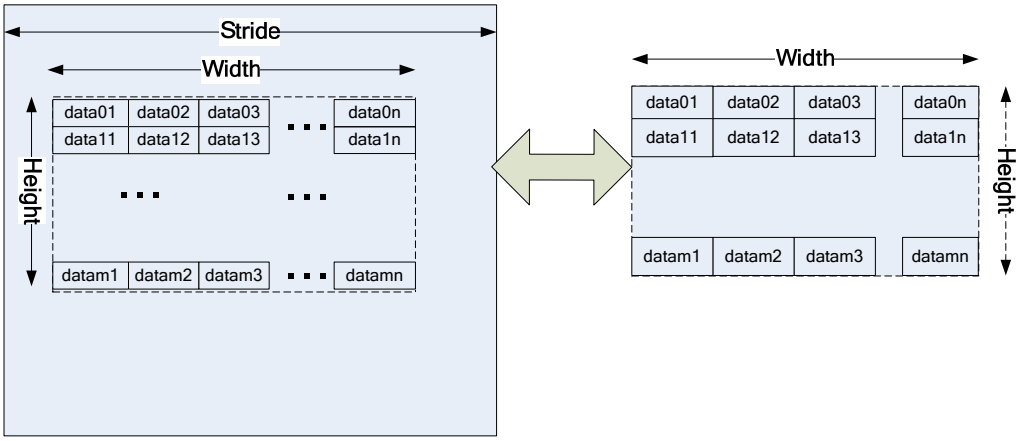
Figure 10-13 Application of DMA data transfer (1)



3×3 Template Filter

This function is used to filter a source image using a 3x3 template and then output the image.

Image resolution: 64x64 to 1920x1024

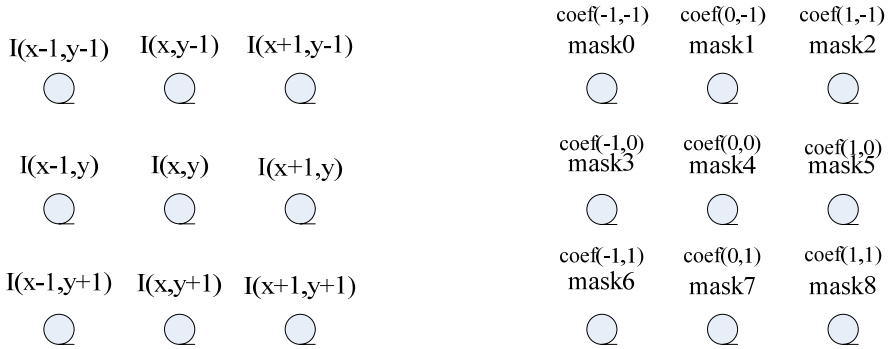
Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> gray image; SP420 -> SP420; SP422 -> SP422

Usage:

- Set op_type to 0x1.
- Set the input format.
- Set coefficients mask0−mask9. The value range of mask0–mask8 is [–128, +127], and the value range of mask9 is [0, 10].

Figure 10-14 Computation formula for 3x3 template filter



$$Iout(x,y) = \left\{ \sum_{-2<j<2} \sum_{-2<i<2} I(x+i, y+j) \bullet coef(i,j) \right\} >> mask9$$

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CSC

CSC from YUV to RGB is supported.

Image resolution: 64x64 to 1920x1080

Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

Input/output format: SP420 -> RGB package; SP420 -> RGB planar; SP422 -> RGB package; SP422 -> RGB planar

Usage:

- Set op_type of the linked list node to 0x02.
- Set in_fmt of the linked list node:
  01: 420
  10: 422
- Set out_fmt of the linked list node:
  0000: package
  0001: planar
- Set csc_fmt of the linked list node:
  00: BT601&BT656 (16–235)
  01: BT709 (16–235)
  10: BT601&BT656 (0–255)
  11: BT709 (0–255)

When csc_fmt is 0 or 1, CSC is video conversion from YUV to RGB. The output meets the following condition: 16 ≤ R, G, B ≤ 235.

When csc_fmt is 2 or 3, CSC is image conversion from YUV to RGB. The output meets the following condition: 0 ≤ R, G, B ≤ 255.

The input and output requirements for the video matrix of the conversion from YUV to RGB are as follows:

- 16 ≤ Y ≤ 235
- 16 ≤ Cb, Cr ≤ 240
- 16 ≤ R, G, B ≤ 235

Table 10-2 describes the video matrix algorithm for the conversion from YUV to RGB.

Table 10-2 Video matrix of the conversion from YCbCr to RGB (BT.601)

Method of Calculating the Floating Point for the CSC from RGB to YCbCr:									
R	=	1	×(Y)	+	0.0	×(Cb-128)	+	1.371	×(Cr-128)
G	=	1	×(Y)	–	0.336	×(Cb-128)	–	0.698	×(Cr-128)
B	=	1	×(Y)	+	1.732	×(Cb-128)	+	0.0	×(Cr-128)

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Table 10-3 Video matrix of the conversion from YCbCr to RGB (BT.709)

Method of Calculating the Floating Point for the CSC from RGB to YCbCr:									
R	=	1	×(Y)	+	0.0	×(Cb-128)	+	1.540	×(Cr-128)
G	=	1	×(Y)	–	0.183	×(Cb-128)	–	0.459	×(Cr-128)
B	=	1	×(Y)	+	1.816	×(Cb-128)	+	0.0	×(Cr-128)

The input and output requirements for the image matrix of the conversion from YUV to RGB are as follows:

- $16 \leq Y \leq 235$
- $16 \leq U, V \leq 240$
- $0 \leq R, G, B \leq 255$

Table 10-4 describes the image matrix algorithm for the conversion from YUV to RGB.

Table 10-4 Image matrix of the conversion from YCbCr to RGB (BT.601)

Method of Calculating the Floating Point for the CSC from RGB to YCbCr:									
R	=	1.164	×(Y-16)	+	0.0	×(Cb-128)	+	1.596	×(Cr-128)
G	=	1.164	×(Y-16)	–	0.391	×(Cb-128)	–	0.813	×(Cr-128)
B	=	1.164	×(Y-16)	+	2.018	×(Cb-128)	+	0.0	×(Cr-128)

Table 10-5 Image matrix of the conversion from YCbCr to RGB (BT.709)

Method of Calculating the Floating Point for the CSC from RGB to YCbCr:									
R	=	1.164	×(Y-16)	+	0.0	×(Cb-128)	+	1.793	×(Cr-128)
G	=	1.164	×(Y-16)	–	0.213	×(Cb-128)	–	0.534	×(Cr-128)
B	=	1.164	×(Y-16)	+	2.115	×(Cb-128)	+	0.0	×(Cr-128)

3x3 Template Filter + CSC

This function is used to filter a source image as 3x3 template, perform CSC, and then output the image.

Image resolution: 64x64 to 1920x1024

Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

Input/output format: SP420 -> RGB package; SP420 -> RGB planar; SP422 -> RGB package; SP422 -> RGB planar

Usage:

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- Set op_type to 0x3.
- Set the CSC coefficient.
- Set the input format and output format.
- Set coefficients mask0−mask9. The value range of mask0–mask8 is [–128, +127], and the value range of mask9 is [0, 10].

Sobel

Image resolution: 64x64 to 1920x1024

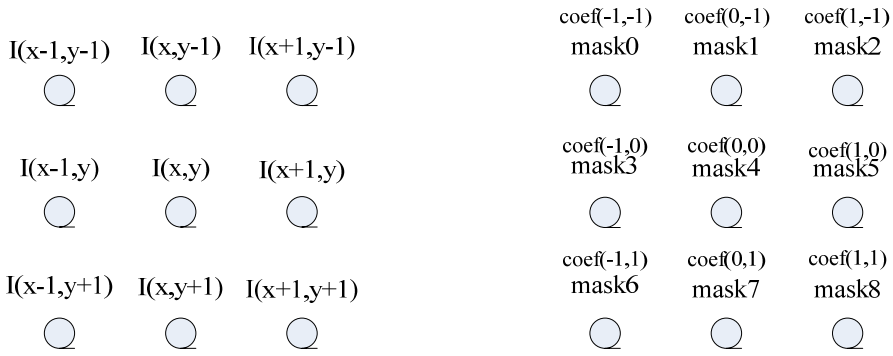
Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> SOBEL_OUT

Usage:

- Set op_type to 0x4.
- Set coefficients mask0−mask8. The value range of mask0–mask8 is [–128, +127].

Figure 10-15 Sobel calculation formulas



$$Hout(x,y)=\sum_{-2<j<2}\sum_{-2<i<2}I(x+i,y+j)\bullet coef(i,j)$$

$$Vout(x,y)=\sum_{-2<j<2}\sum_{-2<i<2}I(x+i,y+j)\bullet coef(j,i)$$

Canny

Image resolution: 64x64 to 1920x1024

Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> CANNY_OUT1; gray image -> CANNY_OUT2

Usage:

- Set op_type to 0x5.
- Set the output format.
- Set coefficients mask0−mask8. The value range of mask0–mask8 is [–128, +127].

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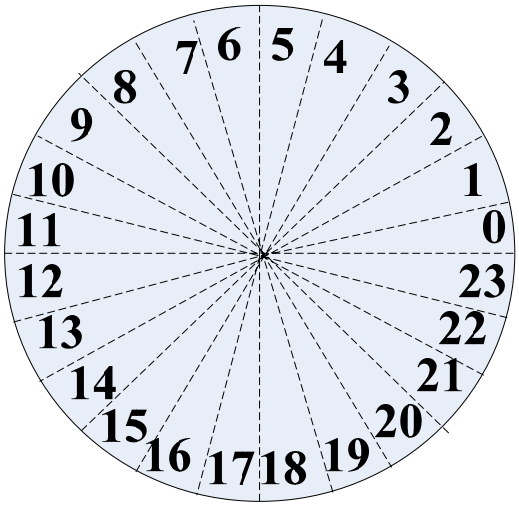
Definition of amplitude: $Mag(x, y) = abs(Hout(x, y)) + abs(Vout(x, y))$

Figure 10-16 Definition of canny angle quantization



Output angle: $\theta = \left[\frac{\arctan(\frac{V}{H}) * 12}{\pi} \right]$

3x3 Dilate

Image resolution: 64x64 to 1920x1024

Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> gray image

Usage:

- Set op_type to 0x6.
- Set coefficients mask−mask8.
- The input/output data is 0 or 255. The mask value is 0 or 255.

Figure 10-17 shows the formula for calculating the 3x3 dilate operator.

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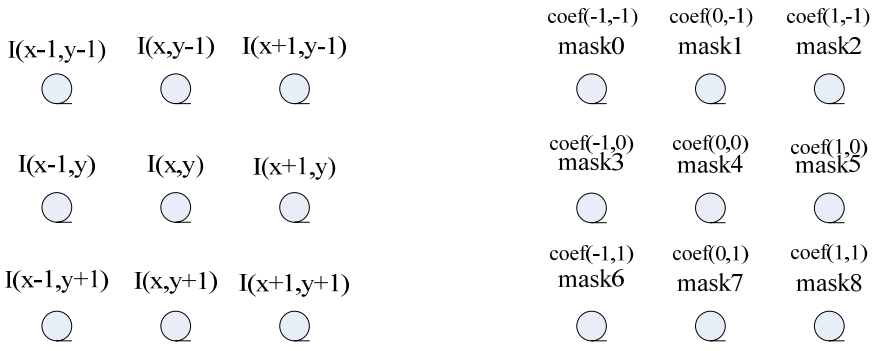
Figure 10-17 Formula for calculating the 3x3 dilate operator



$$Iout(x,y) = f(I(x+(k\,\&\,3)-1, y+(k\%3)-1)\,\&\,coef((k\,\&\,3)-1,(k\%3)-1),|,0,8)$$

$$f(A_k,\Theta,c_{\min},c_{\max}) = A_{c_{\min}}\Theta A_{c_{\min+1}}\cdots\Theta A_{c_{\max}}$$

NOTE

In the preceding formula, | indicates bitwise OR operation, & indicates bitwise AND operation, and % indicates REM operation.

3x3 Erode

Image resolution: 64x64 to 1920x1024

Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

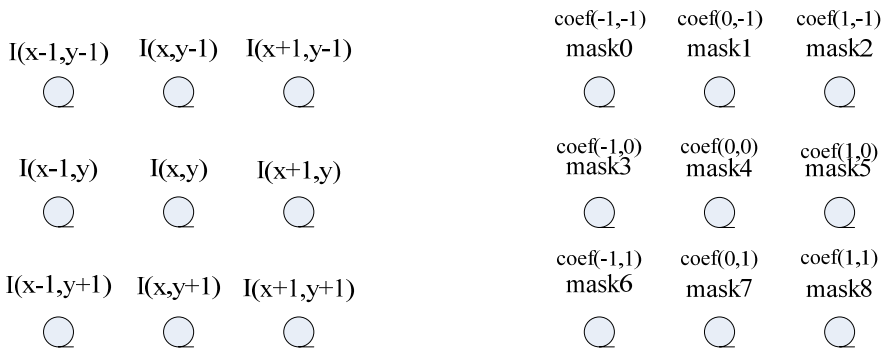
Input/output format: gray image -> gray image

Usage:

- Set op_type to 0x7.
- Set coefficients mask0−mask8.
- The input/output data is 0 or 255. The mask value is 0 or 255.

Figure 10-18 shows the formula for calculating the 3x3 erode operator.

Figure 10-18 Formula for calculating the 3x3 erode operator



$$Iout(x,y) = f(I(x+(k\,\&\,3)-1, y+(k\%3)-1)\,|\,coef((k\,\&\,3)-1,(k\%3)-1),\&,0,8)$$

$$f(A_k,\Theta,c_{\min},c_{\max}) = A_{c_{\min}}\Theta A_{c_{\min+1}}\cdots\Theta A_{c_{\max}}$$

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NOTE

In the preceding formula, | indicates bitwise OR operation, & indicates bitwise AND operation, and % indicates REM operation.

Thresh

A fixed threshold is used to perform thresh operation on an image. Three modes are supported:

- mode=2: If the pixel value is above threshold, the pixel value is unchanged. Otherwise, the pixel value is minValue.

$$I_{out}(x,y)=\begin{cases}\min Value & (I(x,y)\le threshold)\\ I(x,y) & (I(x,y)>threshold)\end{cases}$$

- mode=1: If the pixel value is above threshold, the pixel value is maxValue. Otherwise, the pixel value is unchanged.

$$I_{out}(x,y)=\begin{cases}I(x,y) & (I(x,y)\le threshold)\\ \max Value & (I(x,y)>threshold)\end{cases}$$

- mode=0: If the pixel value is above threshold, the pixel value is maxValue. Otherwise, the pixel value is minValue.

$$I_{out}(x,y)=\begin{cases}\min Value & (I(x,y)\le threshold)\\ \max Value & (I(x,y)>threshold)\end{cases}$$

Image resolution: 64x64 to 1920x1080

Address alignment mode: Bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> gray image

Usage:

- Set op_type of the linked list node to 0x08.
- Set linked list nodes mask0, mask1, and mask2 map to threshold, minValue, and maxValue respectively.

AND

CAUTION

The height and width of source image 2 must be consistent with those of source image 1. However, their stride can be different.

The AND operation is performed on the pixel value of source image 2 and source image 1, and then the data is transferred to the target area. The sizes of the two images are the same.

Image resolution: 64x64 to 1920x1080

Address alignment mode: Bytes of the input and output addresses need to be aligned.

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Input/output format: gray image -> gray image

Usage: Set op_type of the node in the linked list to 0x09.

$$I_{out}(x, y) = I_{src1}(x, y) \& I_{src2}(x, y)$$

NOTE

In the preceding formula, & indicates bitwise AND operation.

Subtract

CAUTION

The height and width of source image 2 must be consistent with those of source image 1. However, their stride can be different.

The subtract operation is performed on the pixel value of source image 2 and source image 1, and then the data is transferred to the target area. The following two working modes are provided:

0000: Output the absolute difference value, that is, $dst[i, j] = abs(src1[i, j] - src2[i, j]$

0001: Move one bit right, and then output the difference value, with the sign bit reserved, that is, $dst[i, j] = (src1[i, j] - src2[i, j]) >> 1$

For example, if the pixel value in a certain position of image 1 is 0x23, and the pixel value in the corresponding position of image 2 is 0x40, the result is 0x1D in mode 0000 or 0xF1 in mode 0001.

Image resolution: 64x64 to 1920x1080

Address alignment mode: Bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> gray image

Usage:

- Set op_type of the linked list node to 0x0a.
- Set out_fmt of the linked list node to 0x0000 or 0x0001.

OR

CAUTION

The height and width of source image 2 must be consistent with those of source image 1. However, their stride can be different.

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The OR operation is performed on the pixel value of source image 2 and source image 1, and then the data is transferred to the target area.

Image resolution: 64x64 to 1920x1080

Address alignment mode: Bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> gray image

Usage: Set op_type of the node in the linked list to 0x0b.

$$I_{out}(x,y) = I_{src1}(x,y) \mid I_{src2}(x,y)$$

NOTE

In the preceding formula, | indicates bitwise OR operation.

Integral

The output format of integral images for pixel values and for squared pixel values is 64 bytes. The integral image for pixel values occupies the lower 28 bits, and the integral image for squared pixel values occupies the upper 36 bits.

Image resolution: 64x64 to 1920x1080

Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> INTEGRAL_OUT

Usage: Set op_type of the node in the linked list to 0x0c.

$$I_{sum}(x,y) = \sum_{i\geq 0}^{i\leq x}\sum_{j\geq 0}^{j\leq y} I(i,j)$$

$$I_{sq}(x,y) = \sum_{i\geq 0}^{i\leq x}\sum_{j\geq 0}^{j\leq y} (I(i,j) \bullet I(i,j))$$

$$I_{out}(x,y) = (I_{sum}(x,y) \,\&\, 0\text{x}FFFFFFF) \mid (I_{sq}(x,y) << 28)$$

NOTE

In the preceding formulas, | indicates bitwise OR operation, & indicates bitwise AND operation, and << indicates left shift operation.

Histogram

In the 256-level histogram statistics, a gray image is input, and a 32-bit 256-level histogram statistic value is output.

Image resolution: 64x64 to 1920x1080

Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> HIST_OUT

Usage: Set op_type of the node in the linked list to 0x0d.

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$$I_{out}(x) = \sum_i \sum_j ((I(i,j) == x)?1:0) \qquad x = 0 \ldots 255$$

10.4 Register Summary

Table 10-6 describes the IVE registers.

Table 10-6 Summary of IVE registers (base address: 0x205E_0000)

Offset Address	Register	Description	Page
0x0000	IVE_START	Start register	10-25
0x0004	INT_EN	Interrupt enable register	10-26
0x0008	INT_RW	Raw interrupt register	10-26
0x000C	INT_STATUS	Interrupt status register	10-27
0x0010	LIST_POINTER	Link table start address register	10-27
0x0014	IVE_STATUS	IVE working status register	10-28
0x0018	IVE_TASK_ID	Completed task ID register	10-28

10.5 Register Description

IVE_START

IVE_START is a start register.

Offset Address	Register Name	Total Reset Value
0x0000	IVE_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								ive_start
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	WO	ive_start	IVE start signal, active high.

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INT_EN

INT_EN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0004	INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														list_int_en	node_int_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	list_int_en	Link table interrupt enable. 0: disabled 1: enabled
[0]	RW	node_int_en	Node interrupt enable. 0: disabled 1: enabled

INT_RW

INT_RW is a raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x0008	INT_RW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														list_int_rw	node_int_rw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.

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[1]	RW	list_int_rw	Link table raw interrupt. After reading an interrupt through INT_STATUS, the software writes INT_RW to clear the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RW	node_int_rw	Node raw interrupt. After reading an interrupt through INT_STATUS, the software writes INT_RW to clear the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

INT_STATUS

INT_STATUS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x000C	INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														list_int_status	node_int_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RO	list_int_status	Link table interrupt status. The software determines whether a linked list interrupt is generated by reading this bit. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	node_int_status	Node interrupt status. The software determines whether a node interrupt is generated by reading this bit. 0: No interrupt is generated. 1: An interrupt is generated.

LIST_POINTER

LIST_POINTER is a linked list start address register.

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Offset Address	Register Name	Total Reset Value
0x0010	LIST_POINTER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	link_table_header_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	link_table_header_addr	Address of the first node in the linked list.

IVE_STATUS

IVE_STATUS is an IVE working status register.

Offset Address	Register Name	Total Reset Value
0x0014	IVE_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ive_working_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	ive_working_status	Current working status of the IVE. 0: idle 1: busy

IVE_TASK_ID

IVE_TASK_ID is a completed task ID register.

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Offset Address	Register Name	Total Reset Value
0x0018	IVE_TASK_ID	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ive_task_id															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	ive_task_id	ID of a task that was just completed. If task IDs are incremental, all tasks before a specified task have been completed.

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Contents

11 Video Interfaces.....11-1
11.1 VICAP.....11-1
11.1.1 Overview.....11-1
11.1.2 Features.....11-1
11.1.3 Function Description.....11-2
11.1.4 Operating Mode.....11-13
11.1.5 Register Summary.....11-15
11.1.6 Register Description.....11-19
11.2 VDP.....11-61
11.2.1 Overview.....11-61
11.2.2 Function Description.....11-61
11.2.3 Operating Mode.....11-64

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Figures

Figure 11-1 Functional block diagram of the VICAP module 11-1
Figure 11-2 8-channel D1/960H input application 1 11-3
Figure 11-3 4-channel 720p input application 11-3
Figure 11-4 2-channel 1080p input application 11-4
Figure 11-5 Vertical timing of the 525-line 60 fields/s video system 11-6
Figure 11-6 Vertical timing of the 625-line 50 fields/s video system 11-7
Figure 11-7 Horizontal input timing of the HD interface 11-7
Figure 11-8 Vertical input timing of the HD interface 11-8
Figure 11-9 ITU-R BT.601 horizontal timing 11-8
Figure 11-10 NTSC vertical sync timing 11-9
Figure 11-11 PAL vertical sync timings 11-9
Figure 11-12 DC horizontal timing 11-10
Figure 11-13 DC vertical pulse timing 11-10
Figure 11-14 DC vertical line active timing 11-11
Figure 11-15 Relationships between the active video area and the horizontal/vertical blanking areas 11-11
Figure 11-16 YCbCr4:2:2 storage mode 11-12
Figure 11-17 Big endian and little endian storage modes 11-13
Figure 11-18 VICAP hardware workflow 11-14
Figure 11-19 Software configuration workflow 11-15
Figure 11-20 Space allocation of VICAP registers 11-16
Figure 11-21 Overall architecture of the VDP module 11-62
Figure 11-22 Format of the ITU-R BT.656 YCbCr 4:2:2 line data 11-66
Figure 11-23 Horizontal timing of the BT.1120 interface 11-67
Figure 11-24 Three sets of coordinates 11-69
Figure 11-25 Progressive decompression storage mode 11-72
Figure 11-26 Interlaced decompression storage mode 11-73

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Tables

Table 11-1 Format of the ITU-R BT.656 YCbCr 4:2:2 line data 11-5

Table 11-2 Formats of SAV and EAV 11-5

Table 11-3 Valid SAV and EAV values 11-5

Table 11-4 ITU-R BT.656 correction codes 11-6

Table 11-5 Summary of the VICAP registers (base address: 0x2058_0000) 11-16

Table 11-6 Clock configuration of DHD0 (interface clocks and data from DHD0 or DSD0/DSD1) 11-64

Table 11-7 Clock configuration of DSD0 or DSD1 11-65

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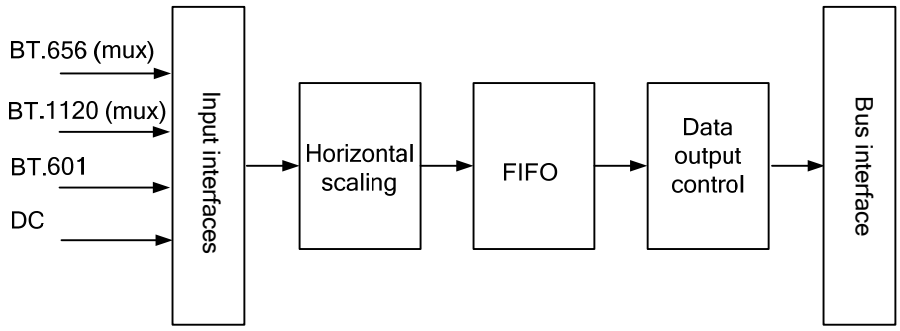
11 Video Interfaces

11.1 VICAP

11.1.1 Overview

The video capture (VICAP) module receives video data over the BT.656 interface (mux), BT.1120 (mux) interface, BT.601 interface, or digital camera (DC) interface, and stores the data in the specified addresses of the DDR. During this process, the VICAP module performs horizontal scaling on video data (or simple down sampling or scaling based on channels) and outputs multiple video streams. Figure 11-1 shows the functional block diagram of the VICAP module.

Figure 11-1 Functional block diagram of the VICAP module



11.1.2 Features

The VICAP module has the following features:

- Supports the maximum input resolution of 1920x1080.
- Supports four external BT.656 interfaces or two external BT.1120 interfaces.
- Internally supports four ports and processes 16-channel videos. Each channel supports interlaced and progressive input modes
- Supports BT.656 (mux), BT.1120 (mux), BT.601, and DC timings.
- Supports SMPTE293M/ITU-R BT.1358 timing (480p/576p), SMPTE 274M/BT.1120 timings (1080i/1080p), and SMPTE 296M timing (720p).

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- Supports horizontal scaling down at most two times (integral multiple).
- Supports configurable 2-level bus priorities for each channel.
- Obtains data in a specified window.
- Supports mirror and flip.
- Supports the output storage modes of SPYCbCr 4:2:0 and SPYCbCr 4:2:2.

11.1.3 Function Description

11.1.3.1 Typical Application

The VICAP module captures video data in multiple input timings and stores the captured data in the DDR. By using different function modes configured by the system, the VICAP module can connect to different external VI interfaces, supporting multiple external input devices.

It uses 38 pins, two clocks, four external sync signals (multiplexed with other pins), and 32 data lines. It also provides four ports and 16 channels. Each port parses the timings of a interconnected chip, and each channel processes 1-channel video signals. Each port corresponds to four channels. The four independent ports can work together in any form. The details are as follows:

- Four ports are used to connect four chips with 8-bit data lines.
- Two ports are used to connect two chips with 16-bit data lines.
- Three ports are used to connect a chip with 16-bit data lines and two chips with 8-bit data lines.

Each port can transfer 4-channel D1/960H data, 2-channel D1/960H data, 1-channel D1/960H data, 1-channel 720p data, or 1-channel 1080p data. The 1080p60 data can be transferred only by the 16-bit data line.

The VICAP module supports the following typical input modes:

- 8-channel D1/960H
- 4-channel 720p
- 2-channel 1080p

CAUTION

Each BT.1120 interface has two clocks: CLK and CLKA. If a BT.1120 interface acts as a 16-bit data input, CLK is used; if a BT.1120 interface acts two 8-bit data inputs, the upper eight bits use CLK, and the lower eight bits use CLKA.

8-Channel D1/960H

Figure 11-2 shows 8-channel D1/960H input application 1.

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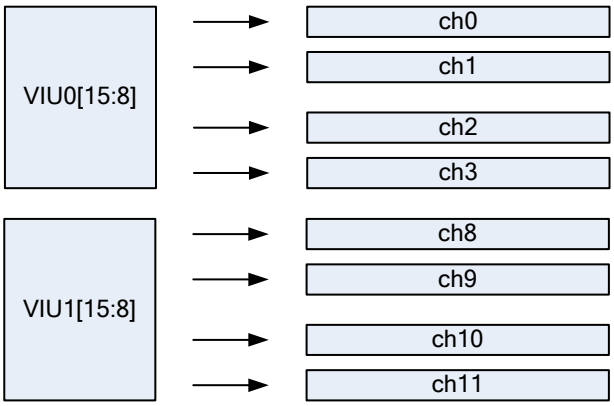
Figure 11-2 8-channel D1/960H input application 1



Each 8-bit pin transfers 4-channel time-division-multiplexing (TDM) D1/960H data. A total of 32-bit pins are used.

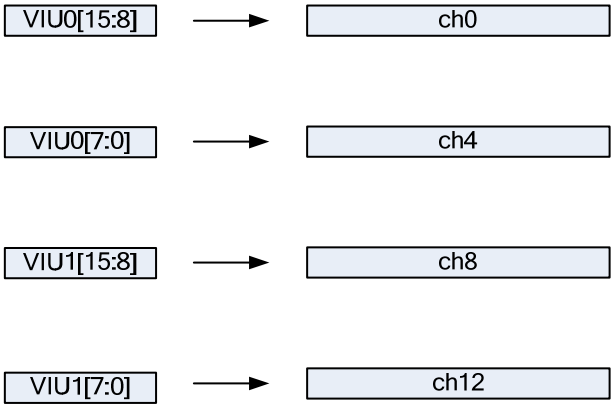
Where,

- VIU0 indicates the pin corresponding to BT.1120 interface 0.
- VIU1 indicates the pin corresponding to BT.1120 interface 1.
- [15:8] indicates bit 15 to bit 8.
- [7:0] indicates bit 7 to bit 0.
- ch0 to ch15 indicate channel 0 to channel 15 respectively.

4-Channel 720p

Figure 11-3 shows 4-channel 720p input application.

Figure 11-3 4-channel 720p input application



Each 8-bit pin transfers 1-channel 720p data. A total of 32-bit pins are used. In interleave mode, eight bits can be used to transfer data in CYCYCY sequence by using the TDM

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function, which doubles the clock frequency. In normal mode, the data is transferred over the 16-bit data line.

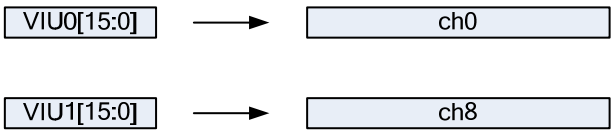
Where,

- VIU0 indicates the pin corresponding to BT.1120 interface 0.
- VIU1 indicates the pin corresponding to BT.1120 interface 1.
- [15:8] indicates bit 15 to bit 8.
- [7:0] indicates bit 7 to bit 0.
- ch0 to ch15 indicate channel 0 to channel 15 respectively.

2-Channel 1080p

Figure 11-4 shows 2-channel 1080p input application.

Figure 11-4 2-channel 1080p input application



16-bit pins are combined to form a BT.1120 interface to transfer 1-channel 1080p data. A total of 32-bit pins are used.

Where,

- VIU0 indicates the pin corresponding to BT.1120 interface 0.
- VIU1 indicates the pin corresponding to BT.1120 interface 1.
- [15:8] indicates bit 15 to bit 8.
- [7:0] indicates bit 7 to bit 0.
- ch0 to ch15 indicate channel 0 to channel 15 respectively.

Mixed Timing Input

The interconnected chips are independent of each other, and they can work together in any form.

11.1.3.2 Function Principle

ITU-R BT. 656 YCbCr4:2:2

1. Horizontal timing

Based on the ITU-R BT.656 protocol, sync signals are included in data streams. The special bytes start of active video (SAV) and end of active video (EAV) indicate the start and end of active line data respectively. In video streams, the header of the timing reference code indicates that the following byte is SAV or EAV. The timing reference code consists of FF 00 00. FF and 00 indicate the reserved bytes of the image encoding data, that is, non-image data. Table 11-1 shows the format of the ITU-R BT.656 line data.

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Table 11-1 Format of the ITU-R BT.656 YCbCr 4:2:2 line data

Timing Reference Code				Line Blanking Area					Timing Reference Code				YCbCr 4:2:2 with 720 Valid Pixels						
FF	00	00	EAV	80	10	…	80	10	FF	00	00	SAV	Cb0	Y0	Cr0	Y1	…	Cr718	Y719

The difference between SAV and EAV depends on the special bit H. Both SAV and EAV include vertical blanking bit V and field indicator bit F. Table 11-2 describes the formats of SAV and EAV.

Table 11-2 Formats of SAV and EAV

Bit7	Bit6 (F)	Bit5 (V)	Bit4 (H)	Bit[3:0] (P3–P0)
Fixed value 1	Field indicator bit 1st field: F = 0 2nd field: F = 1	Vertical blanking bit VBI: V = 1 Active video: V = 0	SAV: H = 0 EAV: H = 1	Check bits

The ITU-R BT.656 protocol defines valid SAV and EAV by using eight valid reserved bits. Four check bits are used to correct 1-bit error and detect 2-bit errors. Table 11-3 describes the valid SAV and EAV values.

Table 11-3 Valid SAV and EAV values

Code	Binary Value	Field Number	Vertical Blanking Interval or Not
SAV	10000000	1	No
EAV	10011101	1	No
SAV	10101011	1	Yes
EAV	10110110	1	Yes
SAV	11000111	2	No
EAV	11011010	2	No
SAV	11101100	2	Yes
EAV	11110001	2	Yes

The four valid reserved bits including P0, P1, P2, and P3 provide the error correction function. They are determined by the F, V, and H bits, as shown in Table 11-4.

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Table 11-4 ITU-R BT.656 correction codes

F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

NOTE

- P0 = F^V^H
- P1 = F^V
- P2 = F^H
- P3 = V^H

2. Vertical timing

The positions of the vertical timings are determined by bit F and bit V of the timing reference codes SAV and EAV. Figure 11-5 shows the vertical timing of the 525-line 60 field/s video system and Figure 11-6 shows the vertical timing of the 625-line 50 field/s video system.

Figure 11-5 Vertical timing of the 525-line 60 fields/s video system

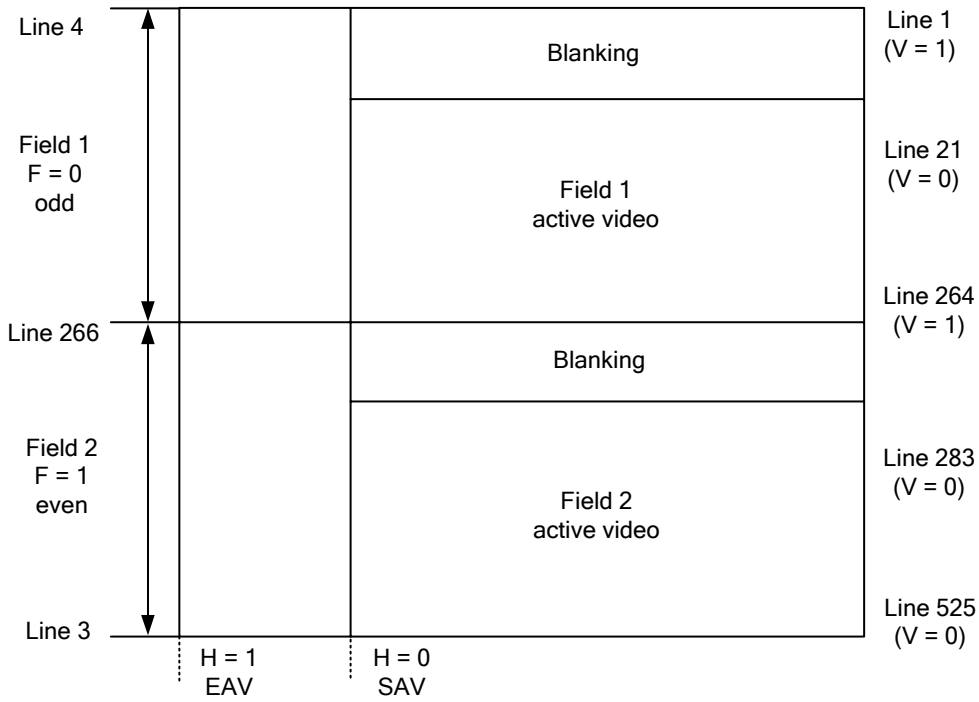

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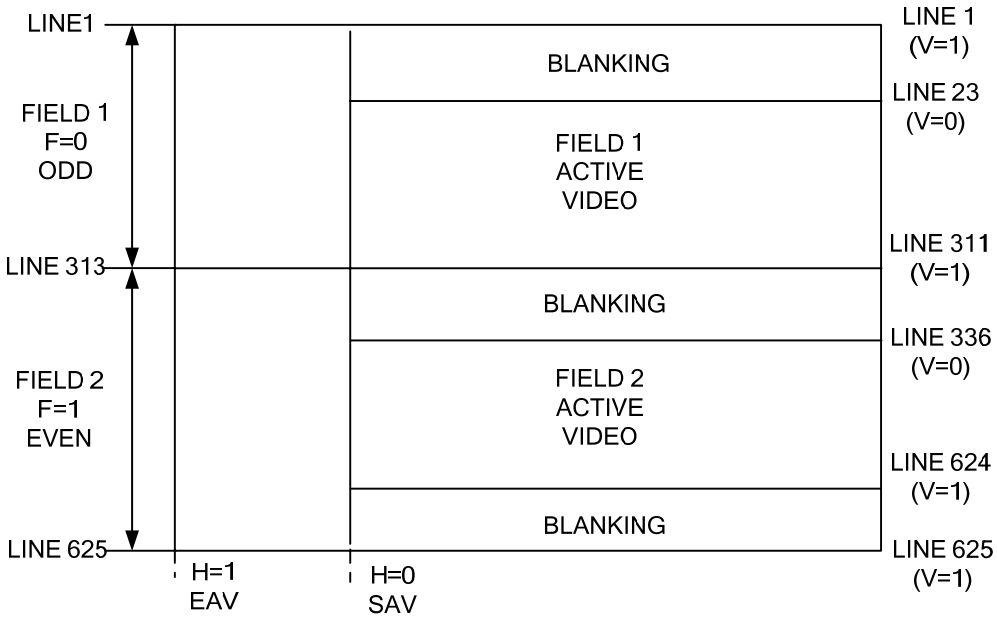
Figure 11-6 Vertical timing of the 625-line 50 fields/s video system



The VICAP module identifies vertical timings based on SAV and EAV regardless of the lines.

BT.1120 (HD) Interface Timings

The VICAP module supports the high-definition (HD) interface timings with Y/C separation inputs. In this case, two ports are required. One is used to transfer luminance and the other is used to transfer chrominance, as shown in Figure 11-7 and Figure 11-8.

Figure 11-7 Horizontal input timing of the HD interface

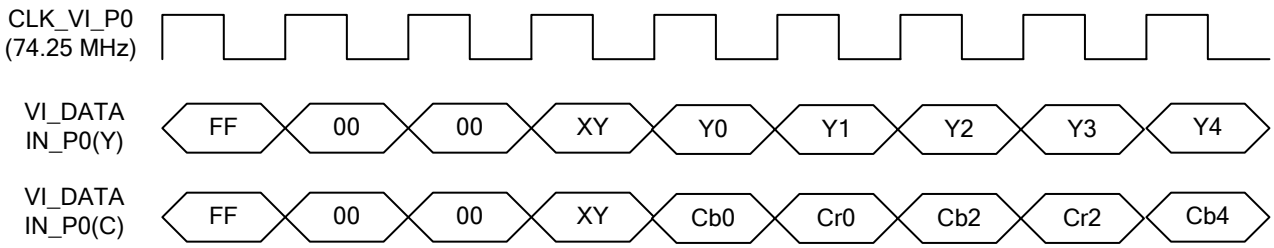


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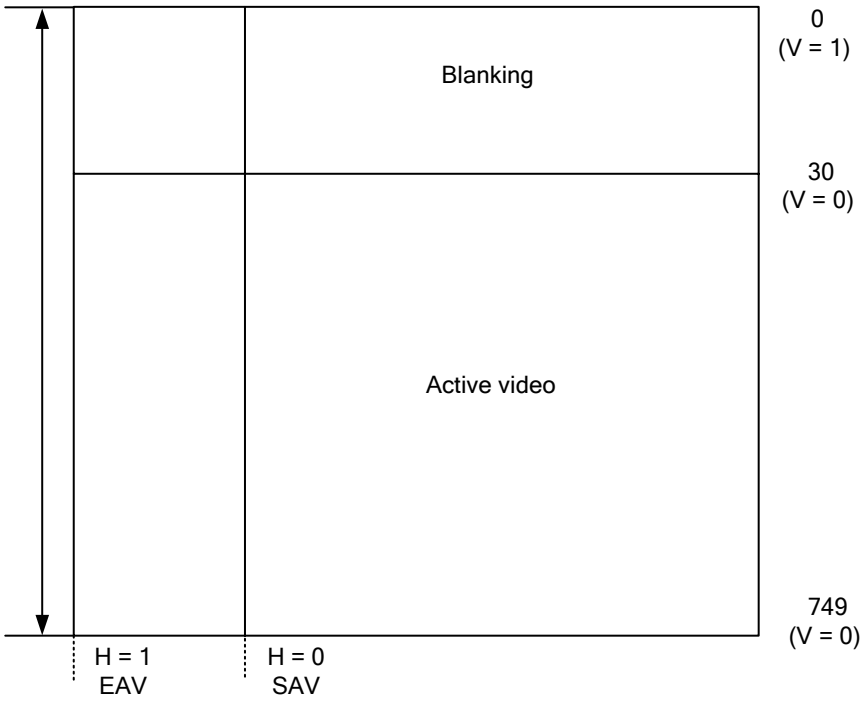
Figure 11-8 Vertical input timing of the HD interface

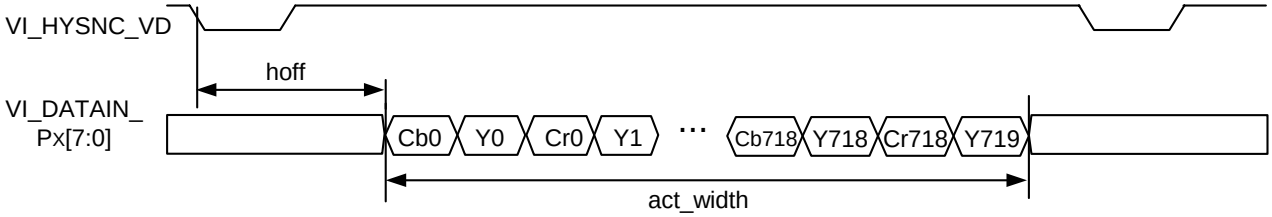


ITU-R BT.601 YCbCr4:2:2

1. Horizontal timing

The horizontal pulse indicates the start of a new line, as shown in Figure 11-9. After hoff clock cycles, an input signal passes the line front blanking area and enters the line active data area. The value of hoff is 244 in the NTSC525 line system or 264 in the PAL625 line system. After act_width clock cycles, the input signal passes the line active data area and enters the line back blanking area. The value of act_width can be set and the typical value is 720 or 704. In addition, the horizontal sync polarity is configurable.

Figure 11-9 ITU-R BT.601 horizontal timing



2. Vertical timing

According to the ITU-R BT.601 protocol, the VSYNC and FIELD signals are vertical sync signals. The VSYNC pulse or FIELD transition indicates the start of the odd field or even field. The VICAP module supports two types of vertical synchronization.

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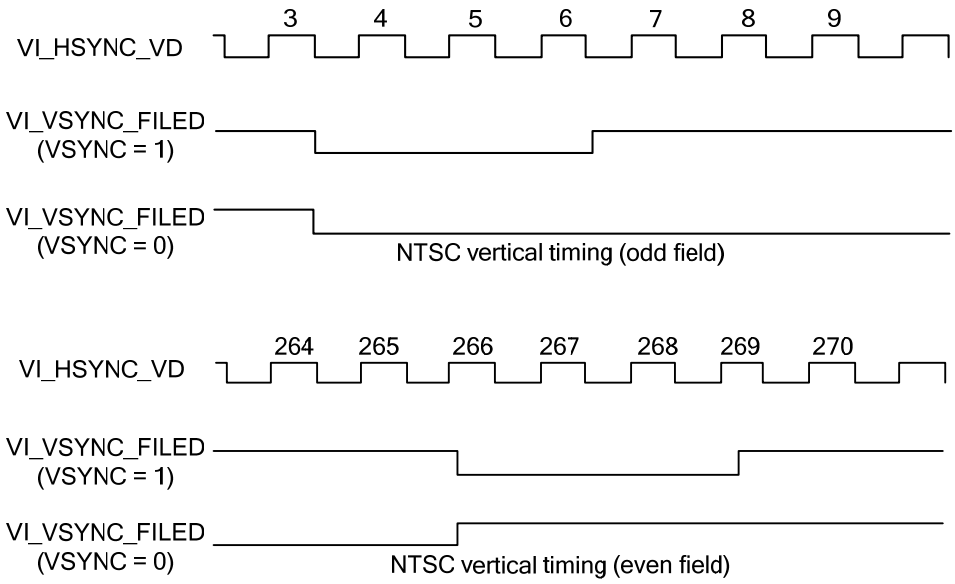
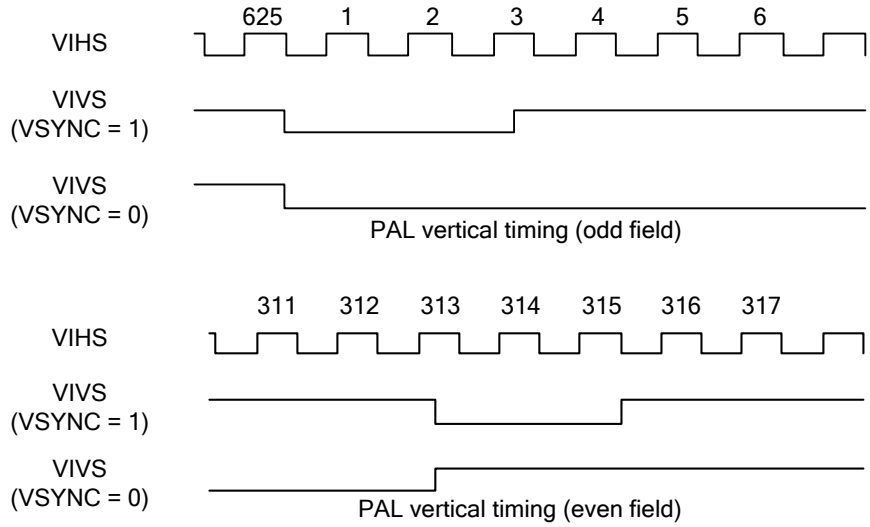
Figure 11-10 shows the NTSC vertical sync timings (525 lines) and Figure 11-11 shows the PAL vertical sync timings (625 lines). Where, VI_HSYNC_VD is the horizontal sync pulse, and VI_VSYNC_FIELD is the vertical sync pulse when VSYNC is 1 or field sync signal when VSYNC is 0.

Figure 11-10 NTSC vertical sync timing



In NTSC interlaced scanning mode, the level of the vertical sync signal in field 1 becomes low at the start of line 4, retains low for three consecutive lines, and then becomes high at the start of line 7. The VICAP module receives 240-line data from line 22 to line 261. The level of the vertical sync signal in field 2 becomes low in the middle of line 266, retains low for three consecutive lines, and then becomes high in the middle of line 269. The VICAP module receives 240-line data from line 285 to line 524.

Figure 11-11 PAL vertical sync timings



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In PAL interlaced scanning mode, the level of the vertical sync signal in field 1 becomes low at the start of line 1, retains low for 2.5 consecutive lines, and then becomes high in the middle of line 3. The VICAP module receives 288-line data from line 24 to line 310. The level of the vertical sync signal in field 2 becomes low in the middle of line 313, retains low for 2.5 consecutive lines, and then becomes high at the start of line 316. The VICAP module receives 288-line data from line 336 to line 623.

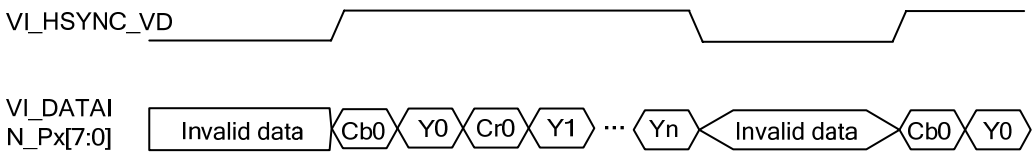
The preceding timings are typical BT.601 vertical timings. The following items are configurable: the number of lines from the start of the field to the active line, the number of field active lines, and vertical sync polarity.

DC Interface Timings

1. Horizontal timing

When a DC is connected to the VICAP module, VI_HSYNC_VD is the data valid signal. The polarity of this signal is configurable. Figure 11-12 shows the horizontal timing.

Figure 11-12 DC horizontal timing



2. Vertical timing

The VICAP module supports the vertical pulse timing and vertical line active timing, as shown in Figure 11-13 and Figure 11-14. In addition, the vertical sync polarity is configurable.

Figure 11-13 DC vertical pulse timing

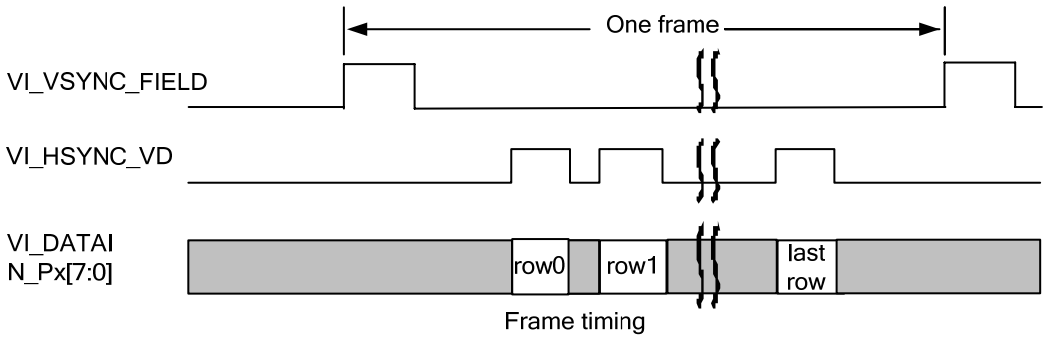


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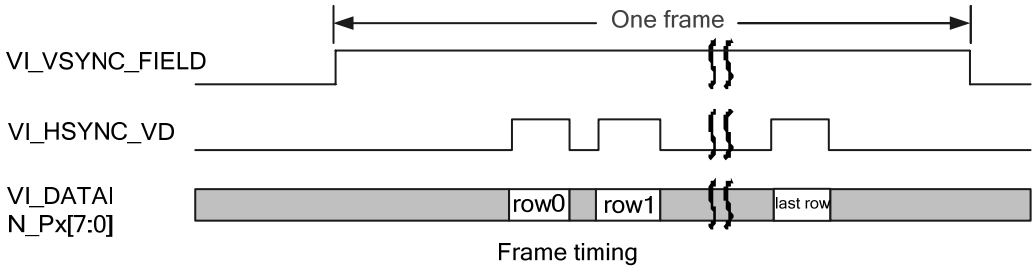
Figure 11-14 DC vertical line active timing

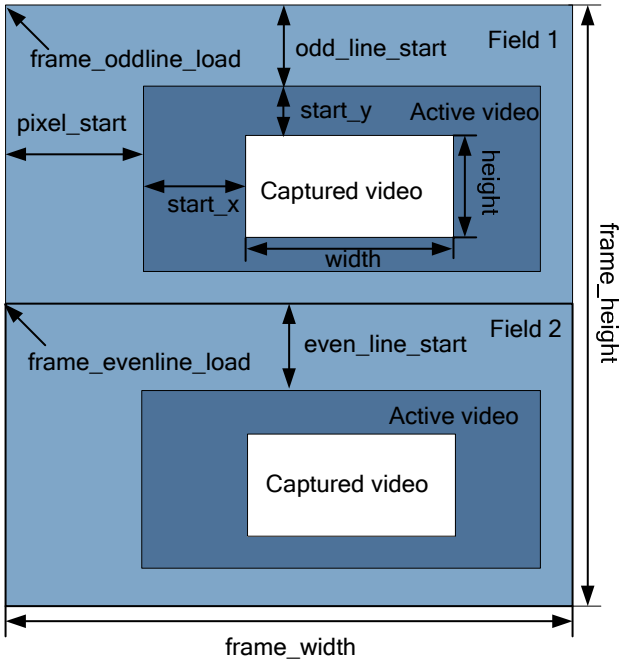


The VICAP module processes the preceding two timings in the same way. To be specific, the VICAP module considers the start of a frame after it detects a rising edge or a falling edge, and then detects the data active signal to check whether the current data is active.

11.1.3.3 Picture Cropping

The active video is shown in Figure 11-15, the actual view range, however, is within the active video range. That is, compared with the boundary of the active video, the boundary of the actual view is shrunk, which avoids the boundary effect.

Figure 11-15 Relationships between the active video area and the horizontal/vertical blanking areas



11.1.3.4 Picture Storage Modes

The picture storage modes are as follows:

- Semi-planar YCbCr storage mode

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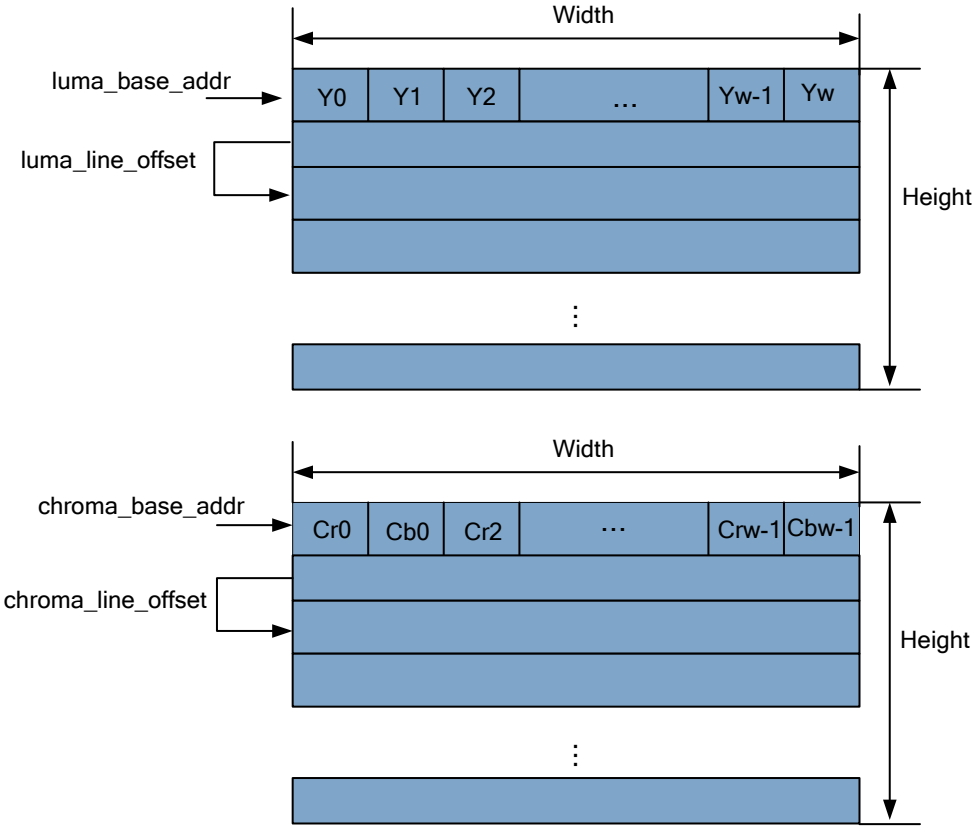
After setting a view area, the system stores the read data in semi-planar mode. That is, the luminance component and the chrominance component are stored in the luminance space and chrominance space of the DDR respectively.

- For one line, the luminance component and chrominance component are stored separately and consecutively.
- For two consecutive lines, the components are stored based on the offset parameter. This parameter defines the storage stride between the start of two lines. The storage locations in the DDR of the luminance component and chrominance component are specified by the start address base_addr. Figure 11-16 shows the mode of storing the YCbCr4:2:2 data captured by the VICAP module.

Figure 11-16 YCbCr4:2:2 storage mode



In the DDR, data is stored by word (32 bits). Four 8-bit pixels constitute a 32-bit word in big endian mode or little endian mode. Figure 11-17 shows how to store the luminance components and chrominance component in big endian mode and little endian mode.

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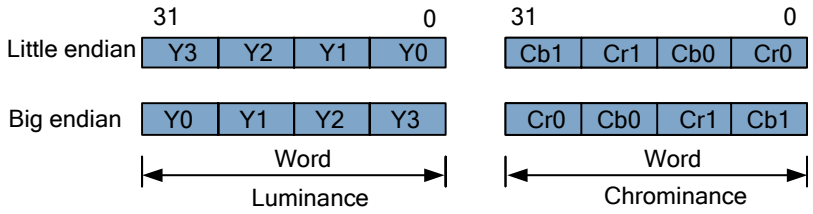
Figure 11-17 Big endian and little endian storage modes



The VICAP module supports only the DDR that stores data in little endian mode.

11.1.3.5 Mirror and Flip

When the pictures captures by the lens are reversed horizontal and vertically due to the reserve installation of the sensor, you can rectify this problem by using the mirror and flip functions of the VICAP module. The functions are implemented by writing reverse DDR address. Note that the start addresses of frames must be 12-bit-aligned.

11.1.4 Operating Mode

11.1.4.1 reg_newer Function of the VICAP Module

- Before enabling a channel of the VICAP module, the software must perform the following operations:
  - Configure the VICAP attribute register.
  - Write 1 to the reg_newer bit to inform the VICAP module that the current register is ready.
- After the VICAP module is enabled, the VICAP logic starts to work. When a field or a frame arrives:
  - If reg_newer is 0, the VICAP module does not receive data. However, it sets the hardware status to snooze and waits for the next field or frame.
  - If reg_newer is 1, the VICAP module starts to receive data, generates the register update interrupt reg_update_int, and sets the hardware status to busy.
- After all the current data is received, the busy status of the hardware is cleared. When the next field or frame arrives:
  - If reg_newer is 0, the data of the next field or frame is not received.
  - If reg_newer is 1, the data of the next field or frame is received.

11.1.4.2 VICAP Hardware Workflow

Figure 11-18 shows the VICAP hardware workflow.

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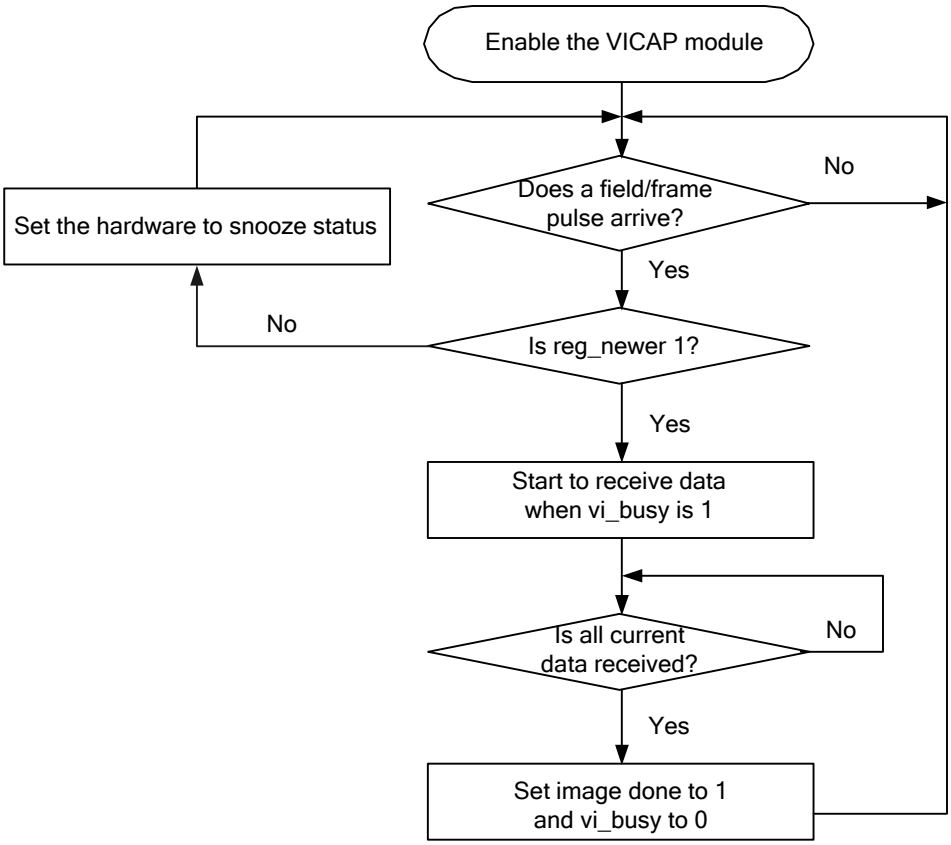
Figure 11-18 VICAP hardware workflow



In BT.656, BT.601, or DC mode, after the data of a specified field or frame is received, the VICAP module checks the reg_newer bit when the next field or frame arrives. If reg_newer is 1, it indicates that software updates or confirms corresponding VICAP registers. In this case, the VICAP module automatically loads the register values configured by the software to the working register (this register is inaccessible to software), clears reg_newer, and starts to receive the data of the next field or frame. If reg_newer is 0, the VICAP module starts to receive data only when reg_newer 1 and a new field or frame arrives.

11.1.4.3 Software Configuration Workflow

Figure 11-19 shows the software configuration process in interrupt mode.

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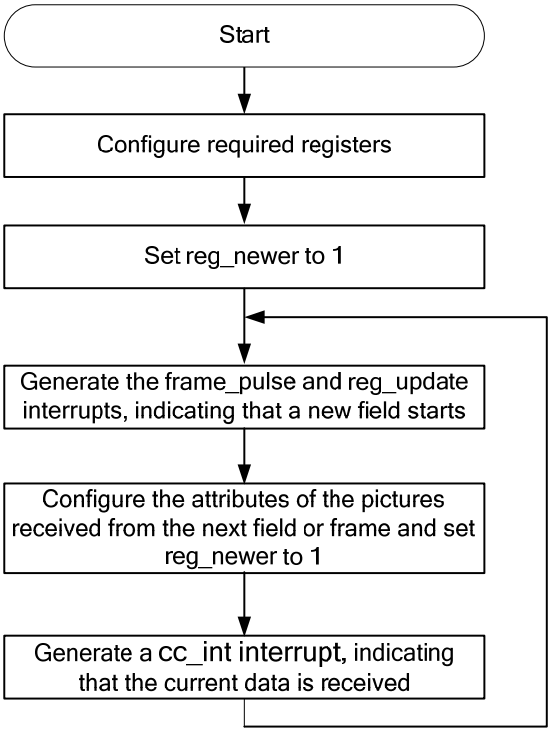
Figure 11-19 Software configuration workflow



In BT.656 or DC mod, the timing registers can be ignored; in BT.601 mode, the timing registers must be configured. The timing registers include the vertical sync timing register and horizontal sync register.

11.1.5 Register Summary

Figure 11-20 shows the space allocation of VICAP registers.

CAUTION

As at most four external ports are supported, the registers with the prefix "PT_" in Table 11-5 exist only in channel 0, channel 4, channel 8, and channel 12. The register whose offset addresses range from 0x0000 to 0x0200 are system registers.

- Port 0 can be connected to any channel of channel 0–channel 3.
- Port 1 can be connected to any channel of channel 4–channel 7.
- Port 2 can be connected to any channel of channel 8–channel 11.
- Port 3 can be connected to any channel of channel 12–channel 15.

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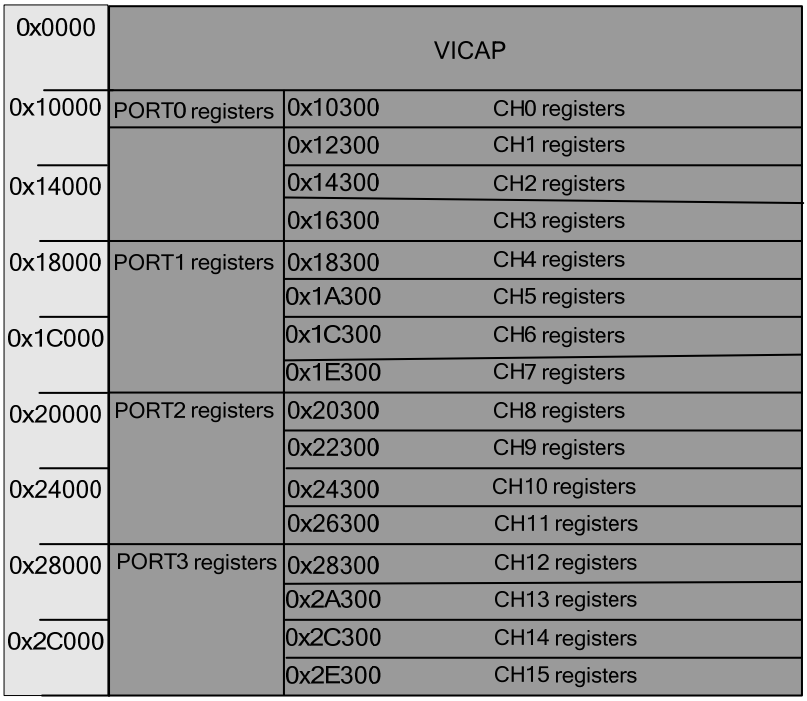
Figure 11-20 Space allocation of VICAP registers



Note: The addresses with "0x" are offset addresses.

Table 11-5 describes the VICAP registers.

NOTE

The register description in section 11.1.6 is applicable to PORT 0 and CH 0.

- PORT 0 is used as an example to introduce PT-XXX in Table 11-5. Compared with PORT0, except that the offset addresses of the PORT1–PORT3 are different from that of PORT0, others are the same
- Chn 0 is used as an example to introduce CH_XXX in Table 11-5. Compared with CH0, except that the offset addresses of the CH1–CH15 are different from that of CH0, others are the same.

Table 11-5 Summary of the VICAP registers (base address: 0x2058_0000)

Offset Address	Register	Description	Page
0x0000	WK_MODE	Global working configuration register	11-19
0x0004	AXI_CFG	Bus configuration register	11-20
0x0008	MIXER0_PRO_CFG 0	Master priority configuration register	11-20
0x0100	VICAP_INT	Interrupt indicator register	11-22
0x10000	PT_INTF_MOD	Port mode register	11-24
0x10004	PT_R_MASK_L	R component mask register	11-26
0x10008	PT_B_MASK_L	B component mask register	11-26

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Offset Address	Register	Description	Page
0x1000C	PT_G_MASK_L	G component mask register	11-27
0x10014	PT_R_OFFSET_L	R component offset register	11-27
0x10018	PT_B_OFFSET_L	B component offset register	11-27
0x1001C	PT_G_OFFSET_L	G component offset register	11-28
0x10040	PT_TEST_CFG	Port test configuration register	11-28
0x10044	PT_ID_STATUS	Port ID status register	11-29
0x10300	CH_INTF_CFG0	Port timing register 0	11-29
0x10304	CH_INTF_CFG1	Port timing register 1	11-31
0x10310	CH_INTF_HFB	Horizontal front blanking width register	11-33
0x10314	CH_INTF_HACT	Horizontal active width register	11-33
0x10318	CH_INTF_HBB	Horizontal back blanking width register	11-33
0x10320	CH_INTF_VFB	Vertical front blanking width register	11-34
0x10324	CH_INTF_VACT	Vertical active area width register	11-34
0x10328	CH_INTF_VBB	Vertical back blanking width register	11-34
0x10330	CH_INTF_VBFB	Vertical bottom front blanking width register	11-35
0x10334	CH_INTF_VBACT	Vertical bottom active width register	11-35
0x10338	CH_INTF_VBBB	Vertical bottom back blanking width register	11-36
0x10360	CH_FSTART_DLY	Frame sync delay register	11-36
0x10400	CH_CTRL	Channel control register	11-36
0x10404	CH_REG_NEWER	Capture control register	11-37
0x10410	CH_CROP_START	Crop start position register	11-37
0x10414	CH_CROP_SIZE	Crop size configuration register	11-38
0x10418	CH_YDES_SIZE	Raw stream luminance storage size register	11-38
0x1041C	CH_CDES_SIZE	Raw stream chrominance storage size register	11-39
0x10420	CH_YBASE_ADDR	Raw stream luminance storage base address register	11-39
0x10424	CH_CBASE_ADDR	Raw stream chrominance storage base address register	11-39

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Offset Address	Register	Description	Page
0x10428	CH_YLINE_OFFSET	Raw stream luminance line offset register	11-40
0x1042C	CH_CLINE_OFFSET	Raw stream chrominance line offset register	11-40
0x10430	CH_INT_RAW	Channel raw interrupt register	11-40
0x10434	CH_INT	Channel interrupt register	11-29
0x10438	CH_INT_MASK	Channel interrupt mask register	11-43
0x1043C	CH_STATUS	Channel status register	11-44
0x10440	CH_IPI_STATUS_SIZE	Channel size indication register	11-45
0x10444	CH_IPI_STATUS_SEAV	Channel SEAV indication register	11-45
0x10500	CH_DITHER_CFG	Dither configuration register	11-46
0x10504	CH_DITHER_COEF0	Dither coefficient register 0	11-47
0x10508	CH_DITHER_COEF1	Dither coefficient register 1	11-47
0x1050C	CH_DITHER_SIZE	Dither input picture width register	11-47
0x10510	CH_MIR_CTRL	Raw stream mirror control register	11-48
0x10700	CH_MSC_CFG	Block mask configuration register	11-48
0x10710	CH_BLOCK0_START	Mask start position register for block 0	11-49
0x10714	CH_BLOCK1_START	Mask start position register for block 1	11-50
0x10718	CH_BLOCK2_START	Mask start position register for block 2	11-50
0x1071C	CH_BLOCK3_START	Mask start position register for block 3	11-50
0x10720	CH_BLOCK0_SIZE	Mask size register for block 0	11-51
0x10724	CH_BLOCK1_SIZE	Mask size register for block 1	11-51
0x10728	CH_BLOCK2_SIZE	Mask size register for block 2	11-52
0x1072C	CH_BLOCK3_SIZE	Mask size register for block 3	11-52
0x10730	CH_BLOCK0_COLOR	Filling color register for block 0	11-53
0x10734	CH_BLOCK1_COLOR	Filling color register for block 1	11-53

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Offset Address	Register	Description	Page
0x10738	CH_BLOCK2_COLOR	Filling color register for block 2	11-53
0x1073C	CH_BLOCK3_COLOR	Filling color register for block 3	11-54
0x10800	CH_VCDS_CFG	Major stream chrominance vertical down sampling configuration register	11-54
0x10808	CH_VCDS_COEF	Major stream chrominance vertical down sampling coefficient register	11-55
0x10940	CH_SCL_LHFIR_SPH	Luminance horizontal scaling parameter configuration register	11-55
0x10944	CH_SCL_CHFIR_SPH	Chrominance horizontal scaling parameter configuration register	11-56
0x10948	CH_SCL_LHFIR_OFFSET	Luminance scaling horizontal offset register	11-57
0x1094C	CH_SCL_CHFIR_OFFSET	Chrominance scaling horizontal offset register	11-57
0x10980	CH_LHFIR_COEF0	Luminance horizontal scaling coefficient register 0	11-58
0x10984	CH_LHFIR_COEF1	Luminance horizontal scaling coefficient register 1	11-58
0x10988	CH_LHFIR_COEF2	Luminance horizontal scaling coefficient register 2	11-59
0x10990	CH_CHFIR_COEF0	Chrominance horizontal scaling coefficient register 0	11-59
0x10994	CH_CHFIR_COEF1	Chrominance horizontal scaling coefficient register 1	11-60
0x10998	CH_CHFIR_COEF2	Chrominance horizontal scaling coefficient register 2	11-60
0x10B00	CH_Y_CLIP_CFG	Chrominance clip configuration register	11-60
0x10B04	CH_C_CLIP_CFG	Luminance clip configuration register	11-61

11.1.6 Register Description

WK_MODE

WK_MODE is a global working configuration register.

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Offset Address	Register Name	Total Reset Value
0x0000	WK_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															power_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	power_mode	Clock mode. 0: The low-power mode is disabled. 1: The low-power mode is enabled.

AXI_CFG

AXI_CFG is a bus configuration register.

Offset Address	Register Name	Total Reset Value
0x0004	AXI_CFG	0xF0F0_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												m1_otd				reserved												m0_otd			
Reset	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved.
[19:16]	RW	m0_id	ID.
[15:4]	-	reserved	Reserved.
[3:0]	RW	m0_otd	Number of outstandings. The number must be between 0 and 4.

MIXER0_PRO_CFG0

MIXER0_PRO_CFG0 is master priority configuration register.

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Offset Address	Register Name	Total Reset Value
0x0008	MIXER0_PRO_CFG0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ch15_c_pro	ch15_y_pro	ch14_c_pro	ch14_y_pro	ch13_c_pro	ch13_y_pro	ch12_c_pro	ch12_y_pro	ch11_c_pro	ch11_y_pro	ch10_c_pro	ch10_y_pro	ch9_c_pro	ch9_y_pro	ch8_c_pro	ch8_y_pro	ch7_c_pro	ch7_y_pro	ch6_c_pro	ch6_y_pro	ch5_c_pro	ch5_y_pro	ch4_c_pro	ch4_y_pro	ch3_c_pro	ch3_y_pro	ch2_c_pro	ch2_y_pro	ch1_c_pro	ch1_y_pro	ch0_c_pro	ch0_y_pro
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	ch15_c_pro	Chrominance priority of channel 15. The value 0 indicates the highest priority.
[30]	RW	ch15_y_pro	Luminance priority of channel 15. The value 0 indicates the highest priority.
[29]	RW	ch14_c_pro	Chrominance priority of channel 14. The value 0 indicates the highest priority.
[28]	RW	ch14_y_pro	Luminance priority of channel 14. The value 0 indicates the highest priority.
[27]	RW	ch13_c_pro	Chrominance priority of channel 13. The value 0 indicates the highest priority.
[26]	RW	ch13_y_pro	Luminance priority of channel 13. The value 0 indicates the highest priority.
[25]	RW	ch12_c_pro	Chrominance priority of channel 12. The value 0 indicates the highest priority.
[24]	RW	ch12_y_pro	Luminance priority of channel 12. The value 0 indicates the highest priority.
[23]	RW	ch11_c_pro	Chrominance priority of channel 11. The value 0 indicates the highest priority.
[22]	RW	ch11_y_pro	Luminance priority of channel 11. The value 0 indicates the highest priority.
[21]	RW	ch10_c_pro	Chrominance priority of channel 10. The value 0 indicates the highest priority.
[20]	RW	ch10_y_pro	Luminance priority of channel 10. The value 0 indicates the highest priority.
[19]	RW	ch9_c_pro	Chrominance priority of channel 9. The value 0 indicates the highest priority.
[18]	RW	ch9_y_pro	Luminance priority of channel 9. The value 0 indicates the highest priority.
[17]	RW	ch8_c_pro	Chrominance priority of channel 8. The value 0 indicates the highest priority.

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[16]	RW	ch8_y_pro	Luminance priority of channel 8. The value 0 indicates the highest priority.
[15]	RW	ch7_c_pro	Chrominance priority of channel 7. The value 0 indicates the highest priority.
[14]	RW	ch7_y_pro	Luminance priority of channel 7. The value 0 indicates the highest priority.
[13]	RW	ch6_c_pro	Chrominance priority of channel 6. The value 0 indicates the highest priority.
[12]	RW	ch6_y_pro	Luminance priority of channel 6. The value 0 indicates the highest priority.
[11]	RW	ch5_c_pro	Chrominance priority of channel 5. The value 0 indicates the highest priority.
[10]	RW	ch5_y_pro	Luminance priority of channel 5. The value 0 indicates the highest priority.
[9]	RW	ch4_c_pro	Chrominance priority of channel 4. The value 0 indicates the highest priority.
[8]	RW	ch4_y_pro	Luminance priority of channel 4. The value 0 indicates the highest priority.
[7]	RW	ch3_c_pro	Chrominance priority of channel 3. The value 0 indicates the highest priority.
[6]	RW	ch3_y_pro	Luminance priority of channel 3. The value 0 indicates the highest priority.
[5]	RW	ch2_c_pro	Chrominance priority of channel 2. The value 0 indicates the highest priority.
[4]	RW	ch2_y_pro	Luminance priority of channel 2. The value 0 indicates the highest priority.
[3]	RW	ch1_c_pro	Chrominance priority of channel 1. The value 0 indicates the highest priority.
[2]	RW	ch1_y_pro	Luminance priority of channel 1. The value 0 indicates the highest priority.
[1]	RW	ch0_c_pro	Chrominance priority of channel 0. The value 0 indicates the highest priority.
[0]	RW	ch0_y_pro	Luminance priority of channel 0. The value 0 indicates the highest priority.

VICAP_INT

VICAP_INT is an interrupt indicator register.

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Offset Address	Register Name	Total Reset Value
0x0100	VICAP_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_ch15	int_ch14	int_ch13	int_ch12	int_ch11	int_ch10	int_ch9	int_ch8	int_ch7	int_ch6	int_ch5	int_ch4	int_ch3	int_ch2	int_ch1	int_ch0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15]	RO	int_ch15	Interrupt indicator of channel 15. 0: No interrupt is generated. 1: An interrupt is generated.
[14]	RO	int_ch14	Interrupt indicator of channel 14. 0: No interrupt is generated. 1: An interrupt is generated.
[13]	RO	int_ch13	Interrupt indicator of channel 13. 0: No interrupt is generated. 1: An interrupt is generated.
[12]	RO	int_ch12	Interrupt indicator of channel 12. 0: No interrupt is generated. 1: An interrupt is generated.
[11]	RO	int_ch11	Interrupt indicator of channel 11. 0: No interrupt is generated. 1: An interrupt is generated.
[10]	RO	int_ch10	Interrupt indicator of channel 10. 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	int_ch9	Interrupt indicator of channel 9. 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	int_ch8	Interrupt indicator of channel 8. 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	int_ch7	Interrupt indicator of channel 7. 0: No interrupt is generated. 1: An interrupt is generated.

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[6]	RO	int_ch6	Interrupt indicator of channel 6. 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	int_ch5	Interrupt indicator of channel 5. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	int_ch4	Interrupt indicator of channel 4. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	int_ch3	Interrupt indicator of channel 3. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	int_ch2	Interrupt indicator of channel 2. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	int_ch1	Interrupt indicator of channel 1. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	int_ch0	Interrupt indicator of channel 0. 0: No interrupt is generated. 1: An interrupt is generated.

PT_INTF_MOD

PT_INTF_MOD is a port mode register.

Offset Address	Register Name	Total Reset Value
0x10000	PT_INTF_MOD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								interleave_seq	ch3_id_en	ch2_id_en	ch1_id_en	ch0_id_en	ch3_id		ch2_id		ch1_id		ch0_id		port_cap_mode		port_mux_mode		fix_code		reserved		port_mod		reserved		clk_mode	port_en

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	-	reserved	Port register. Four ports are supported. The offset addresses are as follows: 0x1_0000–0x1_00FF: offset addresses of port 0 0x1_8000–0x1_80FF: offset addresses of port 1 0x2_0000–0x2_00FF: offset addresses of port 2 0x2_8000–0x2_80FF: offset addresses of port 3 In the following register descriptions, only the offset addresses of port 0 are provided. The descriptions of other ports are similar.
[24]	RW	interleave_seq	Y/C sequence during interleaving. 0: The C component is before the Y component. 1: The Y component is before the C component.
[23]	RW	ch3_id_en	Channel 3 ID enable. 0: The channel ID is not checked. 1: The data channel is selected based on the channel ID.
[22]	RW	ch2_id_en	Channel 2 ID enable. 0: The channel ID is not checked. 1: The data channel is selected based on the channel ID.
[21]	RW	ch1_id_en	Channel 1 ID enable. 0: The channel ID is not checked. 1: The data channel is selected based on the channel ID.
[20]	RW	ch0_id_en	Channel 0 ID enable. 0: The channel ID is not checked. 1: The data channel is selected based on the channel ID.
[19:18]	RW	ch3_id	The data channel is selected based on the channel ID when the channel 3 ID is enabled.
[17:16]	RW	ch2_id	The data channel is selected based on the channel ID when the channel 2 ID is enabled.
[15:14]	RW	ch1_id	The data channel is selected based on the channel ID when the channel 1 ID is enabled.
[13:12]	RW	ch0_id	The data channel is selected based on the channel ID when the channel 0 ID is enabled.
[11:10]	RW	port_cap_mode	Port mode. 0: BT.656 mode 1: BT.601 mode 2: DC mode 3: interleave mode

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[9:8]	RW	port_mux_mode	Multiplexing mode. 0: 1-channel multiplexing mode 01: 2-channel multiplexing mode 10: 4-channel multiplexing mode 11: reserved
[7]	RW	fix_code	MSB of the sync code. 0: The MSB is 1. 1: The MSB is 0.
[6:5]	-	reserved	Reserved.
[4:3]	RW	port_mod	Port mode. 00: single-component input 01: dual-component input 10: tri-component input 11: reserved
[2]	RO	-	reserved
[1]	RW	clk_mode	Clock mode. 0: sampling on the rising edge 1: sampling on the falling edge
[0]	RW	port_en	Port enable. 0: disabled 1: enabled

PT_R_MASK_L

PT_R_MASK_L is R component mask register.

Offset Address	Register Name	Total Reset Value
0x10004	PT_R_MASK_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	r_mask																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	r_mask	R component mask.

PT_B_MASK_L

PT_B_MASK_L is B component mask register.

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Offset Address	Register Name	Total Reset Value
0x10008	PT_B_MASK_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	b_mask																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	b_mask	B component mask.

PT_G_MASK_L

PT_G_MASK_L is G component mask register.

Offset Address	Register Name	Total Reset Value
0x1000C	PT_G_MASK_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	g_mask																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	g_mask	G component mask.

PT_R_OFFSET_L

PT_R_OFFSET_L is R component offset register.

Offset Address	Register Name	Total Reset Value
0x10014	PT_R_OFFSET_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								r_offset							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	RW	r_offset	R component offset.

PT_B_OFFSET_L

PT_B_OFFSET_L is B component offset register.

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Offset Address	Register Name	Total Reset Value
0x10018	PT_B_OFFSET_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								b_offset							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	RW	b_offset	B component offset.

PT_G_OFFSET_L

PT_G_OFFSET_L is G component offset register.

Offset Address	Register Name	Total Reset Value
0x1001C	PT_G_OFFSET_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								g_offset							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	RW	g_offset	G component offset.

PT_TEST_CFG

PT_TEST_CFG is a port test configuration register.

Offset Address	Register Name	Total Reset Value
0x10040	PT_TEST_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														hsync_sel	cbar_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved.

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[2]	RW	interlace	Interlaced/Progressive mode. 0: progressive mode 1: interlaced mode
[1]	RW	hsync_sel	Horizontal sync signal select in test mode.
[0]	RW	cbar_en	color_bar test enable. 0: disabled 1: enabled

PT_ID_STATUS

PT_ID_STATUS is a port ID status register.

Offset Address	Register Name	Total Reset Value
0x10044	PT_ID_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								id3		id2		id1		id0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:6]	RO	id3	Channel 3 ID.
[5:4]	RO	id2	Channel 2 ID.
[3:2]	RO	id1	Channel 1 ID.
[1:0]	RO	id0	Channel 0 ID.

CH_INTF_CFG0

CH_INTF_CFG0 is timing register 0.

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Offset Address	Register Name	Total Reset Value
0x10300	CH_INTF_CFG0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					vsync_valid_neg	vsync_valid	port_scan_mod			port_mode		vsync_mode	vsync_polar	hsync_mode	hsync_polar	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved.
[10]	RW	vsync_valid_neg	Configuration signal of the VI_P_VSYNC_FIELD pin. 0: active high (active when vsync_valid is 1) 1: active low (active when vsync_valid is 1)
[9]	RW	vsync_valid	Configuration signal of the VI_P_VSYNC_FIELD pin. 0: vertical pulse mode 1: vertical active mode
[8:7]	RW	port_scan_mod	Port data input mode. Bit[8]: Scan_mode[1] 0: Y/C composite input mode 1: Y/C separation input mode Bit[7]: Scan_mode[0] 0: interlaced input mode 1: progressive input mode
[6:5]	RW	port_mode	Port data receive mode. 00: BT.656 mode 01: BT.601 mode 10: DC mode Other values: reserved
[4]	RW	vsync_mode	Configuration signal of the VI_P_VSYNC_FIELD pin. 0: field number (odd field or even field) or toggle mode In BT.601 mode, this signal indicates the field number mode. In DC mode, this signal indicates the toggle mode. 1: vertical pulse mode or active mode

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[3]	RW	vsync_polar	Polarity configuration signal of the VI_P_VSYNC_FIELD pin. 0: active high In pulse mode (port_vsync = 1), positive pulse indicates sync pulse. In field number mode (port_vsync = 0), the high level indicates even field and the low level indicates odd field. In line active mode, high level indicates line active. 1: active low In pulse mode (port_vsync = 1), negative pulse indicates sync pulse. In field number mode (port_vsync = 0), the low level indicates even field and the high level indicates odd field. In line active mode, the low level indicates line active.
[2]	RW	hsync_mode	Configuration signal of the VI_P_HSYNC_VD pin. 0: data active signal 1: horizontal sync pulse signal Note: Set this bit to 1 for the 16-bit sync interface.
[1]	RW	hsync_polar	Polarity configuration signal of the VI_P_HSYNC_VD pin. 0: active high In pulse mode (port_hsync = 1), positive pulse indicates sync pulse. In data active mode (port_hsync = 0), the high level indicates data active. 1: active low In pulse mode (port_hsync = 1), negative pulse indicates sync pulse. In data active mode (port_hsync = 0), the low level indicates data active.
[0]	-	reserved	Reserved.

CH_INTF_CFG1

CH_INTF_CFG1 is timing register 1.

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Offset Address	Register Name	Total Reset Value
0x10304	CH_INTF_CFG1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																port_mod				reserved								yuv_seq		ftc_cfg	ftc_polar	reserved	sav_ver_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:14]	RW	port_mod	Port mode. 00: single-component input 01: dual-component input 11: reserved
[13:6]	-	reserved	Reserved.
[5:4]	RW	yuv_seq	YUV input sequence. 00: UYVY 01: VYUY 10: YUYV 11: YVYU UV sequence in dual-component mode. 00: VUVU 01: UVUV 10: reserved 11: reserved
[3]	RW	ftc_cfg	MSB of the BT.656 timing reference code. 0: fixed at 1 1: fixed at 0
[2]	RW	ftc_polar	Polarity of the field indication bit (F) of the BT.656 timing reference code. 0: 1st field:F = 0 and 2nd field:F = 1 (standard) 1: 1st field:F = 1 and 2nd field:F = 0 (non-standard)
[1]	-	reserved	Reserved.
[0]	RW	sav_ver_en	SAV and EAV data check enable. 0: disabled 1: enabled

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CH_INTF_HFB

CH_INTF_HFB is horizontal front blanking width register.

Offset Address	Register Name	Total Reset Value
0x10310	CH_INTF_HFB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	hfb	Horizontal front blanking width.

CH_INTF_HACT

CH_INTF_HACT is horizontal active width register.

Offset Address	Register Name	Total Reset Value
0x10314	CH_INTF_HACT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hact															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	hact	Horizontal active width.

CH_INTF_HBB

CH_INTF_HBB is horizontal back blanking width register.

Offset Address	Register Name	Total Reset Value
0x10318	CH_INTF_HBB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hbb															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	hbb	Horizontal back blanking width.

CH_INTF_VFB

CH_INTF_VFB is vertical front blanking width register.

Offset Address	Register Name	Total Reset Value
0x10320	CH_INTF_VFB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	vfb	Vertical front blanking width.

CH_INTF_VACT

CH_INTF_VACT is vertical active width register.

Offset Address	Register Name	Total Reset Value
0x10324	CH_INTF_VACT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vact															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	vact	Vertical active width.

CH_INTF_VBB

CH_INTF_VBB is vertical back blanking width register.

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Offset Address	Register Name	Total Reset Value
0x10328	CH_INTF_VBB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	vbb	Vertical back blanking width.

CH_INTF_VBFB

CH_INTF_VBFB is vertical bottom front blanking width register.

Offset Address	Register Name	Total Reset Value
0x10330	CH_INTF_VBFB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	vbfb	Vertical bottom front blanking width.

CH_INTF_VBACT

CH_INTF_VBACT is vertical bottom active width register.

Offset Address	Register Name	Total Reset Value
0x10334	CH_INTF_VBACT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vact															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	vact	Vertical bottom active width.

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CH_INTF_VBBB

CH_INTF_VBBB is vertical bottom back blanking width register.

Offset Address	Register Name	Total Reset Value
0x10338	CH_INTF_VBBB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbbb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	vbbb	Vertical bottom back blanking width.

CH_FSTART_DLY

CH_FSTART_DLY is frame sync delay register.

Offset Address	Register Name	Total Reset Value
0x10360	CH_FSTART_DLY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	reserved	Frame sync delay.

CH_CTRL

CH_CTRL is a channel control register.

Offset Address	Register Name	Total Reset Value
0x10400	CH_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ch_en

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	ch_en	Raw stream enable. 0: disabled 1: enabled

CH_REG_NEWER

CH_REG_NEWER is a capture control register.

Offset Address	Register Name	Total Reset Value
0x10404	CH_REG_NEWER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															reg_newer
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	reg_newer	Channel updated. This bit is automatically cleared when a frame is received.

CH_CROP_START

CH_CROP_START is a crop start position register.

Offset Address	Register Name	Total Reset Value
0x10410	CH_CROP_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	y_start	Number of the line from which pictures start to be captured.

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[15:12]	-	reserved	Reserved.
[11:0]	RW	x_start	Number of the pixel from which pictures start to be captured.

CH_CROP_SIZE

CH_CROP_SIZE is a crop size configuration register.

Offset Address	Register Name	Total Reset Value
0x10414	CH_CROP_SIZE	0x023F_03BF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				crop_hgt												reserved				crop_wth											
Reset	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	crop_hgt	Height of a captured picture (in lines).
[15:12]	-	reserved	Reserved.
[11:0]	RW	crop_wth	Width of a line of a captured picture (in pixels).

CH_YDES_SIZE

CH_YDES_SIZE is a raw stream luminance storage size register.

Offset Address	Register Name	Total Reset Value
0x10418	CH_YDES_SIZE	0x023F_03BF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1

Bits	Access	Name	Description
[31:28]	RW	reserved	Reserved.
[27:16]	RW	height	Output height of the Y component (in lines).
[15:12]	-	reserved	Reserved.
[11:0]	RW	width	Output width of the Y component (in pixels).

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CH_CDES_SIZE

CH_CDES_SIZE is a raw stream chrominance storage size register.

Offset Address	Register Name	Total Reset Value
0x1041C	CH_CDES_SIZE	0x023F_03BF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1

Bits	Access	Name	Description
[31:28]	RW	reserved	Reserved.
[27:16]	RW	height	Output height of the C component (in lines).
[15:12]	-	reserved	Reserved.
[11:0]	RW	width	Output width of the C component (in pixels).

CH_YBASE_ADDR

CH_YBASE_ADDR is a raw stream luminance storage base address register.

Offset Address	Register Name	Total Reset Value
0x10420	CH_YBASE_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ybase_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	ybase_addr	Base address for storing the luminance of the raw stream.

CH_CBASE_ADDR

CH_CBASE_ADDR is a raw stream chrominance storage base address register.

Offset Address	Register Name	Total Reset Value
0x10424	CH_CBASE_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cbase_addr																															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cbase_addr	Base address for storing the chrominance of the raw stream.

CH_YLINE_OFFSET

CH_YLINE_OFFSET is a raw stream luminance line offset register.

Offset Address	Register Name	Total Reset Value
0x10428	CH_YLINE_OFFSET	0x0000_03C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																y_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	y_stride	Stride for storing the picture luminance (in bytes).

CH_CLINE_OFFSET

CH_CLINE_OFFSET is a raw stream chrominance line offset register.

Offset Address	Register Name	Total Reset Value
0x1042C	CH_CLINE_OFFSET	0x0000_03C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																c_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	c_stride	Stride for storing the picture chrominance (in bytes).

CH_INT_RAW

CH_INT_RAW is a channel raw interrupt register.

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Offset Address	Register Name	Total Reset Value
0x10430	CH_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													bus_err	buf_ovf	cc_int	reserved						timing_err	field_throw	reserved						reg_update	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	-	reserved	Reserved.
[18]	WC	bus_err	Status of the raw stream bus error interrupt. Writing 1 clears this interrupt. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[17]	WC	buf_ovf	Status of the raw stream internal FIFO overflow error interrupt. Writing 1 clears this interrupt. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[16]	WC	cc_int	Status of the raw stream capture completion interrupt. Writing 1 clears this interrupt. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[15:10]	-	reserved	Reserved.
[9]	WC	timing_err	Status of the timing error interrupt. Writing 1 clears this interrupt. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[8]	WC	field_throw	Status of the field/frame loss interrupt. Writing 1 clears this interrupt. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[7:2]	-	reserved	Reserved.
[1]	WC	reg_update	Status of the register update interrupt. Writing 1 clears this interrupt. 0: No raw interrupt is generated. 1: A raw interrupt is generated.

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[0]	WC	fstart	Status of the field/frame start interrupt. Writing 1 clears this interrupt. 0: No raw interrupt is generated. 1: A raw interrupt is generated.

CH_INT

CH_INT is a channel interrupt register.

Offset Address	Register Name	Total Reset Value
0x10434	CH_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					scl_bus_err	scl_buf_ovf	scl_cc_int	reserved					bus_err	buf_ovf	cc_int	reserved						timing_err	field_throw	reserved						reg_update	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	-	reserved	Reserved.
[18]	RO	bus_err	Status of the raw stream bus error interrupt. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[17]	RO	buf_ovf	Status of the raw stream internal FIFO overflow error interrupt. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[16]	RO	cc_int	Status of the raw stream capture completion interrupt. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[15:10]	-	reserved	Reserved.
[9]	RO	timing_err	Status of the timing error interrupt. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[8]	RO	field_throw	Status of the field/frame loss interrupt. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[7:2]	-	reserved	Reserved.

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[1]	RO	reg_update	Status of the register update interrupt. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	RO	fstart	Status of the frame/field start interrupt. 0: No raw interrupt is generated. 1: A raw interrupt is generated.

CH_INT_MASK

CH_INT_MASK is a channel interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x10438	CH_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					scl_bus_err_en	scl_buf_ovf_en	scl_cc_int_en	reserved				bus_err_en	buf_ovf_en	cc_int_en		reserved						timing_err_en	field_throw_en	reserved						reg_update_en	fstart_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	-	reserved	Reserved.
[18]	RW	bus_err_en	Raw stream bus error interrupt status enable. 0: masked 1: enabled
[17]	RW	buf_ovf_en	Raw stream internal FIFO overflow error interrupt status enable. 0: masked 1: enabled
[16]	RW	cc_int_en	Raw stream capture completion interrupt status enable. 0: masked 1: enabled
[15:10]	-	reserved	Reserved.
[9]	RW	timing_err_en	Timing error interrupt status enable. 0: masked 1: enabled

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[8]	RW	field_throw_en	Field/Frame loss interrupt status enable. 0: masked 1: enabled
[7:2]	-	reserved	Reserved.
[1]	RW	reg_update_en	Register update interrupt status enable. 0: masked 1: enabled
[0]	RW	fstart_en	Frame/field start interrupt status enable. 0: masked 1: enabled

CH_STATUS

CH_STATUS is a channel status register.

Offset Address	Register Name	Total Reset Value
0x1043C	CH_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												scl_busy	scl_bus_err	scl_buf_ovf	scl_image_done	reserved						timing_err	field_throw	reserved							field2
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RW	reserved	Reserved.
[19]	RO	busy	Working status. 0: idle 1: busy
[18]	RO	bus_err	Bus error. 0: correct 1: incorrect
[17]	RO	buf_ovf	Internal buffer overflow. 0: not overflow 1: overflow

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[16]	RO	image_done	Capture completion. 0: not complete 1: complete
[15:10]	-	reserved	Reserved.
[9]	RO	timing_err	Timing error status. 0: correct 1: incorrect
[8]	RO	field_throw	Field/Frame data loss. 0: not lost 1: lost
[7:1]	-	reserved	Reserved.
[0]	RO	field2	Odd/Even field indicator. 0: odd field 1: even field

CH_IPI_STATUS_SIZE

CH_IPI_STATUS_SIZE is a channel size indication register.

Offset Address	Register Name	Total Reset Value
0x10440	CH_IPI_STATUS_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	height	Picture height.
[15:0]	-	reserved	Reserved.

CH_IPI_STATUS_SEAV

CH_IPI_STATUS_SEAV is a channel SEAV indication register.

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Offset Address	Register Name	Total Reset Value
0x10444	CH_IPI_STATUS_SEAV	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																SEAV								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:8]	RO	SEAV	SEAV code value.
[7:0]	-	reserved	Reserved.

CH_DITHER_CFG

CH_DITHER_CFG is a dither configuration register.

Offset Address	Register Name	Total Reset Value
0x10500	CH_DITHER_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_md				reserved																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	dither_md	Dither mode select. 000: 12-bit inputs, 10-bit outputs, no dithering, and direct bit truncation 001: 12-bit inputs, 10-bit output, and time-domain dithering 010: 12-bit inputs, 10-bit output, and spatial-domain dithering 011: 12-bit inputs, 8-bit output, and time-domain and spatial-domain dithering 100: 12-bit inputs, 10-bit outputs, and round off 101: 12-bit inputs, 8-bit outputs, and round off 111: dithering bypass
[28:0]	-	reserved	Reserved.

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CH_DITHER_COEF0

CH_DITHER_COEF0 is dither coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x10504	CH_DITHER_COEF0	0x3860_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_coef3								dither_coef2								dither_coef1								dither_coef0							
Reset	0	0	1	1	1	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dither_coef3	Coefficient 3 for the dither in time-domain mode.
[23:16]	RW	dither_coef2	Coefficient 2 for the dither in time-domain mode.
[15:8]	RW	dither_coef1	Coefficient 1 for the dither in time-domain mode.
[7:0]	RW	dither_coef0	Coefficient 0 for the dither in time-domain mode.

CH_DITHER_COEF1

CH_DITHER_COEF1 is dither coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x10508	CH_DITHER_COEF1	0xFBE7_0F1E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_coef7								dither_coef6								dither_coef5								dither_coef4							
Reset	1	1	1	1	1	0	1	1	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	0

Bits	Access	Name	Description
[31:24]	RW	dither_coef7	Coefficient 7 for the dither in time-domain mode.
[23:16]	RW	dither_coef6	Coefficient 6 for the dither in time-domain mode.
[15:8]	RW	dither_coef5	Coefficient 5 for the dither in time-domain mode.
[7:0]	RW	dither_coef4	Coefficient 4 for the dither in time-domain mode.

CH_DITHER_SIZE

CH_DITHER_SIZE is a dither input picture width register.

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Offset Address	Register Name	Total Reset Value
0x1050C	CH_DITHER_SIZE	0x0000_03BF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved.
[11:0]	RW	width	Input picture width of the dither.

CH_MIR_CTRL

CH_MIR_CTRL is a raw stream mirror control register.

Offset Address	Register Name	Total Reset Value
0x10510	CH_MIR_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														flip_en	mir_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved.
[1]	RW	flip_en	Flip enable. 0: disabled 1: enabled
[0]	RW	mir_en	Mirror enable. 0: disabled 1: enabled

CH_MSC_CFG

CH_MSC_CFG is a block mask configuration register.

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Offset Address	Register Name	Total Reset Value
0x10700	CH_MSC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												msc3_en	msc2_en	msc1_en	msc0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved.
[3]	RW	msc3_en	Block 3 mask enable. 0: disabled 1: enabled
[2]	RW	msc2_en	Block 2 mask enable. 0: disabled 1: enabled
[1]	RW	msc1_en	Block 1 mask enable. 0: disabled 1: enabled
[0]	RW	msc0_en	Block 0 mask enable. 0: disabled 1: enabled

CH_BLOCK0_START

CH_BLOCK0_START is the mask start position register for block 0.

Offset Address	Register Name	Total Reset Value
0x10710	CH_BLOCK0_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	y_start	Vertical start point for masking block 0.
[15:12]	-	reserved	Reserved.
[11:0]	RW	x_start	Horizontal start point for masking block 0.

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CH_BLOCK1_START

CH_BLOCK1_START is the mask start position register for block 1.

Offset Address	Register Name	Total Reset Value
0x10714	CH_BLOCK1_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	y_start			reserved	x_start		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	y_start	Vertical start point for masking block 1.
[15:12]	-	reserved	Reserved.
[11:0]	RW	x_start	Horizontal start point for masking block 1.

CH_BLOCK2_START

CH_BLOCK2_START is the mask start position register for block 2.

Offset Address	Register Name	Total Reset Value
0x10718	CH_BLOCK2_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	y_start			reserved	x_start		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	y_start	Vertical start point for masking block 2.
[15:12]	-	reserved	Reserved.
[11:0]	RW	x_start	Horizontal start point for masking block 2.

CH_BLOCK3_START

CH_BLOCK3_START is the mask start position register for block 3.

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Offset Address	Register Name	Total Reset Value
0x1071C	CH_BLOCK3_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	y_start	Vertical start point for masking block 3.
[15:12]	-	reserved	Reserved.
[11:0]	RW	x_start	Horizontal start point for masking block 3.

CH_BLOCK0_SIZE

CH_BLOCK0_SIZE is the mask size register for block 0.

Offset Address	Register Name	Total Reset Value
0x10720	CH_BLOCK0_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				blk_height												reserved				blk_width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	blk_height	Vertical height for masking block 0.
[15:12]	-	reserved	Reserved.
[11:0]	RW	blk_width	Horizontal width for making block 0.

CH_BLOCK1_SIZE

CH_BLOCK1_SIZE is the mask size register for block 1.

Offset Address	Register Name	Total Reset Value
0x10724	CH_BLOCK1_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				blk_height												reserved				blk_width											

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	blk_height	Vertical height for masking block 1.
[15:12]	-	reserved	Reserved.
[11:0]	RW	blk_width	Horizontal width for making block 1.

CH_BLOCK2_SIZE

CH_BLOCK2_SIZE is the mask size register for block 2.

Offset Address	Register Name	Total Reset Value
0x10728	CH_BLOCK2_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				blk_height												reserved				blk_width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	blk_height	Vertical height for masking block 2.
[15:12]	-	reserved	Reserved.
[11:0]	RW	blk_width	Horizontal width for making block 2.

CH_BLOCK3_SIZE

CH_BLOCK3_SIZE is the mask size register for block 3.

Offset Address	Register Name	Total Reset Value
0x1072C	CH_BLOCK3_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				blk_height												reserved				blk_width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	blk_height	Vertical height for masking block 3.
[15:12]	-	reserved	Reserved.

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[11:0]	RW	blk_width	Horizontal width for making block 3.

CH_BLOCK0_COLOR

CH_BLOCK0_COLOR is the filling color register for block 0.

Offset Address	Register Name	Total Reset Value
0x10730	CH_BLOCK0_COLOR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								blk_cr								blk_cb								blc_y							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	blk_cr	Cr component of the filling color of block 0.
[15:8]	RW	blk_cb	Cb component of the filling color of block 0.
[7:0]	RW	blc_y	Y component of the filling color of block 0.

CH_BLOCK1_COLOR

CH_BLOCK1_COLOR is the filling color register for block 1.

Offset Address	Register Name	Total Reset Value
0x10734	CH_BLOCK1_COLOR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								blk_cr								blk_cb								blc_y							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	blk_cr	Cr component of the filling color of block 1.
[15:8]	RW	blk_cb	Cb component of the filling color of block 1.
[7:0]	RW	blc_y	Y component of the filling color of block 1.

CH_BLOCK2_COLOR

CH_BLOCK2_COLOR is the filling color register for block 2.

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Offset Address	Register Name	Total Reset Value
0x10738	CH_BLOCK2_COLOR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								blk_cr								blk_cb								blc_y							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	blk_cr	Cr component of the filling color of block 2.
[15:8]	RW	blk_cb	Cb component of the filling color of block 2.
[7:0]	RW	blc_y	Y component of the filling color of block 2.

CH_BLOCK3_COLOR

CH_BLOCK3_COLOR is the filling color register for block 3.

Offset Address	Register Name	Total Reset Value
0x1073C	CH_BLOCK3_COLOR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								blk_cr								blk_cb								blc_y							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	blk_cr	Cr component of the filling color of block 3.
[15:8]	RW	blk_cb	Cb component of the filling color of block 3.
[7:0]	RW	blc_y	Y component of the filling color of block 3.

CH_VCDS_CFG

CH_VCDS_CFG is a major stream chrominance vertical down sampling configuration register.

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Offset Address	Register Name	Total Reset Value
0x10800	CH_VCDS_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															cds_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	cds_en	Down sampling enable. 0: disabled 1: enabled

CH_VCDS_COEF

CH_VCDS_COEF is a major stream chrominance vertical down sampling coefficient register.

Offset Address	Register Name	Total Reset Value
0x10808	CH_VCDS_COEF	0x0000_001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												coef1				reserved												coef0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.
[20:16]	RW	coef1	Down sampling coefficient 1.
[15:5]	-	reserved	Reserved.
[4:0]	RW	coef0	Down sampling coefficient 0.

CH_LHFIR_SPH

CH_SCL_LHFIR_SPH is a luminance horizontal scaling parameter configuration register.

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Offset Address	Register Name	Total Reset Value
0x10940	CH_LHFIR_SPH	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hlmsc_en	reserved															hlratio				reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hlmsc_en	Luminance horizontal scaling enable. 0: disabled 1: enabled
[30:16]	-	reserved	Reserved.
[15:12]	RW	hlratio	Luminance horizontal scaling ratio. It is calculated by dividing the output width by the input width. If horizontal pre-processing is enabled, the input width after pre-processing is used. The ratio is in the format of (u, 4). That is, the ratio is an unsigned bit and consists of a 4-bit integral part.
[11:0]	-	reserved	Reserved.

CH_CHFIR_SPH

CH_CHFIR_SPH is a chrominance horizontal scaling parameter configuration register.

Offset Address	Register Name	Total Reset Value
0x10944	CH_CHFIR_SPH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hchmsc_en	reserved															hchratio				reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hchmsc_en	Chrominance horizontal scaling enable. 0: disabled 1: enabled
[30:16]	-	reserved	Reserved.

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[15:12]	RW	hchratio	Chrominance horizontal scaling ratio. It is calculated by dividing the output width by the input width. If horizontal pre-processing is enabled, the input width after pre-processing is used. The ratio is in the format of (u, 4). That is, the ratio is an unsigned number and consists of a 4-bit integral part.
[11:0]	-	reserved	Reserved.

CH_LHFIR_OFFSET

CH_LHFIR_OFFSET is a luminance scaling horizontal offset register.

Offset Address	Register Name	Total Reset Value
0x10948	CH_LHFIR_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hluma_offset				reserved												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16:12]	RW	hluma_offset	Luminance horizontal start position offset, in the format of (s, 5). That is, the offset value consists of a 1-bit signed bit and 4-bit integral part. The value is expressed as a complementary code and the offset value ranges from –6 to +15.
[11:0]	-	reserved	Reserved.

CH_CHFIR_OFFSET

CH_CHFIR_OFFSET is a chrominance scaling horizontal offset register.

Offset Address	Register Name	Total Reset Value
0x1094C	CH_CHFIR_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hchroma_offset				reserved												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16:12]	RW	hchroma_offset	Chrominance horizontal start position offset, in the format of (s, 5). That is, the offset value consists of a 1-bit signed bit and 4-bit integral part. The value is expressed as a complementary code and the offset value ranges from –6 to +15.

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[11:0]	-	reserved	Reserved.

CH_LHFIR_COEF0

CH_LHFIR_COEF0 is luminance horizontal scaling coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x10980	CH_LHFIR_COEF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef2								coef1								coef0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved.
[29:20]	RW	coef2	Luminance horizontal scaling and filtering coefficient 2.
[19:10]	RW	coef1	Luminance horizontal scaling and filtering coefficient 1.
[9:0]	RW	coef0	Luminance horizontal scaling and filtering coefficient 0. 8-tap horizontal scaling (integral multiple) is supported.

CH_LHFIR_COEF1

CH_LHFIR_COEF1 is luminance horizontal scaling coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x10984	CH_LHFIR_COEF1	0x0000_01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef5								coef4								coef3											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved.
[29:20]	RW	coef5	Luminance horizontal scaling and filtering coefficient 5.
[19:10]	RW	coef4	Luminance horizontal scaling and filtering coefficient 4.

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[9:0]	RW	coef3	Luminance horizontal scaling and filtering coefficient 3.

CH_LHFIR_COEF2

CH_LHFIR_COEF2 is luminance horizontal scaling coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x10988	CH_LHFIR_COEF2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												coef7												coef6							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved.
[19:10]	RW	coef7	Luminance horizontal scaling and filtering coefficient 7.
[9:0]	RW	coef6	Luminance horizontal scaling and filtering coefficient 6.

CH_CHFIR_COEF0

CH_CHFIR_COEF0 is chrominance horizontal scaling coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x10990	CH_CHFIR_COEF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		coef2										coef1												coef0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved.
[29:20]	RW	hch_coef2	Chrominance horizontal scaling and filtering coefficient 2.
[19:10]	RW	hch_coef1	Chrominance horizontal scaling and filtering coefficient 1.
[9:0]	RW	hch_coef0	Chrominance horizontal scaling and filtering coefficient 0. 8-tap horizontal scaling (integral multiple) is supported.

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CH_CHFIR_COEF1

CH_CHFIR_COEF1 is chrominance horizontal scaling coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x10994	CH_CHFIR_COEF1	0x0000_01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef5								coef4								coef3											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved.
[29:20]	RW	coef5	Chrominance horizontal scaling and filtering coefficient 5.
[19:10]	RW	coef4	Chrominance horizontal scaling and filtering coefficient 4.
[9:0]	RW	coef3	Chrominance horizontal scaling and filtering coefficient 3.

CH_CHFIR_COEF2

CH_CHFIR_COEF2 is chrominance horizontal scaling coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x10998	CH_CHFIR_COEF2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												hch_coef7								hch_coef6											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved.
[19:10]	RW	hch_coef7	Chrominance horizontal scaling and filtering coefficient 7.
[9:0]	RW	hch_coef6	Chrominance horizontal scaling and filtering coefficient 6.

CH_Y_CLIP_CFG

CH_Y_CLIP_CFG is a luminance clip configuration register.

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Offset Address	Register Name	Total Reset Value
0x10B00	CH_Y_CLIP_CFG	0x00FF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								max								reserved								min							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	max	Maximum output value.
[15:8]	-	reserved	Reserved.
[7:0]	RW	min	Minimum output value.

CH_C_CLIP_CFG

CH_C_CLIP_CFG is a chrominance clip configuration register.

Offset Address	Register Name	Total Reset Value
0x10B04	CH_C_CLIP_CFG	0x00FF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								max								reserved								min							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	max	Maximum output value.
[15:8]	-	reserved	Reserved.
[7:0]	RW	min	Minimum output value.

11.2 VDP

11.2.1 Overview

The video display (VDP) module reads video and graphics data from the DDR, overlays the data on the video and graphics layers, and transmits the data through the display channel.

11.2.2 Function Description

Figure 11-21 shows the overall architecture of the VDP module.

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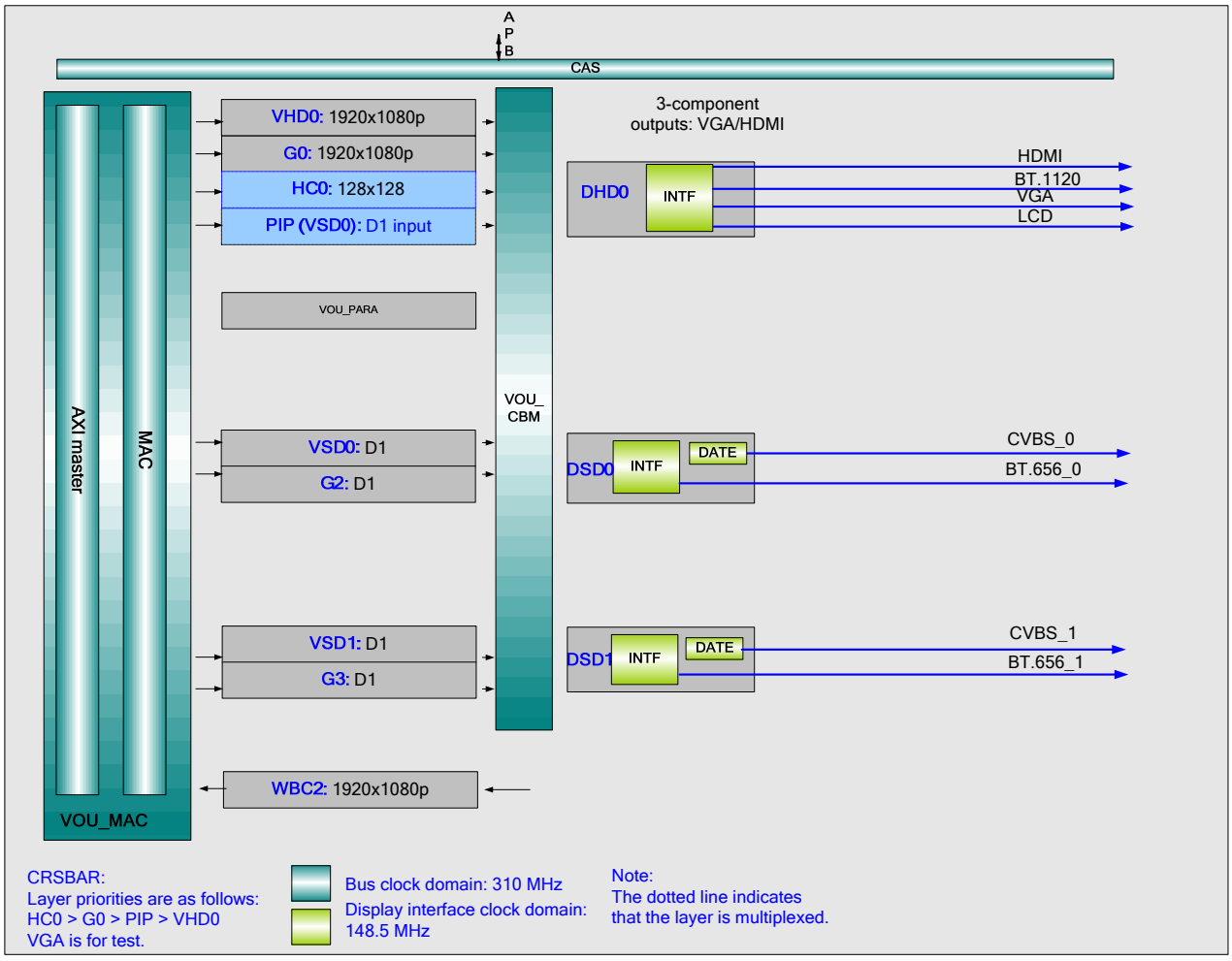
Figure 11-21 Overall architecture of the VDP module



- Surfaces: data paths of bus inputs. The surface reads the bus data of a layer and processes data. The surfaces include video layers (VHD0, VSD0 and VSD1), graphics layers (G0, G2, and G3), and cursor layer HC0.
- Display channel: Display channels include high–definition display channels (DHD0) and standard-definition display channels (DSD0 and DSD1).
- Crossbar and mixer (CBM): It overlays the video layer and graphics layers.
- Parameter (PARA): It updates and loads the channel automatic contrast control (ACC) coefficients.
- MAC: bus request arbitration module of each layer. Each module reads data from the DDR over the AXI bus. The MAC arbitrates when layers raise requests.
- Control and status (CAS): It configures registers over the APB and reports the status of other modules to the CPU.

The VDP registers are classified into:

- Global registers

  Include the bus configuration register, interrupt register, and version register.
- Surface registers

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Include the video layer configuration register and graphics layer configuration register.

- Display channel registers

  Include the DHD and DSD configuration registers.

- Coefficient register

  Video layer ACC coefficient. As the coefficient data amount is large, the coefficient is read by using the AXI master, which does not consume the CPU resources.

The VDP module has the following features:

- Digital output interfaces
  - ITU-R BT.656 SD output
  - ITU-R BT.1120 HD output, VGA HD output, and HDMI HD output, and LCD output. LCD output and ITU-R BT.1120 output are unavailable at the same time.
  - Data from the same channel simultaneously displayed over the BT.1120/LCD, HDMI, and VGA interfaces (data cannot be output over the LCD and VGA interfaces at the same time)
  - 1- or 2-channel BT.656 outputs from DSD0 or DSD1 over the HD BT.1120 interface
- Analog output interfaces

  CVBS output from DSD0 and DSD1 (same pictures can also be output over the ITU-R BT.656 interface)
- Video layer
  - Input pixel formats: semi-planar YCbCr4:2:2 and semi-planar YCbCr4:2:0
  - Global alpha
  - Color space conversion (CSC) and adjustment of luminance, contrast, hue, and saturation
  - Vertical chrominance up sampling
  - Horizontal chrominance up sampling
  - Read/write on multiple regions (32 regions for VHD0 and eight regions for VSD0)
  - At most 8x scaling
- Graphics layer
  - Three graphics layers: graphics layers 0, 2, and 3.
  - One hardware cursor layer: HC0
  - Data formats: ARGB8888 and ARGB1555
  - Global alpha and pixel alpha
  - Three data extended modes

    Lower bits stuffed with 0s

    Lower bits stuffed with the MSB

    Lower bits stuffed with upper bits
  - Even width and height
  - Minimum input/output resolution 32x32 and maximum input/output resolution 2560x1600 for G0
  - Minimum input/output resolution 32x32 and maximum input/output resolution 720x576 for G2 or G3
- Overlay

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  - 256-level alpha blending of one background layer, two video layers, one graphics layer, and one cursor layer. The priorities of graphics layers and video layers can be set and the alpha value of the layer with the highest priority is used during overlay.
  - Adjustment of the size and position of each overlay layer
  - Adjustment of the luminance, contrast, hue, and saturation of overlaid pictures–
- The VDP module has one HD channel and two SD channels. Each channel has a separate vertical timing interrupt (indicating the end of a field/frame), three low bandwidth interrupts, and one writeback channel (WBC) interrupt.

11.2.3 Operating Mode

11.2.3.1 Clock Configuration

The VDP module has three clock sources:

- VPLL0
- VPLL2
- AXI bus clock

The following clocks can be configured by using corresponding registers:

- BT.1120 interface clock that from DHD0 (when the BT.1120 interface outputs BT.1120 signals) or from DSD0/DSD1 (when the BT.1120 interface outputs BT.656 signals)
- HDMI interface clock from DHD0
- DAC1 interface clock from DHD0

Table 11-6 and Table 11-7 describe the mappings between channel interface types and PLL configurations. To look up the PLL configuration based on a channel, perform the following steps:

Step 1 Specify a channel.

Step 2 Look up the interface type in the table corresponding to the specified channel.

Step 3 Look up the PLL and DATA and DAC configurations in the corresponding interface type row.

----End

Table 11-6 Clock configuration of DHD0 (interface clocks and data from DHD0 or DSD0/DSD1)

	DHD0 (MHz)	DSD0/DSD1 (MHz)	PLL0 or PLL2 (MHz)	HDATE (MHz)	DAC1 (MHz)
BT.1120/ HDMI	148.5	N/A	PLL0 (297)	N/A	N/A
	74.25	N/A	PLL0 (148.5)	N/A	N/A
VGA	148.5	N/A	PLL0 (148.5)	N/A	148.5
BT.656	N/A	27	PLL2 (27)	N/A	N/A

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Table 11-7 Clock configuration of DSD0 or DSD1

	DSD0 or DSD1	PLL0, PLL1, or PLL2 (MHz)	SDATE (MHz)	DAC0 (MHz)
CVBS	27	PLL2 (27)	54	54
BT.656	27	PLL2 (27)	N/A	N/A

11.2.3.2 Reset

The VDP module can be reset by a hard reset or soft reset.

The VDP module has the following three soft reset signals (writing 1 to the corresponding clock reset control bit resets the corresponding module and writing 0 deasserts the reset):

- Soft reset shared by two SD channels
- HD0 soft reset
- AXI bus soft reset

CAUTION

Before soft-reset the AXI bus, do as follows:

- Disable all layers.
- Configure the bus reset request after the next field/frame interrupt is detected.

11.2.3.3 Bus Configurations

AXI Masters

The VDP module provides one master interface to improve the bus access efficiency. As the VDP module supports AXI master interfaces, VHD0, VSD0–VSD1, G0, G2, HC0, or WBC2 can read or write data over master.

Register Configuration

The VDP registers are read and written over the APB interface. The APB clock is 150 MHz. For the Hi3521, the base address of VDP registers is 0x205C_0000, the register addressing space is 64 KB, and the address offset range is 0x0000–0xFFFF.

Outstanding Configuration

The depth of the AXI master outstanding ranges from 0 to 7. When the outstanding depth is set to 0, the AXI master does not operate the bus.

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11.2.3.4 Analog Output Interfaces

The SD channels support at most two CVBS output interfaces. The VDP module provides the following analog output interfaces:

- DSD0->CVBS_0
- DSD1->CVBS_1
- PAL and NTSC norms supported by the CVBS interfaces

11.2.3.5 Digital Output Interfaces

The VDP module supports four types of digital output interfaces:

- ITU-R BT.656 interface
- ITU-R BT.1120 interface
- HDMI
- VGA interface
- LCD interface

The LCD interface and BT.1120 interface cannot be used at the same time. The BT.1120 interface can output 1- or 2-channel BT.656 signals from DSD0 or DSD1.

ITU-R BT.656 Interfaces

The VDP module supports a maximum of two BT.656 output interfaces:

- DSD0->BT.656_0
- DSD1->BT.656_1

The ITU-R BT.656 interfaces support the following two norms:

- PAL norm (625 line/frame@25 frame/second)
- NTSC norm (525 line/frame@30 frame/second)

According to the ITU-R Recommendation BT.656, sync signals are included in video data streams. The special bytes SAV and EAV in data streams indicate the start and end of the line respectively.

In video streams, the header of the timing reference code indicates that the following byte is SAV or EAV. The timing reference code consists of FF 00 00. FF and 00 indicate the reserved bytes of the image encoding data, that is, non-image data. Figure 11-22 shows the format of the ITU-R BT. 656 line data stream.

Figure 11-22 Format of the ITU-R BT.656 YCbCr 4:2:2 line data

Line Blanking		Timing Reference code				YCbCr4:2:2 with 720 Valid Pixels						Timing Reference Code				Line Blanking	
...	10	FF	00	00	SAV	C_B0	Y0	CR0	Y1	...	Y719	FF	00	00	EAV	80	...

According to the ITU-R BT.656 YCbCr 4:2:2 protocol, the ratio of sampled luminance signals to sampled chrominance signals is 2:1. Two luminance signals share a CbCr signal.

The recommended number of active luminance pixel points sampled per line is 720 and the recommended number of active chrominance pixel points sampled per line is 360. The chrominance pixel points are sampled from the corresponding even pixels in co-sited format.

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The start sampling point is pixel 0. When luminance and chrominance signals are transmitted in the same 8-bit channel, the transmission sequence is C_B0 Y0 C_R0 Y1 C_B2 Y2 C_R2 Y3…C_B718 Y718 C_R718 Y719 and the clock frequency is 27 MHz.

ITU-R BT.1120 Interface

The video source of the BT.1120 interface can be DHD0.

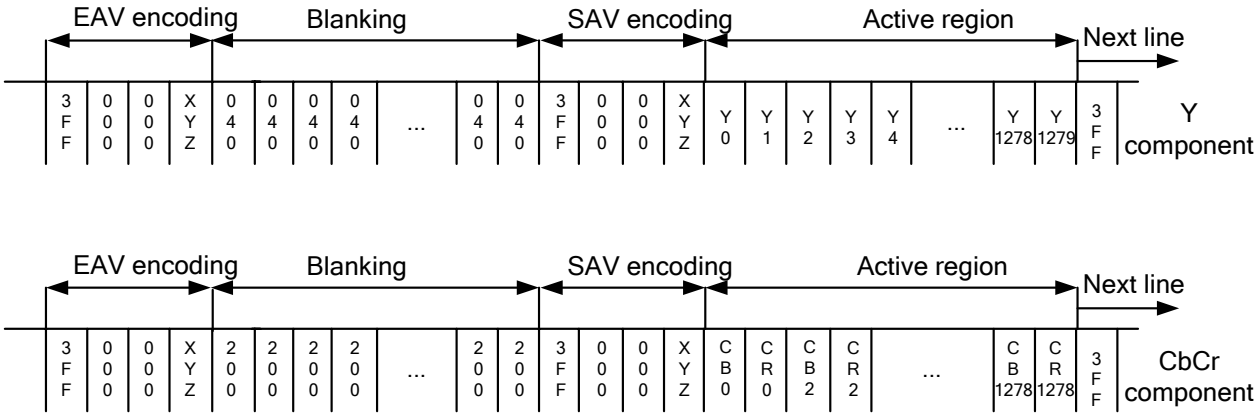
- External synchronization, line/field synchronization, and data active
- Maximum output resolution of 1920x1080
- Data Y/C exchange

In BT.1120 mode, sync signals are included in video data streams. The special bytes SAV and EAV in data streams indicate the start and end of the line respectively.

According to the ITU-R BT.1120 YCbCr 4:2:2, the ratio of sampled luminance signals to sampled chrominance signals is 2:1. Two luminance signals share a CbCr signal.

Figure 11-23 shows the scanning timing at the resolution of 1280x720p. Luminance signals and chrominance signals are transmitted in different channels, and the clock frequency is 74.25 MHz.

Figure 11-23 Horizontal timing of the BT.1120 interface



HDMI

The Hi3521 HDMI complies with the 1.4a protocol. The video source of the HDMI can be DHD0.

- Maximum output resolution of 1600x1200 or 1920x1080
- Clock frequency ranging from 74.25 MHz to 165 MHz
- Interlaced and progressive display
- Data format of YCbCr444

VGA Interface

The video source of the VGA interface can be DHD0.

- Output resolution ranging from 720pP50 to 1600x1200 or 1920x1080

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- Clock frequency ranging from 40 MHz to 268.5 MHz
- Progressive display
- RGB888 output supported by configuring the channel CSC function

LCD Interface

The video source of the LCD interface can be DHD0.

- Output resolution ranging from 720pP50 to 1600x1200 or 1920x1080
- Clock frequency ranging from 40 MHz to 268.5 MHz
- Progressive display
- RGB888 output supported by configuring the channel CSC function

11.2.3.6 HD Video Layers

Reading Multiple Regions

The VDP module can read multiple regions to display their pictures at the same time. The data sources of regions can be different. The details are as follows:

- Multiple regions supported by VHD0
- A maximum of 32 regions for VHD0
- User-defined region size, minimum size of 32x32 and maximum size of 1920x1080 for VHD0.
- Separate enabling of each region
- User-defined display position of each region on the screen. The position can be set as required by configuring the start and end coordinates of regions.
- Same or different video sources for regions
- User-defined source luminance and chrominance start addresses of regions, 2-byte-aligned
- User-defined source luminance and chrominance stride of regions, 16-byte-aligned.
- Interlaced mode and progressive mode

Display Position

The VDP module allows you to set the video display position.

- The video layer has three sets of coordinates.
- Source start coordinates for reading data. The VDP module is configured with the start address calculated by the CPU.
- Start and end coordinates of the video layer relative to the displayed area
- Display start and end coordinates of the video layer on the screen
- The combination of three sets of coordinates enables video sources to be displayed anywhere on the screen.

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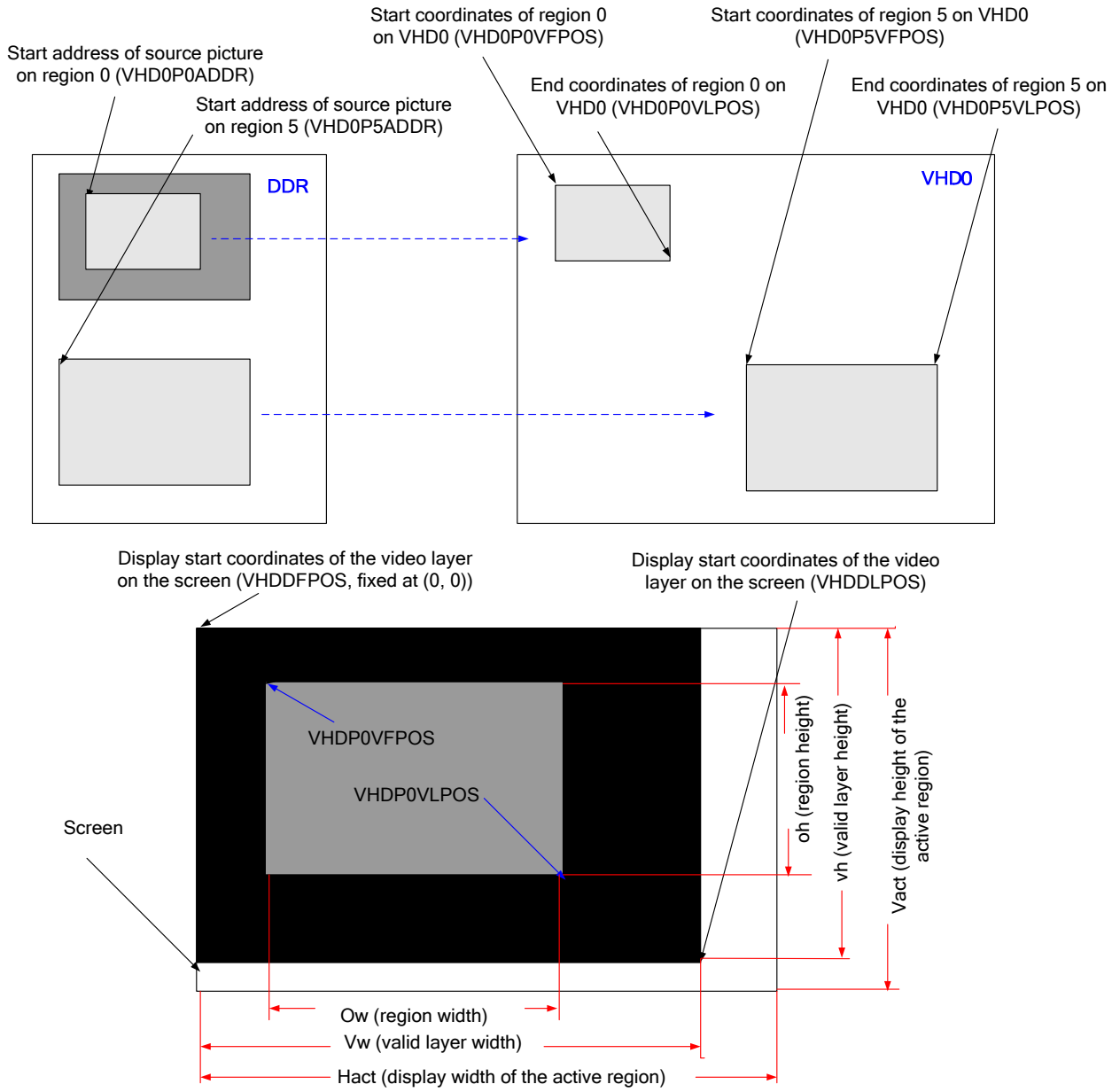
Figure 11-24 Three sets of coordinates



CAUTION

The display start coordinates of the video layer on the screen must be set to (0, 0).

Scaling

The VDP module has a high-performance scaling engine that supports scaling at various ratios. The details are as follows:

- Only VHD0 supports scaling.

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- VHD0 supports only zoom in.
- VHD0 supports luma transient improvement (LTI) and chroma transient improvement (CTI).
- The video formats semi-planar420 and semi-planar422 are supported.
- For VHD0, the minimum input resolution is 32x32 and the maximum input resolution is 1920x1080.
- For VHD0, the minimum output resolution is 32x32 and the maximum output resolution is 1920x1080.
- The filtering mode and replication mode are supported.
- The functions of 8-tap horizontal luminance filtering and 4-tap horizontal chrominance filtering are supported. For each type of filtering, 32 groups of configurable filtering coefficients are provided.
- The functions of 6-tap vertical luminance filtering and 4-tap vertical chrominance filtering are supported. For each type of filtering, 32 groups of configurable filtering coefficients are provided.
- The AXI automatically loads scaling coefficients from the DDR.
- Vertical luminance/chrominance and horizontal luminance/chrominance can be configured separately.
- One pixel is output every one clock cycle.

CAUTION

- Perform vertical scaling before horizontal scaling.
- For VHD0, the picture whose width is between 1280 pixels to 1920 pixels cannot be zoomed in to 1920 pixels.

420-422 (Vertical Chrominance Up Sampling)

When YUV420 data is input, 2x vertical scaling must be performed on the chrominance to convert the data format into YUV422.

As the picture quality of the VHD and VSD is different, the format is converted in different ways.

- The data format of the VHD is converted as follows:
  - 4-tap filtering
  - Replication

  The two modes can be configured.
- The data format of the VSD is converted in replication mode.

IFIR (Horizontal Chrominance Up Sampling)

After horizontal chrominance up sampling, the YUV422 data format is converted into YUV444.

This function can be implemented in three ways:

- Replication

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- Bilinear interpolation
- 8-tap filtering

CSC

- CSC between YUV709 and YUV601
- CSC between RGB and YUV

ACC

- Configurable 256x13 lookup tables
- Maximum resolution of 1920x1080

Adaptive Color Management (ACM)

- Maximum resolution of 1920x1080
- Separate adjustment of four 16x16 UV color units

11.2.3.7 SD Video Layers

The VDP module has multiple SD video layers. The details are as follows:

- SD video layers of VSD0 and VSD1. VSD0 supports a maximum of eight regions, and VSD1 supports only one region.
- Input pixel formats of semi-planar420 and semi-planar422
- Minimum input resolution of 32x32 and maximum input resolution of 720x576
- Minimum output resolution of 32x32 and maximum output resolution of 720x576
- A multiple of 2 for the input horizontal resolution and a multiple of 4 for the input vertical resolution
- Interlaced mode and progressive mode
- User-defined source luminance and chrominance start addresses, 2-byte-aligned
- User-defined source luminance and chrominance stride, 16-byte-aligned
- Optional horizontal chrominance up scaling (IFIR), replication mode, bilinear interpolation, and 6-tap filtering
- CSC from YCbCr to RGB and adjustment of contrast, hue, and saturation
- User-defined display position, anywhere on the screen
- Frame/field update mode
- User-defined global alpha ranging from 0 to 255
- ACC and ACM supported only by VSD0

11.2.3.8 Graphics Layers

The graphics layers include G0, G2, and G3.

Decompression

Only VDP G0 can decompress the pictures that are compressed in lossless mode. The details are as follows:

- Input pixel formats of ARGB1555 and ARGB8888

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- Interlaced compression and progressive compression
- Frame/field update mode
- Minimum input/output resolution 32x32 and maximum input/output resolution 2560x1600 for G0
- Minimum input/output resolution 32x32 and maximum input/output resolution 720x576 for G2 or G3
- A multiple of 2 for the vertical resolution
- User-defined display position, anywhere on the screen
- Separate decompression for four components. The addresses (16-byte-aligned) of four components can be configured and a bankwidth register (16-byte-aligned) and a stride (16-byte-aligned) are shared.
- Decompression performance of 1 pixel/clock
- No compression of the pixel alpha value in ARGB1555 format

The decompression (DCMP) module supports interlaced decompression and progressive decompression. The compressed data is stored in the same way of storing the interlaced and progressive source data. The compression information including the start address, bankwidth and stride needs to be configured. As the alpha, R, G, B components are compressed separately, there are four start addresses corresponding to the four components respectively. The bankwidth is similar to the line in semi-planar storage mode. The difference is that the stored data of a bankwidth may be the compressed data of several component lines. The stride is the same as that in semi-planar storage mode and is used to determine the start address of the compressed data in each line.

Figure 11-25 Progressive decompression storage mode

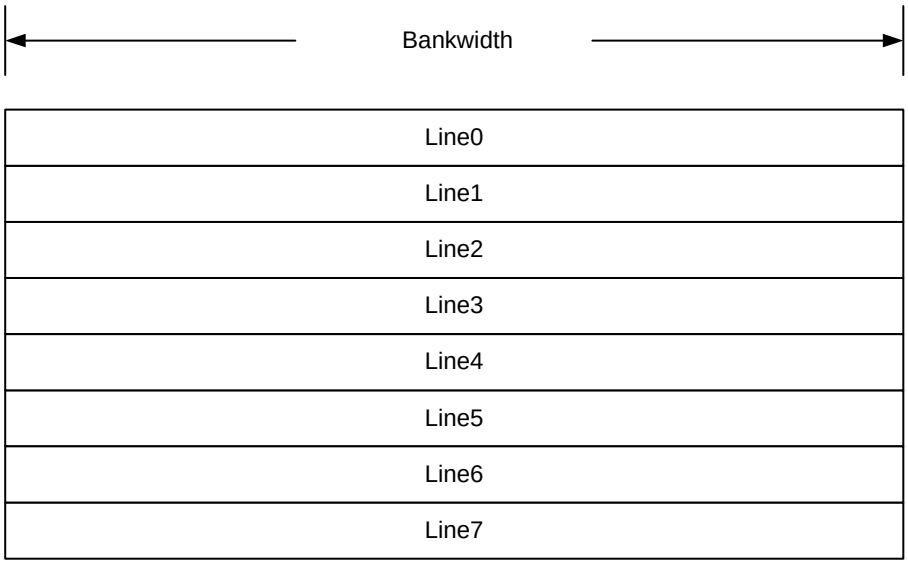

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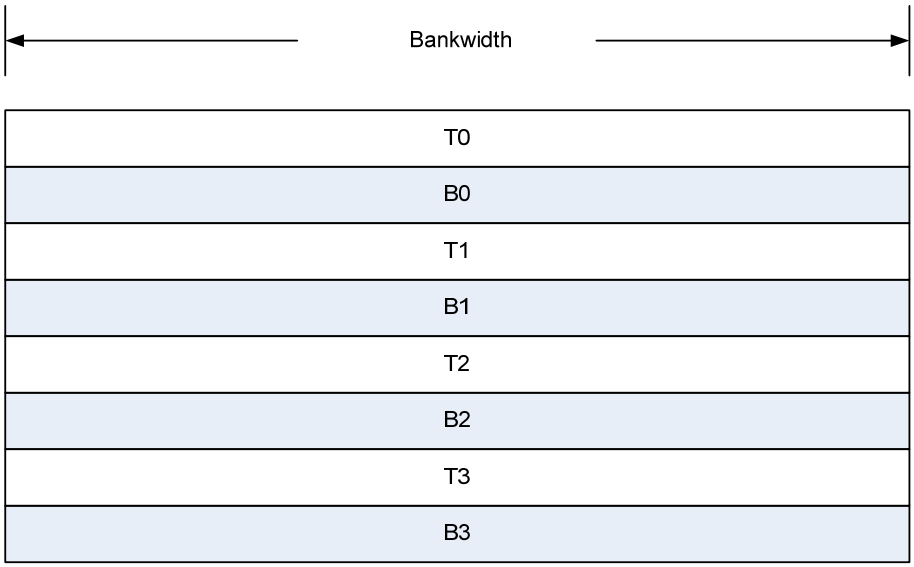
Figure 11-26 Interlaced decompression storage mode



The following describes the decompression configurations in different application scenarios:

- Configurations for progressive decompression, frame update, and frame interrupt
  - Set the graphics layer to the compression mode.
  - Set the base address of four components.
  - Set the bankwidth and stride. Ensure that the strides for compression and decompression are the same, that is, ensure that stride_dcmp is equal to stride_vcmp.
  - Set the graphics layer to the frame update mode.
  - Set the interrupt generation mode to generation by frame.
- Configurations for interlaced decompression, frame update, and frame interrupt
  - Set the graphics layer to the compression mode.
  - Set the bankwidth and stride. Ensure that stride_dcmp is half of stride_vcmp.
  - Set the graphics layer to the frame update mode.
  - Enable interlaced decompression.
- Configurations for interlaced decompression, field update, and field interrupt.
  - Set the graphics layer to the compression mode.
  - Set the bankwidth and stride. Ensure that stride_dcmp is half of stride_vcmp.
  - Set the graphics layer to the field update mode.
  - Set the interrupt generation mode to generation by field and set the start address for storing four components by the top field and bottom field respectively by running the interrupt service routine (ISR).

CSC

The CSCs among RGB, YCbCr601, YCbCr709, xvYCC601, and xvYCC709 are supported.

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Alpha Processing

The alpha value sources of graphics layers are as follows:

- Pixel alpha value: overlay attribute of a pixel
- Global alpha value: overlay attributes of a layer

There is a special case for the pixel alpha value. In RGB1555 format, the alpha value is only one bit. This bit is the index of the alpha value rather than the actual alpha value. The index value is used to select the actual alpha value from the alpha register. When the index value is 0, alpha0 is selected; when the index value is other values, alpha1 is selected.

Premultiplication Format

The premultiplication in ARGB8888 format with pixel α is supported.

HC Layers

The VDP module has one HC layer. The details are as follows:

- Special graphics layers HC0
- Input pixel formats of ARGB1555 and ARGB8888
- Minimum input resolution of 32x32 and maximum input resolution of 128x128
- Minimum output resolution of 32x32 and maximum output resolution is 128x128
- A multiple of 2 for the input vertical resolution
- Interlaced mode and progressive mode
- Frame update and field update
- User-defined source start address, 128-bit-aligned (16-byte-aligned)
- User-defined source stride, 128-bit-aligned (16-byte-aligned)
- CSCs RGB, YCbCr601, YCbCr709, xvYCC601, and xvYCC709
- User-defined display position, anywhere on the screen
- User-defined global alpha ranging from 0 to 255
- Enabling or disabling of the pixel alpha, and alpha0 or alpha1 for the picture in ARGB1555 format with pixel alpha
- Premultiplication in ARGB8888 format with pixel α

CAUTION

- When premultiplication is enabled, the global alpha cannot be 1.
- Premultiplication is unavailable in ARGB1555 format.

11.2.3.9 Layer Overlay

The VDP supports four mixers. The data of the four mixers is output through specific channels. The mapping between mixers and output channel is as follows:

- MIX1 —> DHD0

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- MIX3 —> DSD0
- MIX4 —> DSD1

The binding relationships are as follows:

- VHD0 and G0 are always bound to mixer 1.
- G2 is always bound to mixer 3.
- VSD1 and G3 are always bound to mixer 4.
- HC0 can be bound to mixer 1, mixer 3, or mixer 4.
- VSD0 (PIP) can be bound to mixer 1 or mixer 3.
- The background colors of mixer 1, mixer 3, and mixer 4 can be set separately.

The following configurations are performed:

Step 1 Disable related VO interfaces.

Step 2 Configure sur_attrix to determine the connections of layers.

Step 3 Configure the registers of each layer.

Step 4 Configure the priority of each layer.

Step 5 Enable related VO interfaces.

----End

CAUTION

- If HC0 or VSD0 (PIP) is bound to mixer 1, they cannot be bound to mixer 3, or mixer 4.
- HC0 can be bound only to mixer 1, mixer 3, or mixer 4.
- HC0 and VSD0 (PIP) can drive different mixers. However, the driven mixer cannot be switched in real-time. That is, you must disable related VO interface before changing the mixer driven by the layer.

11.2.3.10 Processing Functions of HD Channels

Timing Configuration

NOTE

- HFB = horizontal front blanking
- HBB = horizontal back blanking
- HACT = horizontal active
- HPW = horizontal pulse width
- VFB = vertical front blanking
- VBB = vertical back blanking
- VACT = vertical active
- VPW = vertical pulse width
- BVFB = bottom vertical front blanking
- BVBB = bottom vertical back blanking

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- BVACT = bottom vertical active
- BVPW = bottom vertical pulse width
- HMID = horizontal middle

The VDP output interfaces support typical and non-typical timings to connect to different interfaces.

- Maximum resolution 1920x1080 for the DHD0 interface
- Interface horizontal timing parameters
  - HFB: 16-bit width, 1–65535 clock cycles
  - HBB: 16-bit width, 1–65535 clock cycles
  - HACT: 16-bit width, 1–65535 clock cycles
  - HPW: 16-bit width, 1–65535 clock cycles
- Interface vertical timing parameters
  - VFB: 8-bit width, 1–256 lines
  - VBB: 8-bit width, 5–256 lines
  - VACT: 12-bit width, 1–256 lines
  - VPW: 16-bit width, 1–65535 lines
- Interlaced timing parameters
  - BVFB: 8-bit width, 1–256 lines
  - BVBB: 8-bit width, 5–256 lines
  - BVACT: 12-bit width, 1–256 lines
  - BVPW: 16-bit width, 1–65535 lines
  - HMID: 16-bit, 1–65535 clock cycles. The clock cycle indicate the clock cycle of a pixel relative to the active region in a line.

CAUTION

- Number of clocks in a line = HFB + HBB + HACT x (n clock/pixel). Note that HDW must be smaller than HBB.
- Number of frames in a line = VFB + VBB + VACT. Note that VPW must be smaller than VBB and BVPW must be smaller than BVBB.
- Interfaces must be disabled before you set all timing parameters.

DFIR

You can determine whether to enable the DFIR function. Typically, the 1,2,1 filtering mode is used and the filtering performance is 1 pixel/clock.

Clip

The VDP provides flexible clip function.

- According to the interface timing protocol, the output data must be within a range. If the data exceeds the range, the data must be clipped.

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- You can determine whether to enable the clip function. The upper and lower limits for clipping can be configured and the clipping performance is 1 pixel/clock.

Gamma Correction

The VDP module supports gamma correction. You can determine whether to enable gamma correction.

11.2.3.11 Processing Functions of SD Channels

The VDP supports two SD channels. The details are as follows:

- SD channels of DSD0 and DSD1
- Maximum resolution 720x576
- CVBS interface supported only by DSD0 and DSD1
- Chrominance down sampling DFIR enable.
- Clip enable..
- User-defined upper and lower limits for clipping

11.2.3.12 Writeback Function of the WBC2 Channel

WBC2 writeback indicates that the data output from DHD0 is written back to the DDR after being scaled. The data acts as the SD input source when the data is displayed in SD and HD modes at the same time.

Progressive and Interlaced Writeback

The progressive and interlaced writeback modes of the VDP module can be configured.

- WBC2 writeback enable.
- Input data format of YUV422. The data of WBC2 is derived from mix 2 of the CBM. When data is input to WBC2, the sampling format of YUV422 is obtained through down sampling.
- Output data formats of semi-planar422 and semi-planar420.
- Progressive writeback and interlaced writeback. The writeback mode depends on DHD0. When DHD0 is in interlaced display mode, WBC2 works in interlaced mode; when DHD0 is in progressive display mode, WBC2 works in progressive mode.
- Input resolution ranging from 32x32 to 1920x1080. The input resolution of WBC2 depends on the valid width and height of DHD0. When DHD0 is in progressive display mode, the input height is the height of a frame; when DHD0 is in progressive mode, the input height is the height of a field.
- Output resolution ranging from 32x32 to 720x576.

WBC2 Scaling

The VDP module supports WBC2 scaling during WBC writeback.

- Only WBC2 zoom-out function is supported.
- The minimum input resolution is 32x32 and the maximum input resolution is 1920x1080 during WBC2 scaling.
- The minimum output resolution is 32x32 and the maximum output resolution is 720x576 during WBC2 scaling.

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- The filtering mode and replication mode are supported.
- The functions of 8-tap horizontal luminance filtering and 4-tap horizontal chrominance filtering are supported. For each type of filtering, 32 groups of configurable filtering coefficients are provided.
- The functions of 6-tap vertical luminance filtering and 4-tap vertical chrominance filtering are supported. For each type of filtering, 32 groups of configurable filtering coefficients are provided.
- The AXI automatically loads scaling coefficients from the DDR.
- Vertical luminance/chrominance and horizontal luminance/chrominance can be configured separately.
- One pixel is output every one clock cycle.

CAUTION

- Perform horizontal scaling before vertical scaling during WBC2 scaling.
- At most 1/16x WBC2 scaling is supported, and the luminance line buffer and chrominance line buffer for scaling are 720 respectively. When SPYCbCr420 data is output, at most 1/8x scaling is supported.

11.2.3.13 Interrupts

The VDP module supports 7 interrupts. The interrupts are classified into:

- Vertical timing interrupt
- Low bandwidth interrupt
- WBC2 interrupt

Vertical Timing Interrupt

The VDP module has one HD channel and two SD channels. Each channel has an independent vertical timing interrupt that indicates the end of a frame or field. Therefore, the VDP module supports three vertical timing interrupts. The positions of generating interrupts can be configured. The details are as follows:

- Interrupt generation modes of generation by frame and by field.
- Mode of generating vertical timing interrupts configured as generation by frame in progressive display mode.
- Mode of generating vertical timing interrupts configured as generation by frame or by field in interlaced display mode. You are advised to set the interrupt generation mode to generation by field for HD and generation by field for SD.
- Configurable interrupt mask.
- Configurable threshold of vertical timing interrupts.
- Separate enabling and disabling of each interrupt source. Writing 1 clears the interrupt.

Low Bandwidth Interrupt

The VDP module has one HD channel and two SD channels. Each channel has an independent low bandwidth interrupt that indicates the low bandwidth information about a

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frame or field. Therefore, the VDP module supports three low bandwidth interrupts. The details are as follows:

- Interrupt generation modes of generation by frame and field.
- Mode of generating vertical timing interrupts configured as generation by frame in progressive display mode.
- Mode of generating vertical timing interrupts configured as generation by frame or by field in interlaced display mode. You are advised to set the interrupt generation mode to generation by field for HD and generation by field for SD.
- Configurable interrupt mask.
- Separate enabling and disabling of each interrupt source. Writing 1 clears the interrupt.

WBC2 Interrupt

The VDP module allows the WBC status to be reported in interrupt mode.

- The VDP has a WBC2 channel. Therefore, the VDP module supports a WBC interrupt that indicates data writeback completion of a frame or field.
- The mode of generating the WBC2 interrupt depends on that of DHD0:
  - If the interrupt generation mode of DHD0 is generation by frame, the interrupt generation mode of WBC2 is generation by frame.
  - If the interrupt generation mode of DHD0 is generation by field, the interrupt generation mode of WBC2 is generation by field.
- Configurable interrupt mask.
- Separate enabling and disabling of the interrupt source. Writing 1 clears the interrupt.

11.2.3.14 Low-Power Control

Dynamic Clock Gating for the Memory

The VDP module supports configurable clock gating:

- The dynamic clock gating of the memory is controlled by using the clock gating signal ck_gate_en.
  - 0: The clock is directly input to the memory.
  - 1: The memory clock is forced to 0.
- All VDP services (including all layers and channels) must be disabled before dynamic clock gating is enabled.

Low-Power Control for the Memory

The low-power control modes for the memory are as follows:

- Normal mode: The memory output valid data normally.
- Retention mode: The memory outputs data as 0.
- Power-down mode: The data output by the memory is in uncertain status.

NOTE

The power-down mode is recommended.

The low-power control for the memory supports separate control of layers and channels.

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- The low-power strategy of the VDP module is implemented by using the low-power function of the memory.
- You can determine whether to enable the low-power mode of the memory and set the low-power mode.
- The low-power of the VDP module is processed by layers and channels. You can determine whether to enable a layer or channel to enter the low-power mode.
- The video layers VHD0 and VSD0–VSD1 support low-power control.
- The graphics layers G0, G2, and G3 support low-power control.
- The cursor layer HC0 supports low-power control.
- The writeback layer WBC2 supports low-power control.
- The channels DHD0 and DSD0–DSD1 support low-power control.
- The PARA module supports low-power control.

The low-power configuration information includes:

- Power-down signal pd_mode. It controls whether the memory enters the power-down status.
- Retention signal retn_mode. It controls whether the memory enters the retention status. When pd_mode is 1, the memory enters the power-down status.
- Timer information and counter. They control whether the memory exits the low-power status.

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11.2.4 Register Summary

Table 11-8 describes the VDP registers.

Table 11-8 Summary of VDP registers (base address: 0x205C_0000)

Offset Address	Register	Description	Page
0x0000	VHDCTRL	VHD control register	11-99
0x0004	VHDUPD	VHD channel update enable register	11-100
0x0010	VHDCADDR	VHD current frame address register	11-100
0x0014	VHDCCADDR	VHD current frame chrominance address register	11-101
0x0024	VHDSTRI DE	VHD surface stride register	11-101
0x0028	VHDIRESO	VHD input resolution register	11-102
0x0034	VHDCBMPARA	VHD overlay parameter register	11-102
0x0050	VHDCTI_CTRL	CTI control register	11-102
0x0054	VHDCHPASS_COEF	Chrominance high-frequency component extraction coefficient register.	11-103
0x0058	VHDCTI_THRE	CTI processing threshold register	11-104
0x005C	VHDLGAIN_COEF	Gain weighted coefficient register for the luminance high-frequency gain segmentation curve	11-104
0x0060	VHDDFPOS	VHD surface start position (in the display window) register	11-104
0x0064	VHDDLPOS	VHD surface end position (in the display window) register	11-105
0x0070	VHDBK	Video layer background color register	11-105
0x0080	VHDCSCIDC	VHD input DC component register for CSC	11-106
0x0084	VHDCSCODC	VHD output DC component register for CSC	11-106
0x0088	VHDCSCP0	VHD CSC parameter 0 register	11-107

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Offset Address	Register	Description	Page
0x008C	VHDCSCP1	VHD CSC parameter 1 register	11-108
0x0090	VHDCSCP2	VHD CSC parameter 2 register	11-108
0x0094	VHDCSCP3	VHD CSC parameter 3 register	11-109
0x0098	VHDCSCP4	VHD CSC parameter 4 register	11-109
0x00A0	VHDACM0	VHD adaptive color management (ACM) control register 0	11-110
0x00A4	VHDACM1	VHD ACM control register 1	11-110
0x00A8	VHDACM2	VHD ACM control register 2	11-111
0x00AC	VHDACM3	VHD ACM control register 3	11-112
0x00B0	VHDACM4	VHD ACM control register 4	11-112
0x00B4	VHDACM5	VHD ACM control register 5	11-113
0x00B8	VHDACM6	VHD ACM control register 6	11-113
0x00BC	VHDACM7	VHD ACM control register 7	11-114
0x00C0	VHDHSP	VHD horizontal scaling parameter register	11-114
0x00C4	VHDHLOFFSET	VHD horizontal luminance offset register	11-115
0x00C8	VHDHCOFFSET	VHD horizontal chrominance offset register	11-115
0x00D8	VHDVSP	VHD vertical scaling parameter register	11-116
0x00DC	VHDVSR	VHD vertical scaling ratio register	11-117
0x00E0	VHDVOFFSET	VHD vertical scaling offset register	11-117
0x00E4	VHDZMEORESO	VHD zoom engine output resolution register	11-118
0x00E8	VHDZMEIRESO	VHD zoom engine input resolution register	11-118
0x00F0	VHDLTI_CTRL	LTI control register	11-119

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Offset Address	Register	Description	Page
0x00F4	VHDLHPASS_COEF	Luminance high-frequency component extraction coefficient register.	11-120
0x00F8	VHDLTI_THRE	LTI processing threshold register	11-120
0x00FC	VHDLHFREQ_THRE	High-frequency component threshold register for the luminance high-frequency gain segmentation curve	11-120
0x0100	VHDACCTHD1	ACC operation threshold 1 register for the VHD channel	11-121
0x0104	VHDACCTHD2	ACC operation threshold 2 register for the VHD channel	11-121
0x0110	VHDACCLOW1	VHD ACC lookup table register 1 for low luminance.	11-122
0x0114	VHDACCLOW2	VHD ACC lookup table register 2 for low luminance.	11-123
0x0118	VHDACCLOW3	VHD ACC lookup table register 3 for low luminance.	11-123
0x0120	VHDACCMED1	VHD ACC lookup table register 1 for medium luminance.	11-124
0x0124	VHDACCMED2	VHD ACC lookup table register 2 for medium luminance.	11-124
0x0128	VHDACCMED3	VHD ACC lookup table register 3 for medium luminance.	11-125
0x0130	VHDACCHIGH1	VHD ACC lookup table register 1 for high luminance.	11-125
0x0134	VHDACCHIGH2	VHD ACC lookup table register 2 for high luminance.	11-126
0x0138	VHDACCHIGH3	VHD ACC lookup table register 3 for high luminance.	11-126
0x0140	VHDACCML1	VHD ACC lookup table register 1 for medium- and low-luminance.	11-127
0x0144	VHDACCML2	VHD ACC lookup table register 2 for medium- and low-luminance.	11-127

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Offset Address	Register	Description	Page
0x0148	VHDACCML3	VHD ACC lookup table register 3 for medium- and low-luminance.	11-128
0x0150	VHDACCMH1	VHD ACC lookup table register 1 for medium- and high-luminance.	11-128
0x0154	VHDACCMH2	VHD ACC lookup table register 2 for medium- and high-luminance.	11-129
0x0158	VHDACCMH3	VHD ACC lookup table register 3 for medium- and high-luminance.	11-129
0x0160	VHDACC3LOW	Low-threshold luminance statistical value register for three ACC regions	11-130
0x0164	VHDACC3MED	Medium-threshold luminance statistical value register for three ACC regions	11-130
0x0168	VHDACC3HIGH	High-threshold luminance statistical value register for three ACC regions	11-130
0x016C	VHDACC8MLOW	Low-threshold luminance statistical value register after the ACC middle region is divided into eight segments	11-131
0x0170	VHDACC8MHIGH	High-threshold luminance statistical value register after the ACC middle region is divided into eight segments	11-131
0x0174	VHDACCTOTAL	ACC pixel statistical value register	11-132
0x0180	VHDIFIRCOEF01	VHD IFIR filtering coefficients 0–1 register	11-132
0x0184	VHDIFIRCOEF23	VHD IFIR filtering coefficients 2–3 register	11-132
0x0188	VHDIFIRCOEF45	VHD IFIR filtering coefficients 4–5 register	11-133
0x018C	VHDIFIRCOEF67	VHD IFIR filtering coefficients 6–7 register	11-133
0x0400 + m x 0x20	VHDPmRESO	VHD region m resolution register	11-134

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Offset Address	Register	Description	Page
0x0404 + m x 0x20	VHDPmLADDR	VHD region m luminance address register	11-134
0x0408 + m x 0x20	VHDPmCADDR	VHD region m chrominance address register	11-135
0x040C + m x 0x20	VHDPmSTRIDE	VHD region m stride register	11-135
0x0410 + m x 0x20	VHDPmVFPOS	VHD region m video start position register	11-136
0x0414 + m x 0x20	VHDPmVLPOS	VHD region m video end position register	11-136
0x0C00	VHD64REGIONENH	VHD regions 32–63 enable register	错误！未定义书签。
0x0C04	VHD64REGIONENL	VHD regions 0–31 enable register	11-137
0x3000 + i x 0x1000	VSDiCTRL	VSD control register	11-139
0x3004 + i x 0x1000	VSDiUPD	VSD channel update enable register	11-140
0x3010 + i x 0x1000	VSDiCADDR	VSD current frame address register	11-141
0x3014 + i x 0x1000	VSDiCCADDR	VSD current frame chrominance address register	11-141
0x3024 + i x 0x1000	VSDiSTRIDE	VSD surface stride register	11-142
0x3028 + i x 0x1000	VSDiIRESO	VSD input resolution register	11-142
0x3034 + i x 0x1000	VSDiCBMPARA	VSD overlay parameter register	11-143
0x3060 + i x 0x1000	VSDiDFPOS	VSD surface start position (in the display window) register	11-143
0x3064 + i x 0x1000	VSDiDLPOS	VSD surface end position (in the display window) register	11-144
0x3070 + i x 0x1000	VSDIBK	Video layer background color register	11-144
0x3080 + i x 0x1000	VSDiCSCIDC	VSD input DC component register for CSC	11-145
0x3084 + i x 0x1000	VSDiCSCODC	VSD output DC component register for CSC	11-146
0x3088 + i x 0x1000	VSDiCSCP0	VSD CSC parameter 0 register	11-146

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Offset Address	Register	Description	Page
0x308C + i x 0x1000	VSDiCSCP1	VSD CSC parameter 1 register	11-147
0x3090 + i x 0x1000	VSDiCSCP2	VSD CSC parameter 2 register	11-147
0x3094 + i x 0x1000	VSDiCSCP3	VSD CSC parameter 3 register	11-148
0x3098 + i x 0x1000	VSDiCSCP4	VSD CSC parameter 4 register	11-149
0x30A0 + i x 0x1000	VSDIACM0	VSD ACM control register 0	11-149
0x30A4 + i x 0x1000	VSDIACM1	VSD ACM control register 1	11-150
0x30A8 + i x 0x1000	VSDIACM2	VSD ACM control register 2	11-150
0x30AC + i x 0x1000	VSDIACM3	VSD ACM control register 3	11-151
0x30B0 + i x 0x1000	VSDIACM4	VSD ACM control register 4	11-151
0x30B4 + i x 0x1000	VSDIACM5	VSD ACM control register 5	11-152
0x30B8 + i x 0x1000	VSDIACM6	VSD ACM control register 6	11-152
0x30BC + i x 0x1000	VSDIACM7	VSD ACM control register 7	11-153
0x3100 + i x 0x1000	VSDIACCTHD1	ACC operation threshold 1 register for the VSD channel	11-153
0x3104 + i x 0x1000	VSDIACCTHD2	ACC operation threshold 2 register for the VSD channel	11-154
0x3110 + i x 0x1000	VSDIACCLOW1	VSD ACC lookup table register 1 for low luminance.	11-155
0x3114 + i x 0x1000	VSDIACCLOW2	VSD ACC lookup table register 2 for low luminance.	11-155
0x3118 + i x 0x1000	VSDIACCLOW3	VSD ACC lookup table register 3 for low luminance.	11-156
0x3120 + i x 0x1000	VSDIACCMED1	VSD ACC lookup table register 1 for medium luminance.	11-156
0x3124 + i x 0x1000	VSDIACCMED2	VSD ACC lookup table register 2 for medium luminance.	11-157
0x3128 + i x 0x1000	VSDIACCMED3	VSD ACC lookup table register 3 for medium luminance.	11-157
0x3130 + i x 0x1000	VSDIACCHIGH1	VSD ACC lookup table register 1 for high luminance.	11-158

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Offset Address	Register	Description	Page
0x3134 + i x 0x1000	VSDIACCHIGH2	VSD ACC lookup table register 2 for high luminance.	11-158
0x3138 + i x 0x1000	VSDIACCHIGH3	VSD ACC lookup table register 3 for high luminance.	11-159
0x3140 + i x 0x1000	VSDIACCML1	VSD ACC lookup table register 1 for medium- and low-luminance	11-159
0x3144 + i x 0x1000	VSDIACCML2	VSD ACC lookup table register 2 for medium- and low-luminance	11-160
0x3148 + i x 0x1000	VSDIACCML3	VSD ACC lookup table register 3 for medium- and low-luminance.	11-160
0x3150 + i x 0x1000	VSDIACCMH1	VSD ACC lookup table register 1 for medium- and high-luminance.	11-161
0x3154 + i x 0x1000	VSDIACCMH2	VSD ACC lookup table register 2 for medium- and high-luminance.	11-161
0x3158 + i x 0x1000	VSDIACCMH3	VSD ACC lookup table register 3 for medium- and high-luminance.	11-162
0x3160 + i x 0x1000	VSDIACC3LOW	Low-threshold luminance statistical value register for three ACC regions	11-163
0x3164 + i x 0x1000	VSDIACC3MED	Medium-threshold luminance statistical value register for three ACC regions	11-163
0x3168 + i x 0x1000	VSDIACC3HIGH	High-threshold luminance statistical value register for three ACC regions	11-163
0x316C + i x 0x1000	VSDIACC8MLOW	Low-threshold luminance statistical value register after the ACC middle region is divided into eight segments	11-164
0x3170 + i x 0x1000	VSDIACC8MHIGH	High-threshold luminance statistical value register after the ACC middle region is divided into eight segments	11-164
0x3174 + i x 0x1000	VSDIACCTOTAL	ACC pixel statistical value register	11-165

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Offset Address	Register	Description	Page
0x3180 + i x 0x1000	VSDiIFIRCOEF01	VSD IFIR filtering coefficients 0–1 register	11-165
0x3184 + i x 0x1000	VSDiIFIRCOEF23	VSD IFIR filtering coefficients 2–3 register	11-166
0x3188 + i x 0x1000	VSDiIFIRCOEF45	VSD IFIR filtering coefficients 4–5 register	11-166
0x318C + i x 0x1000	VSDiIFIRCOEF67	VSD IFIR filtering coefficients 6–7 register	11-167
0x3400 + i x 0x1000 ＋m x 0x20	VSDiP0RESO	VSD region m resolution register	11-167
0x3404 + i x 0x1000 ＋m x 0x20	VSDiPMLADDR	VSD region m address register	11-168
0x3408 + i x 0x1000 ＋m x 0x20	VSDiPMCADDR	VSD region m chrominance address register	11-168
0x340C + i x 0x1000 ＋m x 0x20	VSDiPMSTRIDE	VSD region m stride register	11-168
0x3410 + i x 0x1000 + m x 0x20	VSDiPMVFPOS	VSD region m video start position register	11-169
0x3414 + i x 0x1000 + m x 0x20	VSDiPMVLPOS	VSD region m video end position register	11-169
0x3C04 + i x 0x1000 + m x 0x20	VSDi16REGIONEN	VSD 16 region enable register	11-170
0x8200	WBC2CTRL	WBC2 control register	11-171
0x8204	WBC2UPD	WBC2 channel update enable register	11-172
0x8208	WBC2ADDR	WBC2 capture address register	11-172
0x820C	WBC2STRIDE	Capture stride register	11-173
0x8210	WBC2ORESO	Output resolution register	11-173
0x8220	WBC2CADDR	WBC2 capture write chrominance address register	11-174
0x8224	WBC2CSTRIDE	WBC2 capture chrominance stride register	11-174
0x82C0	WBC2HSP	WBC2 horizontal scaling parameter register	11-174
0x82C4	WBC2HLOFFSET	WBC2 horizontal luminance offset register	11-175

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Offset Address	Register	Description	Page
0x82C8	WBC2HCOFFSET	WBC2 horizontal chrominance offset register	11-176
0x82D8	WBC2VSP	WBC2 vertical scaling parameter register	11-176
0x82DC	WBC2VSR	WBC2 vertical scaling ratio register	11-178
0x82E0	WBC2VOFFSET	WBC2 vertical luminance offset register	11-178
0x82E4	WBC2ZMEORESO	WBC2 zoom engine output resolution register	11-179
0x82E8	WBC2ZMEIRESO	WBC2 zoom engine input resolution register	11-179
0x9000	G0CTRL	G0 control register	11-180
0x9004	G0UPD	G0 update enable register	11-181
0x9008	G0ADDR	G0 address register	11-181
0x900C	G0STRIDE	G0 stride register	11-182
0x9010	G0CBMPARA	G0 overlay parameter register	11-182
0x9014	G0CKEYMAX	G0 maximum colorkey register	11-183
0x9018	G0CKEYMIN	G0 minimum colorkey register	11-183
0x901C	G0CMASK	G0 colorkey mask value register	11-183
0x9020	G0IRESO	G0 input resolution register	11-184
0x9024	G0ORESO	G0 output resolution register	11-184
0x902C	G0DFPOS	G0 surface start position (in the display window) register	11-185
0x9030	G0DLPOS	G0 surface end position (in the display window) register	11-185
0x90A0	G0CSCIDC	G0 input DC component register for CSC	11-186
0x90A4	G0CSCODC	G0 output DC component register for CSC	11-186
0x90A8	G0CSCP0	G0 CSC parameter 0 register	11-187
0x90AC	G0CSCP1	G0 CSC parameter 1 register	11-188
0x90B0	G0CSCP2	G0 CSC parameter 2 register	11-188

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Offset Address	Register	Description	Page
0x90B4	G0CSCP3	G0 CSC parameter 3 register	11-189
0x90B8	G0CSCP4	G0 CSC parameter 4 register	11-189
0x91B4	G0DCMPBANKWIDTH	G0 compressed data bank width register	11-190
0x91B8	G0DCMPSTRIDE	G0 compressed data stride register	11-190
0x91BC	G0DCMPAADDR	G0 compressed data start address register of A component	11-190
0x91C0	G0DCMPRADDR	G0 compressed data start address register of R component	11-191
0x91C4	G0DCMPGADDR	G0 compressed data start address register of G component	11-191
0x91C8	G0DCMPBADDR	G0 compressed data start address register of B component	11-191
0x9400	G2CTRL	G2 control register	11-192
0x9404	G2UPD	G2 update enable register	11-193
0x9408	G2ADDR	G2 address register	11-193
0x940C	G2STRIDE	G2 stride register	11-194
0x9410	G2CBMPARA	G2 overlay parameter register	11-194
0x9414	G2CKEYMAX	G2 maximum colorkey register	11-195
0x9418	G2CKEYMIN	G2 minimum colorkey register	11-195
0x941C	G2CMASK	G2 colorkey mask value register	11-196
0x9420	G2IRESO	G2 input resolution register	11-196
0x9424	G2ORESO	G2 output resolution register	11-197
0x942C	G2DFPOS	G2 surface start position (in the display window) register	11-197
0x9430	G2DLPOS	G2 surface end position (in the display window) register	11-198
0x94A0	G2CSCIDC	G2 input DC component register for CSC	11-198

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Offset Address	Register	Description	Page
0x94A4	G2CSCODC	G2 output DC component register for CSC	11-199
0x94A8	G2CSCP0	G2 CSC parameter 0 register	11-200
0x94AC	G2CSCP1	G2 CSC parameter 1 register	11-200
0x94B0	G2CSCP2	G2 CSC parameter 2 register	11-201
0x94B4	G2CSCP3	G2 CSC parameter 3 register	11-201
0x94B8	G2CSCP4	G2 CSC parameter 4 register	11-202
0x9600	G3CTRL	G3 control register	11-202
0x9604	G3UPD	G3 update enable register	11-204
0x9608	G3ADDR	G3 address register	11-204
0x960C	G3STRIDE	G3 stride register	11-204
0x9610	G3CBMPARA	G3 overlay parameter register	11-205
0x9614	G3CKEYMAX	G3 maximum colorkey register	11-206
0x9618	G3CKEYMIN	G3 minimum colorkey register	11-206
0x961C	G3CMASK	G3 colorkey mask value register	11-206
0x9620	G3IRESO	G3 input resolution register	11-207
0x9624	G3ORESO	G3 output resolution register	11-207
0x962C	G3DFPOS	G3 surface start position (in the display window) register	11-208
0x9630	G3DLPOS	G3 surface end position (in the display window) register	11-208
0x96A0	G3CSCIDC	G3 input DC component register for CSC	11-209
0x96A4	G3CSCODC	G3 output DC component register for CSC	11-209
0x96A8	G3CSCP0	G3 CSC parameter 0 register	11-210
0x96AC	G3CSCP1	G3 CSC parameter 1 register	11-211
0x96B0	G3CSCP2	G3 CSC parameter 2 register	11-211
0x96B4	G3CSCP3	G3 CSC parameter 3 register	11-212
0x96B8	G3CSCP4	G3 CSC parameter 4 register	11-212
0x9A00	HCCTRL	HC control register	11-213

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Offset Address	Register	Description	Page
0x9A04	HCUPD	HC update enable register	11-214
0x9A08	HCADDR	HC address register	11-214
0x9A0C	HCSTRIDE	HC stride register	11-215
0x9A10	HCCBMPARA	HC overlay parameter register	11-215
0x9A14	HCCKEYMAX	HC maximum colorkey register	11-216
0x9A18	HCCKEYMIN	HC minimum colorkey register	11-216
0x9A1C	HCCMASK	HC colorkey mask register	11-217
0x9A20	HCIRESO	HC input resolution register	11-217
0x9A2C	HCDFPOS	HC surface start position (in the display window) register	11-218
0x9A30	HCDLPOS	HC surface end position (in the display window) register	11-218
0x9AA0	HCCSCIDC	HC input DC component register for CSC	11-218
0x9AA4	HCCSCODC	HC output DC component register for CSC	11-219
0x9AA8	HCCSCP0	HC CSC parameter 0 register	11-220
0x9AAC	HCCSCP1	HC CSC parameter 1 register	11-220
0x9AB0	HCCSCP2	HC CSC parameter 2 register	11-221
0x9AB4	HCCSCP3	HC CSC parameter 3 register	11-221
0x9AB8	HCCSCP4	HC CSC parameter 4 register	11-222
0x9E00	CBMBKG1	HD0 overlay background color register	11-222
0x9E04	CBMBKG2	HD1 overlay background color register	11-223
0x9E08	CBMBKG3	SD0 overlay background color register	11-223
0x9E0C	CBMBKG4	SD1 overlay background color register	11-224
0x9E10	CBMATTR	Crossbar configuration register	11-224
0x9E14	CBMMIX1	Mixer 1 priority configuration register	11-225

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Offset Address	Register	Description	Page
0x9E18	CBMMIX2	Mixer 2 priority configuration register	11-227
0x9E1C	CBMMIX3	Mixer 3 priority configuration register	11-229
0x9E20	CBMMIX4	Mixer 4 priority configuration register	11-231
0xA000	DHDCTRL	DHD global control register	11-232
0xA004	DHDVSYNC	DHD vertical timing register	11-235
0xA008	DHDHSYNC1	DHD horizontal timing register 1	11-235
0xA00C	DHDHSYNC2	DHD horizontal timing register 2	11-236
0xA010	DHDVPLUS	DHD interlaced bottom vertical timing register	11-237
0xA014	DHDPWR	DHD sync signal pulse with register	11-237
0xA01C	DHDVTTHD	DHD vertical timing threshold register	11-238
0xA040	DHDCLIPL	DHD clip lower threshold register	11-239
0xA044	DHDCLIPH	DHD clip upper threshold register	11-239
0xA0F0	DHDSTATE	DHD status register	11-240
0xA800	DSDCTRL	DSD global control register	11-241
0xA804	DSDVSYNC	DSD vertical timing register	11-242
0xA808	DSDHSYNC1	DSD horizontal timing register 1	11-243
0xA80C	DSDHSYNC2	DSD horizontal timing register 2	11-243
0xA810	DSDVPLUS	DSD interlaced bottom vertical timing register	11-244
0xA814	DSDPWR	DSD sync signal pulse width register	11-245
0xA81C	DSDVTTHD	DSD vertical timing threshold register	11-246
0xA840	DSDCLIPL	DSD clip lower threshold register	11-246

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Offset Address	Register	Description	Page
0xA844	DSDCLIPH	DSD clip upper threshold register	11-247
0xA8F0	DSDSTATE	DSD status register	11-248
0xAC00	DSD1CTRL	DSD1 global control register	11-248
0xAC04	DSD1VSYNC	DSD1 vertical timing register	11-250
0xAC08	DSD1HSYNC1	DSD1 horizontal timing register 1	11-250
0xAC0C	DSD1HSYNC2	DSD1 horizontal timing register 2	11-251
0xAC10	DSD1VPLUS	DSD1 bottom vertical sync timing register in interlaced output mode	11-252
0xAC14	DSD1PWR	DSD1 sync signal pulse width register	11-252
0xAC1C	DSD1VTTHD	DSD1 vertical timing threshold register	11-253
0xAC40	DSD1CLIPL	DSD1 clip lower threshold register	11-254
0xAC44	DSD1CLIPH	DSD1 clip upper threshold register	11-254
0xACF0	DSD1STATE	DSD1 status register	11-255
0xC200	DATE_COEFF0	DATE norm parameter configuration register	11-256
0xC204	DATE_COEFF1	DATE amplitude configuration register	11-259
0xC21C	DATE_COEFF7	DATE teletext configuration register	11-260
0xC220	DATE_COEFF8	DATE teletext configuration register	11-263
0xC224	DATE_COEFF9	DATE teletext configuration register	11-264
0xC228	DATE_COEFF10	DATE teletext configuration register	11-264
0xC22C	DATE_COEFF11	DATE closed caption configuration register	11-265
0xC230	DATE_COEFF12	DATE closed caption configuration register	11-266

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Offset Address	Register	Description	Page
0xC234	DATE_COEFF13	DATE CGMS configuration register	11-266
0xC238	DATE_COEFF14	DATE CGMS configuration register	11-267
0xC23C	DATE_COEFF15	DATE WSS configuration register	11-267
0xC240	DATE_COEFF16	DATE VPS configuration register	11-268
0xC244	DATE_COEFF17	DATE VPS configuration register	11-269
0xC248	DATE_COEFF18	DATE VPS configuration register	11-269
0xC24C	DATE_COEFF19	DATE VPS configuration register	11-269
0xC250	DATE_COEFF20	DATE teletext configuration register	11-270
0xC254	DATE_COEFF21	DATE output matrix control register	11-271
0xC258	DATE_COEFF22	DATE discrete time oscillator (DTO) initial phase configuration register	11-273
0xC25C	DATE_COEFF23	DATE video output delay configuration register	11-273
0xC280	DATE_ISRMASK	DATE interrupt mask register	11-275
0xC284	DATE_ISRSTATE	DATE interrupt status register	11-275
0xC288	DATE_ISR	DATE interrupt register	11-275
0xC400	DATE1_COEFF0	DATE1 norm parameter configuration register	11-277
0xC404	DATE1_COEFF1	DATE1 amplitude configuration register	11-280
0xC41C	DATE1_COEFF7	DATE1 teletext configuration register	11-281
0xC420	DATE1_COEFF8	DATE1 teletext configuration register	11-284
0xC424	DATE1_COEFF9	DATE1 teletext configuration register	11-285
0xC428	DATE1_COEFF10	DATE1 teletext configuration register	11-285

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Offset Address	Register	Description	Page
0xC42C	DATE1_COEFF11	DATE1 closed caption configuration register	11-286
0xC430	DATE1_COEFF12	DATE1 closed caption configuration register	11-287
0xC434	DATE1_COEFF13	DATE1 CGMS configuration register	11-287
0xC438	DATE1_COEFF14	DATE1 CGMS configuration register	11-288
0xC43C	DATE1_COEFF15	DATE1 WSS configuration register	11-288
0xC440	DATE1_COEFF16	DATE1 VPS configuration register	11-289
0xC444	DATE1_COEFF17	DATE1 VPS configuration register	11-290
0xC448	DATE1_COEFF18	DATE1 VPS configuration register	11-290
0xC44C	DATE1_COEFF19	DATE1 VPS configuration register	11-290
0xC450	DATE1_COEFF20	DATE1 teletext configuration register	11-291
0xC454	DATE1_COEFF21	DATE1 output matrix control register	11-292
0xC458	DATE1_COEFF22	DATE1 DTO initial phase configuration register	11-294
0xC45C	DATE1_COEFF23	DATE1 video output delay configuration register	11-294
0xC480	DATE1_ISRMASK	DATE1 interrupt mask register	11-296
0xC484	DATE1_ISRSTATE	DATE1 interrupt status register	11-296
0xC488	DATE1_ISR	DATE1 interrupt register	11-296
0xC490	DATE1_VERSION	DATE1 version register	11-297
0xCE00	VOCTRL	VO control register	11-298
0xCE04	VOINTSTA	VO interrupt status register	11-299
0xCE08	VOMSKINTSTA	VO masked interrupt status register	11-301
0xCE0C	VOINTMSK	VDP interrupt mask register	11-303

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Offset Address	Register	Description	Page
0xCE10	VOUVERSION1	VDP version register 1	11-305
0xCE14	VOUVERSION2	VDP version register 2	11-305
0xCE18	VOMUXDATA	VO interface multiplexing data register (VOPINTEST)	11-305
0xCE1C	VOMUX	VO interface multiplexing register	11-305
0xCE24	VGACSCIDC	VGA input DC component register for CSC	11-308
0xCE28	VGACSCODC	VGA output DC component register for CSC	11-309
0xCE2C	VGACSCP0	VGA CSC parameter 0 register	11-309
0xCE30	VGACSCP1	VGA CSC parameter 1 register	11-310
0xCE34	VGACSCP2	VGA CSC parameter 2 register	11-310
0xCE38	VGACSCP3	VGA CSC parameter 3 register	11-311
0xCE3C	VGACSCP4	VGA CSC parameter 4 register	11-311
0xCE40	VOPARAUP	Scaling/gamma/ACC coefficient update enable register	11-312
0xCE44	VHDHCOEFAD	VHD horizontal luminance and chrominance filtering coefficient address register	11-314
0xCE48	VHDVCOEFAD	VHD vertical luminance and horizontal chrominance filtering coefficient address register	11-314
0xCE54	ACCAD	ACC coefficient lookup table address register of the video channel	11-315
0xCE58	WBC2HCOEFAD	WBC2 horizontal luminance and chrominance filtering coefficient address register	11-315
0xCE5C	WBC2VCOEFAD	WBC2 vertical luminance and horizontal chrominance filtering coefficient address register	11-316

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Offset Address	Register	Description	Page
0xCE78	DHDGAMMAAD	DHD gamma correction coefficient address register	11-316
0xCEE0	DACCTRL0_2	DAC0–2 control register	11-316
0xCEE4	DACCTRL3_5	DAC3–5 control register	11-318
0xCEE8	DACSTAT0_2	DAC0–2 status register	11-319
0xCEEC	DACSTAT3_5	DAC3–5 status register	11-320
0xCEF0	DACBANDGAP	Band gap test register	11-320
0xCEF4	VOLPTIMER	Low-power timer register	11-321
0xCEF8	VOLPMODE0	Low-power mode register 0	11-321
0xCEFC	VOLPMODE1	Low-power mode register 1	11-324
0xD000–0xD10C	VHDHLCOEF	VHD horizontal luminance scaling/filtering coefficient register	11-325
0xD200–0xD284	VHDHCCOEF	VHD horizontal chrominance scaling/filtering coefficient register	11-326
0xD400–0xD50C	VHDVLCOEF	VHD vertical luminance scaling/filtering coefficient register	11-327
0xD600–0xD684	VHDVCCOEF	VHD vertical chrominance scaling/filtering coefficient register	11-328
0xE000–0xE10C	WBCHLCOEF	WBC horizontal luminance scaling/filtering coefficient register	11-328
0xE200–0xE284	WBCHCCOEF	WBC horizontal chrominance scaling/filtering coefficient register	11-329
0xE400–0xE50C	WBCVLCOEF	WBC vertical luminance scaling/filtering coefficient register	11-330
0xE600–0xE684	WBCVCCOEF	WBC vertical chrominance scaling/filtering coefficient register	11-331
0xE800–0xE880	DHDGAMMAN	DHD gamma lookup table coefficient register	11-332
0xF000–0xF040	VHDHLTICOEF	VHD horizontal luma transient improvement (HLTI) filtering coefficient register	11-332

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Offset Address	Register	Description	Page
0xF100–0xF140	VHDHCTICOEF	VHD horizontal chroma transient improvement (HCTI) filtering coefficient register	11-333
0xF200–0xF240	VHDVLTICOEF	VHD vertical luma transient improvement (VLTI) filtering coefficient register	11-333
0xF300–0xF340	VHDVCTICOEF	VHD vertical chroma transient improvement (VCTI) filtering coefficient register	11-334

Table 11-9 describes the value ranges and meanings of the variables in the offset addresses of VDP registers.

Table 11-9 Variables in the offset addresses of VDP registers

Variable	Value Range	Description
i	0, 1	VSD 0–1
m	0–31	HD video layer region ID
	0–7 (i = 0)	SD video layer region ID
	0 (i = 1)	SD video layer region ID

11.2.5 Register Description

VHDCTRL

VHDCTRL is a VHD control register (non-instant register). It is used to configure the layer information

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Offset Address	Register Name	Total Reset Value
0x0000	VHDCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_en	reserved											ifir_mode		vup_mode		reserved												ifmt			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	surface_en	Surface enable (non-instant field). 0: disabled 1: enabled
[30:20]	-	reserved	Reserved.
[19:18]	RW	ifir_mode	Horizontal chrominance IFIR mode. 00: reserved 01: chrominance IFIR copy mode 10: bilinear interpolation 11: 6-tap FIR
[17]	-	vup_mode	Register update mode. 0: update by field 1: update by frame
[16:4]	-	reserved	Reserved.
[3:0]	RW	ifmt	Input data format. 0x3: SPYCbCr420 0x4: SPYCbCr422 Other values: reserved

VHDUPD

VHDUPD is a VHD channel update enable register.

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Offset Address	Register Name	Total Reset Value
0x0004	VHDUPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After updates, this bit is cleared automatically by the hardware.

VHDCADDR

VHDCADDR is a VHD current frame address register. In package pixel format, the address is the address of the frame buffer; in semi-planar pixel format, the address is the address of the luminance frame buffer.

Offset Address	Register Name	Total Reset Value
0x0010	VHDCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_caddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_caddr	Address of the current frame.

VHDCCADDR

VHDCCADDR is a VHD current frame chrominance address register. In package pixel format, the address is invalid; in semi-planar pixel format, the address is the address of the luminance frame buffer.

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Offset Address	Register Name	Total Reset Value
0x0014	VHDCCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_ccaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_ccaddr	Chrominance address of the current frame.

VHDSTRIDE

VHDSTRIDE is a VHD surface stride register.

Offset Address	Register Name	Total Reset Value
0x0024	VHDSTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_cstride																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	surface_cstride	Stride of the chrominance frame buffer (valid in semi-planar format), 128-bit alignment.
[15:0]	RW	surface_stride	Stride of the frame buffer (valid in semi-planar format, luminance stride), 128-bit alignment.

VHDIRESO

VHDIRESO is a VHD input resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x0028	VHDIRESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ih												iw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	ih	Height (in line). The value is the actual height minus 1. The frame height is referenced.

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[11:0]	RW	iw	Width (in pixel). The value is the actual width minus 1.

VHDCBMPARA

VHDCBMPARA is a VHD overlay parameter register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x0034	VHDCBMPARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								galpha							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	galpha	Overlay global alpha value. The value ranges from 0 to 128. The value 128 indicates opaque, and the value 0 indicates full transparent.

VHDCTI_CTRL

VHDCTI_CTRL is a CTI control register.

Offset Address	Register Name	Total Reset Value
0x0050	VHDCTI_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cti_en	reserved			cgain_ratio												reserved	cmixing_ratio							reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	**Access**	**Name**	**Description**
[31]	RW	cti_en	CTI enable. 0: disabled 1: enabled
[30:28]	RO	reserved	Reserved.
[27:16]	RW	cgain_ratio	Chrominance gain coefficient.
[15]	RO	reserved	Reserved.
[14:8]	RW	cmixing_ratio	Weighted chrominance mixing coefficient.

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[7:0]	RO	reserved	Reserved.

VHDCHPASS_COEF

VHDCHPASS_COEF is a chrominance high-frequency component extraction coefficient register.

Offset Address	Register Name	Total Reset Value
0x0054	VHDCHPASS_COEF	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		chpass_coef2		chpass_coef1		chpass_coef0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RW	chpass_coef2	Chrominance high-frequency component extraction coefficient 2.
[15:8]	RW	chpass_coef1	Chrominance high-frequency component extraction coefficient 1.
[7:0]	RW	chpass_coef0	Chrominance high-frequency component extraction coefficient 0.

VHDCTI_THRE

VHDCTI_THRE is a CTI processing threshold register.

Offset Address	Register Name	Total Reset Value
0x0058	VHDCTI_THRE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	ccoring_thre				cswing_thre			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	ccoring_thre	Chrominance coring threshold.
[15:0]	RW	cswing_thre	Chrominance swing threshold.

VHDLGAIN_COEF

VHDLGAIN_COEF is a gain weighted coefficient register for the luminance high-frequency gain segmentation curve.

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Offset Address	Register Name	Total Reset Value
0x005C	VHDLGAIN_COEF	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		lgain_coef2		lgain_coef1		lgain_coef0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RW	lgain_coef2	Gain weighted coefficient 2 for the luminance high-frequency gain segmentation curve.
[15:8]	RW	lgain_coef1	Gain weighted coefficient 1 for the luminance high-frequency gain segmentation curve.
[7:0]	RW	lgain_coef0	Gain weighted coefficient 0 for the luminance high-frequency gain segmentation curve.

VHDDFPOS

VHDDFPOS is a VHD surface start position (in the display window) register (non-instant register). The start position is in the unit of pixel.

Offset Address	Register Name	Total Reset Value
0x0060	VHDDFPOS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		disp_yfpos			disp_xfpos		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	disp_yfpos	Start coordinates of the display column. The frame height is referenced and the unit is line.
[11:0]	RW	disp_xfpos	Start coordinates of the display row.

VHDDLPOS

VHDDLPOS is VHD surface end position (in the display window) register (non-instant register). The end position is in the unit of pixel.

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Offset Address	Register Name	Total Reset Value
0x0064	VHDDLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_ylpos												disp_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	disp_ylpos	End coordinates of the display column. The frame height is referenced and the unit is line.
[11:0]	RW	disp_xlpos	End coordinates of the display row.

VHDBK

VHDBK is a video layer background color register.

Offset Address	Register Name	Total Reset Value
0x0070	VHDBK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vbk_alpha								vbk_y								vbk_cb								vbk_cr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	**Access**	**Name**	**Description**
[31:24]	RW	vbk_alpha	Levels 0–128 of the background filling color of the video layer.
[23:16]	RW	vbk_y	Y component.
[15:8]	RW	vbk_cb	Cb component.
[7:0]	RW	vbk_cr	Cr component.

VHDCSCIDC

VHDCSCIDC is a VHD input DC component register for CSC (instant register).

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Offset Address	Register Name	Total Reset Value
0x0080	VHDCSCIDC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				csc_en	cscidc2											cscidc1								cscidc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27]	RW	csc_en	CSC enable. 0: disabled 1: enabled
[26:18]	RW	cscidc2	DC parameter of input component 2. The MSB is the signed bit. The value is expressed as the complement.
[17:9]	RW	cscidc1	DC parameter of input component 1. The MSB is the signed bit. The value is expressed as the complement.
[8:0]	RW	cscidc0	DC parameter of input component 0. The MSB is the signed bit. The value is expressed as the complement.

VHDCSCODC

VHDCSCODC is a VHD output DC component register for CSC (instant register).

Offset Address	Register Name	Total Reset Value
0x0084	VHDCSCODC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					cscodc2											cscodc1								cscodc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved.
[26:18]	RW	cscodc2	DC parameter of output component 2. The MSB is the signed bit. The value is expressed as the complement.
[17:9]	RW	cscodc1	DC parameter of output component 1. The MSB is the signed bit. The value is expressed as the complement.
[8:0]	RW	cscodc0	DC parameter of output component 0. The MSB is the signed bit. The value is expressed as the complement.

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VHDCSCP0

VHDCSCP0 is VHD CSC parameter 0 register (instant register).

Offset Address	Register Name	Total Reset Value
0x0088	VHDCSCP0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp01												reserved				cscp00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp01	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp00	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

VHDCSCP1

VHDCSCP1 is VHD CSC parameter 1 register (instant register).

Offset Address	Register Name	Total Reset Value
0x008C	VHDCSCP1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp10												reserved				cscp02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp10	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.

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[12:0]	RW	cscp02	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

VHDCSCP2

VHDCSCP2 is VHD CSC parameter 2 register (instant register).

Offset Address	Register Name	Total Reset Value
0x0090	VHDCSCP2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp12												reserved				cscp11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp12	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp11	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

VHDCSCP3

VHDCSCP3 is VHD CSC parameter 3 register (instant register).

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Offset Address	Register Name	Total Reset Value
0x0094	VHDCSCP3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp21												reserved				cscp20											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp21	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp20	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

VHDCSCP4

VHDCSCP4 is VHD CSC parameter 4 register (instant register).

Offset Address	Register Name	Total Reset Value
0x0098	VHDCSCP4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cscp22											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved.
[12:0]	RW	cscp22	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

VHDACM0

VHDACM0 is VHD ACM control register 0.

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Offset Address	Register Name	Total Reset Value
0x00A0	VHDACM0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	acm3_en		acm2_en		acm1_en		acm0_en		acm_sec_blk				acm_fir_blk				acm_d_u_off				acm_c_u_off				acm_b_u_off				acm_a_u_off			
Reset	0		0		0		0		0		0		0		0		0		0		0		0		0		0		0		0	

Bits	Access	Name	Description
[31]	RW	acm3_en	ACM 3 enable.
[30]	RW	acm2_en	ACM 2 enable.
[29]	RW	acm1_en	ACM 1 enable.
[28]	RW	acm0_en	ACM 0 enable.
[27:24]	RW	acm_sec_blk	Index value of the V component of ACM 0.
[23:20]	RW	acm_fir_blk	Index value of the U component of ACM 0.
[19:15]	RW	acm_d_u_off	Fourth offset value of the U component of ACM 0.
[14:10]	RW	acm_c_u_off	Third offset value of the U component of ACM 0.
[9:5]	RW	acm_b_u_off	Second offset value of the U component of ACM 0.
[4:0]	RW	acm_a_u_off	First offset value of the U component of ACM 0.

VHDACM1

VHDACM1 is VHD ACM control register 1.

Offset Address	Register Name	Total Reset Value
0x00A4	VHDACM1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												acm_test_en	acm_d_v_off							acm_c_v_off				acm_b_v_off				acm_a_v_off			
Reset	0		0		0		0		0		0		0		0		0		0		0		0		0		0		0		0	

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.

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[20]	RW	acm_test_en	ACM comparison test enable. 0: ACM is enabled for the entire screen. 1: ACM is disabled for the left screen, and ACM is enabled for the right screen.
[19:15]	RW	acm_d_v_off	Fourth offset value of the V component of ACM 0.
[14:10]	RW	acm_c_v_off	Third offset value of the V component of ACM 0.
[9:5]	RW	acm_b_v_off	Second offset value of the V component of ACM 0.
[4:0]	RW	acm_a_v_off	First offset value of the V component of ACM 0.

VHDACM2

VHDACM2 is VHD ACM control register 2.

Offset Address	Register Name	Total Reset Value
0x00A8	VHDACM2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	acm_sec_blk	acm_fir_blk	acm_d_u_off	acm_c_u_off	acm_b_u_off	acm_a_u_off	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:24]	RW	acm_sec_blk	Index value of the V component of ACM 1.
[23:20]	RW	acm_fir_blk	Index value of the U component of ACM 1.
[19:15]	RW	acm_d_u_off	Fourth offset value of the U component of ACM 1.
[14:10]	RW	acm_c_u_off	Third offset value of the U component of ACM 1.
[9:5]	RW	acm_b_u_off	Second offset value of the U component of ACM 1.
[4:0]	RW	acm_a_u_off	First offset value of the U component of ACM 1.

VHDACM3

VHDACM3 is VHD ACM control register 3.

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Offset Address	Register Name	Total Reset Value
0x00AC	VHDACM3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			acm_d_v_off	acm_c_v_off	acm_b_v_off	acm_a_v_off	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:15]	RW	acm_d_v_off	Fourth offset value of the V component of ACM 1.
[14:10]	RW	acm_c_v_off	Third offset value of the V component of ACM 1.
[9:5]	RW	acm_b_v_off	Second offset value of the V component of ACM 1.
[4:0]	RW	acm_a_v_off	First offset value of the V component of ACM 1.

VHDACM4

VHDACM4 is VHD ACM control register 4.

Offset Address	Register Name	Total Reset Value
0x00B0	VHDACM4	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	acm_sec_blk	acm_fir_blk	acm_d_u_off	acm_c_u_off	acm_b_u_off	acm_a_u_off	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:24]	RW	acm_sec_blk	Index value of the V component of ACM 2.
[23:20]	RW	acm_fir_blk	Index value of the U component of ACM 2.
[19:15]	RW	acm_d_u_off	Fourth offset value of the U component of ACM 2.
[14:10]	RW	acm_c_u_off	Third offset value of the U component of ACM 2.
[9:5]	RW	acm_b_u_off	Second offset value of the U component of ACM 2.
[4:0]	RW	acm_a_u_off	First offset value of the U component of ACM 2.

VHDACM5

VHDACM5 is VHD ACM control register 5.

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Offset Address	Register Name	Total Reset Value
0x00B4	VHDACM5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												acm_d_v_off				acm_c_v_off				acm_b_v_off				acm_a_v_off							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:15]	RW	acm_d_v_off	Fourth offset value of the V component of ACM 2.
[14:10]	RW	acm_c_v_off	Third offset value of the V component of ACM 2.
[9:5]	RW	acm_b_v_off	Second offset value of the V component of ACM 2.
[4:0]	RW	acm_a_v_off	First offset value of the V component of ACM 2.

VHDACM6

VHDACM6 is VHD ACM control register 6.

Offset Address	Register Name	Total Reset Value
0x00B8	VHDACM6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				acm_sec_blk				acm_fir_blk				acm_d_u_off				acm_c_u_off				acm_b_u_off				acm_a_u_off							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:24]	RW	acm_sec_blk	Index value of the V component of ACM 3.
[23:20]	RW	acm_fir_blk	Index value of the U component of ACM 3.
[19:15]	RW	acm_d_u_off	Fourth offset value of the U component of ACM 3.
[14:10]	RW	acm_c_u_off	Third offset value of the U component of ACM 3.
[9:5]	RW	acm_b_u_off	Second offset value of the U component of ACM 3.
[4:0]	RW	acm_a_u_off	First offset value of the U component of ACM 3.

VHDACM7

VHDACM7 is VHD ACM control register 7.

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Offset Address	Register Name	Total Reset Value
0x00BC	VHDACM7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												acm_d_v_off				acm_c_v_off				acm_b_v_off				acm_a_v_off							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:15]	RW	acm_d_v_off	Fourth offset value of the V component of ACM 3.
[14:10]	RW	acm_c_v_off	Third offset value of the V component of ACM 3.
[9:5]	RW	acm_b_v_off	Second offset value of the V component of ACM 3.
[4:0]	RW	acm_a_v_off	First offset value of the V component of ACM 3.

VHDHSP

VHDHSP is a VHD horizontal scaling parameter register (non-instant register).

The scaling ratio is calculated as follows:

Scaling ratio = Input width/Output width

Offset Address	Register Name	Total Reset Value
0x00C0	VHDHSP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hlmsc_en	hchmsc_en	reserved					hlfir_en	hchfir_en	reserved			hfir_order	reserved			hratio															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hlmsc_en	Horizontal luminance scaling enable. 0: disabled 1: enabled
[30]	RW	hchmsc_en	Horizontal chrominance scaling enable. 0: disabled 1: enabled
[29:25]	-	reserved	Reserved.

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[24]	RW	hlfir_en	Horizontal luminance scaling mode. 0: replication mode (filtering disabled) 1: filtering mode (filtering enabled)
[23]	RW	hchfir_en	Horizontal chrominance scaling mode. 0: replication mode (filtering disabled) 1: filtering mode (filtering enabled)
[22:20]	-	reserved	Reserved.
[19]	RW	hfir_order	Horizontal scaling sequence. 0: Horizontal scaling is performed before vertical scaling. 1: Horizontal scaling is performed after vertical scaling.
[18:16]	-	reserved	Reserved.
[15:0]	RW	hratio	Horizontal scaling ratio, in (u, 4, 12) format.

VHDHLOFFSET

VHDHLOFFSET is a VHD horizontal luminance offset register (non-instant register). It is used for pan-scan.

Offset Address	Register Name	Total Reset Value
0x00C4	VHDHLOFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hor_loffset															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16:0]	RW	hor_loffset	Horizontal luminance offset, in (s, 5, 12) format. The value is expressed as the complement.

VHDHCOFFSET

VHDHCOFFSET is a VHD horizontal chrominance offset register (non-instant register). It is used for pan-scan.

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Offset Address	Register Name	Total Reset Value
0x00C8	VHDHCOFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hor_coffset															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16:0]	RW	hor_coffset	Horizontal chrominance offset, in (s, 5, 12) format. The value is expressed as the complement.

VHDVSP

VHDVSP is a VHD vertical scaling parameter register.

Offset Address	Register Name	Total Reset Value
0x00D8	VHDVSP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vlmsc_en	vchmsc_en	reserved		vsc_luma_tap	vsc_chroma_tap	chroma_type	vlfir_en	vchfir_en	reserved																						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	vlmsc_en	Vertical luminance scaling enable. 0: disabled 1: enabled
[30]	RW	vchmsc_en	Vertical chrominance scaling enable. 0: disabled 1: enabled
[29:28]	-	reserved	Reserved.
[27]	RW	vsc_luma_tap	Vertical luminance scaling tap. 0: 4-tap FIR 1: 2-tap FIR

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[26]	RW	vsc_chroma_tap	Vertical chrominance scaling tap. 0: 4-tap FIR 1: 2-tap FIR
[25]	RW	chroma_type	Vertical ratio of luminance and chrominance. 0: 422 1: 420
[24]	RW	vlfir_en	Vertical luminance scaling mode. 0: replication mode (filtering disabled) 1: filtering mode (filtering enabled)
[23]	RW	vchfir_en	Vertical chrominance scaling mode. 0: replication mode (filtering disabled) 1: filtering mode (filtering enabled)
[22:0]	-	reserved	Reserved.

VHDVSR

VHDVSR is VHD vertical scaling ratio register (non-instant register).

The scaling ratio is calculated as follows:

Scaling ratio = Input height/Output height

Offset Address	Register Name	Total Reset Value
0x00DC	VHDVSR	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vratio															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	vratio	Vertical scaling ratio, in (u, 4, 12) format.

VHDVOFFSET

VHDVOFFSET is a VHD vertical scaling offset register.

The vertical scaling offset is affected by field offset during pan-scanning and field offset when repeated frames occur. If no field offset occurs, vluma_offset is the lowest integral digit and the fractional part of offset_pan-scan. In YCbCr422 format, vchroma_offset is equal to vluma_offset; in YCbCr420 format, vchroma_offset is calculated as follows: vchroma_offset = scaling_chroma/2 – 0.25 If field offset is required (such as still frames or repeated frames) and the bottom field is repeated, the values of vluma_offset and vchroma_offset configured

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for the top field are the same as those in the case of no field offset. The field offset must be considered when scaling coefficients are configured for the bottom field.

Offset Address	Register Name	Total Reset Value
0x00E0	VHDVOFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vluma_offset																vchroma_offset															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	vluma_offset	Vertical luminance offset, in (s, 4, 12) format. The value is expressed as the complement.
[15:0]	RW	vchroma_offset	Vertical chrominance offset, in (s, 4, 12) format. The value is expressed as the complement.

VHDZMEORESO

VHDZMEORESO is a VHD zoom engine output resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x00E4	VHDZMEORESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								oh												ow											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	oh	Height (in line). The value is the actual height minus 1. In progressive mode, the frame height is referenced; in interlaced mode, the field height is referenced.
[11:0]	RW	ow	Width (in pixel). The value is the actual width minus 1. Note: The actual layer width must be an even number.

VHDZMEIRESO

VHDZMEIRESO is a VHD zoom engine input resolution register (non-instant register).

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Offset Address	Register Name	Total Reset Value
0x00E8	VHDZMEIRESO	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		ih			iw		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	ih	Height (in line). The value is the actual height minus 1. In progressive mode, the frame height is referenced; in interlaced mode, the field height is referenced.
[11:0]	RW	iw	Width (in pixel). The value is the actual width minus 1. Note: The actual layer width must be an even number.

VHDLTI_CTRL

VHDLTI_CTRL is an LTI control register.

Offset Address	Register Name	Total Reset Value
0x00F0	VHDLTI_CTRL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lti_en	reserved	lgain_ratio		reserved	lmixing_ratio	lhpass_coef4	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	**Access**	**Name**	**Description**
[31]	RW	lti_en	LTI enable. 0: disabled 1: enabled
[30:28]	RO	reserved	Reserved.
[27:16]	RW	lgain_ratio	Luminance gain coefficient.
[15]	RO	reserved	Reserved.
[14:8]	RW	lmixing_ratio	Weighted luminance mixing coefficient.
[7:0]	RW	lhpass_coef4	Luminance high-frequency component extraction coefficient 4.

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VHDLHPASS_COEF

VHDLHPASS_COEF is a luminance high-frequency component extraction coefficient register.

Offset Address	Register Name	Total Reset Value
0x00F4	VHDLHPASS_COEF	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lhpass_coef3		lhpass_coef2		lhpass_coef1		lhpass_coef0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	lhpass_coef3	Luminance high-frequency component extraction coefficient 3.
[23:16]	RW	lhpass_coef2	Luminance high-frequency component extraction coefficient 2.
[15:8]	RW	lhpass_coef1	Luminance high-frequency component extraction coefficient 1.
[7:0]	RW	lhpass_coef0	Luminance high-frequency component extraction coefficient 0.

VHDLTI_THRE

VHDLTI_THRE is an LTI processing threshold register.

Offset Address	Register Name	Total Reset Value
0x00F8	VHDLTI_THRE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lcoring_thre				lswing_thre			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lcoring_thre	Luminance coring threshold.
[15:0]	RW	lswing_thre	Luminance swing threshold.

VHDLHFREQ_THRE

VHDLHFREQ_THRE is a high-frequency component threshold register for the luminance high-frequency gain segmentation curve.

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Offset Address	Register Name	Total Reset Value
0x00FC	VHDLHFREQ_THRE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lhfreq_thre1																lhfreq_thre0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lhfreq_thre1	High-frequency component threshold 1 for the luminance high-frequency gain segmentation curve.
[15:0]	RW	lhfreq_thre0	High-frequency component threshold 0 for the luminance high-frequency gain segmentation curve.

VHDACCTHD1

VHDACCTHD1 is ACC operation threshold 1 register for the VHD channel.

Offset Address	Register Name	Total Reset Value
0x0100	VHDACCTHD1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	acc_en	acc_mode	thd_med_low										thd_high												thd_low							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	acc_en	ACC enable (non-instant field). 0: disabled 1: enabled
[30]	RW	acc_mode	Output ACC correction enable (instant field). 0: The ACC table is generated by the hardware. 1: The ACC table is configured by the software.
[29:20]	RW	thd_med_low	Threshold for medium- and low-luminance.
[19:10]	RW	thd_high	Threshold for high luminance.
[9:0]	RW	thd_low	Threshold for low luminance.

VHDACCTHD2

VHDACCTHD2 is ACC operation threshold 2 register for the VHD channel.

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Offset Address	Register Name	Total Reset Value
0x0104	VHDACCTHD2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												acc_reso_mode	acc_rst	acc_multiple						thd_med_high											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19]	RW	acc_reso_mode	ACC maximum resolution. When the width of an input picture is greater than 1920 pixels, this bit must be set to 1.
[18]	RW	acc_rst	ACC reset.
[17:10]	RW	acc_multiple	ACC operation multiplier.
[9:0]	RW	thd_med_high	Threshold for medium- and high-luminance.

VHDACCLOW1

VHDACCLOW1 is a VHD ACC lookup table register 1 for low luminance.

Offset Address	Register Name	Total Reset Value
0x0110	VHDACCLOW1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		table_data3n										table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for low luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for low luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for low luminance.

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VHDACCLOW2

VHDACCLOW2 is a VHD ACC lookup table register 2 for low luminance.

Offset Address	Register Name	Total Reset Value
0x0110	VHDACCLOW2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for low luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for low luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for low luminance.

VHDACCLOW3

VHDACCLOW3 is a VHD ACC lookup table register 3 for low luminance.

Offset Address	Register Name	Total Reset Value
0x0110	VHDACCLOW3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for low luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for low luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for low luminance.

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VHDACCMED1

VHDACCMED1 is a VHD ACC lookup table register 1 for medium luminance.

Offset Address	Register Name	Total Reset Value
0x0120	VHDACCMED1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n												table_data1n							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for medium luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium luminance.

VHDACCMED2

VHDACCMED2 is a VHD ACC lookup table register 2 for medium luminance.

Offset Address	Register Name	Total Reset Value
0x0124	VHDACCMED2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n												table_data1n							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for medium luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium luminance.

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VHDACCMED3

VHDACCMED3 is a VHD ACC lookup table register 3 for medium luminance.

Offset Address	Register Name	Total Reset Value
0x0128	VHDACCMED3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for medium luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium luminance.

VHDACCHIGH1

VHDACCHIGH1 is an ACC lookup table register 1 for high luminance.

Offset Address	Register Name	Total Reset Value
0x0130	VHDACCHIGH1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for high luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for high luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for high luminance.

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VHDACCHIGH2

VHDACCHIGH2 is an ACC lookup table register 2 for high luminance.

Offset Address	Register Name	Total Reset Value
0x0134	VHDACCHIGH2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for high luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for high luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for high luminance.

VHDACCHIGH3

VHDACCHIGH3 is an ACC lookup table register 3 for high luminance.

Offset Address	Register Name	Total Reset Value
0x0138	VHDACCHIGH3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for high luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for high luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for high luminance.

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VHDACCML1

VHDACCMED1 is an ACC lookup table register 1 for medium- and low-luminance.

Offset Address	Register Name	Total Reset Value
0x0140	VHDACCML1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for medium- and low-luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium- and low-luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium- and low-luminance.

VHDACCML2

VHDACCMED2 is an ACC lookup table register 2 for medium- and low-luminance.

Offset Address	Register Name	Total Reset Value
0x0144	VHDACCML2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for medium- and low-luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium- and low-luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium- and low-luminance.

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VHDACCML3

VHDACCMED3 is an ACC lookup table register 3 for medium- and low-luminance.

Offset Address	Register Name	Total Reset Value
0x0148	VHDACCML3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for medium- and low-luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium- and low-luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium- and low-luminance.

VHDACCMH1

VHDACCMH1 is an ACC lookup table register 1 for medium- and high-luminance.

Offset Address	Register Name	Total Reset Value
0x0150	VHDACCMH1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for medium- and high-luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium- and high-luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium- and high-luminance.

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VHDACCMH2

VHDACCMH2 is an ACC lookup table register 2 for medium- and high-luminance.

Offset Address	Register Name	Total Reset Value
0x0154	VHDACCMH2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for medium- and high-luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium- and high-luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium- and high-luminance.

VHDACCMH3

VHDACCMH3 is an ACC lookup table register 3 for medium- and high-luminance.

Offset Address	Register Name	Total Reset Value
0x0158	VHDACCMH3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for medium- and high-luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium- and high-luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium- and high-luminance.

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VHDACC3LOW

VHDACC3LOW is a low-threshold luminance statistical value register for three ACC regions. It is read-only.

Offset Address	Register Name	Total Reset Value
0x0160	VHDACC3LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cnt3_low																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:0]	RO	cnt3_low	Low-threshold luminance statistics on three regions.

VHDACC3MED

VHDACC3MED is a medium-threshold luminance statistical value register for three ACC regions. It is read-only.

Offset Address	Register Name	Total Reset Value
0x0164	VHDACC3MED	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cnt3_med																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:0]	RO	cnt3_med	Medium-threshold luminance statistics on three regions.

VHDACC3HIGH

VHDACC3HIGH is a high-threshold luminance statistical value register for three ACC regions. It is read-only.

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Offset Address	Register Name	Total Reset Value
0x0168	VHDACC3HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cnt3_high																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:0]	RO	cnt3_high	High-threshold luminance statistics on three regions.

VHDACC8MLOW

VHDACC8MLOW is a low-threshold luminance statistical value register after the ACC middle region is divided into eight segments. It is read-only.

Offset Address	Register Name	Total Reset Value
0x016C	VHDACC8MLOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cnt8_med_low																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:0]	RO	cnt8_med_low	Low-threshold luminance statistics on the middle region.

VHDACC8MHIGH

VHDACC8MHIGH is a high-threshold luminance statistical value register after the ACC middle region is divided into eight segments. It is read-only.

Offset Address	Register Name	Total Reset Value
0x0170	VHDACC8MHIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cnt8_med_high																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:0]	RO	cnt8_med_high	High-threshold luminance statistics on the middle region.

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VHDACCTOTAL

VHDACCTOTAL is an ACC pixel statistical value register. It is read-only.

Offset Address	Register Name	Total Reset Value
0x0174	VHDACCTOTAL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												acc_pix_total																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:0]	RO	acc_pix_total	Total ACC pixel.

VHDIFIRCOEF01

VHDIFIRCOEF01 is a VHD IFIR filtering coefficients 0–1 register.

Offset Address	Register Name	Total Reset Value
0x0180	VHDIFIRCOEF01	0x000D_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef1								reserved								coef0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	coef1	IFIR filtering coefficient 1.
[15:10]	-	reserved	Reserved.
[9:0]	RW	coef0	IFIR filtering coefficient 0.

VHDIFIRCOEF23

VHDIFIRCOEF23 is a VHD IFIR filtering coefficients 2–3 register.

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Offset Address	Register Name	Total Reset Value
0x0184	VHDIFIRCOEF23	0x0132_03C1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef3								reserved								coef2							
Reset	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	1

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	coef3	IFIR filtering coefficient 3.
[15:10]	-	reserved	Reserved.
[9:0]	RW	coef2	IFIR filtering coefficient 2.

VHDIFIRCOEF45

VHDIFIRCOEF45 is a VHD IFIR filtering coefficients 4–5 register.

Offset Address	Register Name	Total Reset Value
0x0188	VHDIFIRCOEF45	0x03C1_0132

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef5								reserved								coef4							
Reset	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	coef5	IFIR filtering coefficient 5.
[15:10]	-	reserved	Reserved.
[9:0]	RW	coef4	IFIR filtering coefficient 4.

VHDIFIRCOEF67

VHDIFIRCOEF67 is a VHD IFIR filtering coefficients 6–7 register.

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Offset Address	Register Name	Total Reset Value
0x018C	VHDIFIRCOEF67	0x0000_000D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef7								reserved				coef6											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	coef7	IFIR filtering coefficient 7.
[15:10]	-	reserved	Reserved.
[9:0]	RW	coef6	IFIR filtering coefficient 6.

VHDPmRESO

VHDPmRESO is a VHD region m resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x0400+m x 0x20 (m = 0–63)	VHDPmRESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				w											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	w	Width (in pixel). The value is the actual width minus 1. Note: The actual width must be an even number.

VHDPmLADDR

VHDPmLADDR is a VHD region m address register.

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Offset Address	Register Name	Total Reset Value
0x0404+m x 0x20 (m = 0–31)	VHDPmLADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Start address of VHD region m.

VHDPmCADDR

VHDPmCADDR is a VHD region m chrominance address register.

Offset Address	Register Name	Total Reset Value
0x0408+m x 0x20 (m = 0–31)	VHDPmCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Chrominance start address of VHD region m.

VHDPmSTRIDE

VHDPmSTRIDE is a VHD region m stride register.

Offset Address	Register Name	Total Reset Value
0x040C+m x 0x20 (m = 0–31)	VHDPmSTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_cstride																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	surface_cstride	Stride of the chrominance buffer of VHD region m (valid in semi-planar format), 128-bit alignment.

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[15:0]	RW	surface_stride	Stride of the buffer of VHD region m (valid in semi-planar format, luminance stride), 128-bit alignment.

VHDPmVFPOS

VHDPmVFPOS is a VHD region m video start position register (non-instant register). The start position is in the unit of pixel.

Offset Address	Register Name	Total Reset Value
0x0410 +m x 0x20 (m = 0–31)	VHDPmVFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								video_yfpos												video_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:12]	RW	video_yfpos	Start coordinates of the video column. The frame height is referenced and the unit is line.
[11:0]	RW	video_xfpos	Start coordinates of the video row.

VHDPmVLPOS

VHDPmVLPOS is the VHD region m video end position register (non-instant register). The end position is in the unit of pixel.

Offset Address	Register Name	Total Reset Value
0x0414+m x 0x20 (m = 0–31)	VHDPmVLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								video_ylpos												video_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:12]	RW	video_ylpos	Start coordinates of the video column. The frame height is referenced and the unit is line.
[11:0]	RW	video_xlpos	Start coordinates of the video row.

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VHD64REGIONENL

VHD64REGIONENL is the VHD regions 0–31 enable register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x0C04+n x 0x1000	VHD64REGIONENL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	p31_en	p30_en	p29_en	p28_en	p27_en	p26_en	p25_en	p24_en	p23_en	p22_en	p21_en	p20_en	p19_en	p18_en	p17_en	p16_en	p15_en	p14_en	p13_en	p12_en	p11_en	p10_en	p9_en	p8_en	p7_en	p6_en	p5_en	p4_en	p3_en	p2_en	p1_en	p0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	p31_en	VHD region 31 enable. 0: disabled 1: enabled
[30]	RW	p30_en	VHD region 30 enable. 0: disabled 1: enabled
[29]	RW	p29_en	VHD region 29 enable. 0: disabled 1: enabled
[28]	RW	p28_en	VHD region 28 enable. 0: disabled 1: enabled
[27]	RW	p27_en	VHD region 27 enable. 0: disabled 1: enabled
[26]	RW	p26_en	VHD region 26 enable. 0: disabled 1: enabled
[25]	RW	p25_en	VHD region 25 enable. 0: disabled 1: enabled
[24]	RW	p24_en	VHD region 24 enable. 0: disabled 1: enabled
[23]	RW	p23_en	VHD region 23 enable. 0: disabled 1: enabled

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[22]	RW	p22_en	VHD region 22 enable. 0: disabled 1: enabled
[21]	RW	p21_en	VHD region 21 enable. 0: disabled 1: enabled
[20]	RW	p20_en	VHD region 20 enable. 0: disabled 1: enabled
[19]	RW	p19_en	VHD region 19 enable. 0: disabled 1: enabled
[18]	RW	p18_en	VHD region 18 enable. 0: disabled 1: enabled
[17]	RW	p17_en	VHD region 17 enable. 0: disabled 1: enabled
[16]	RW	p16_en	VHD region 16 enable. 0: disabled 1: enabled
[15]	RW	p15_en	VHD region 15 enable. 0: disabled 1: enabled
[14]	RW	p14_en	VHD region 14 enable. 0: disabled 1: enabled
[13]	RW	p13_en	VHD region 13 enable. 0: disabled 1: enabled
[12]	RW	p12_en	VHD region 12 enable. 0: disabled 1: enabled
[11]	RW	p11_en	VHD region 11 enable. 0: disabled 1: enabled

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[10]	RW	p10_en	VHD region 10 enable. 0: disabled 1: enabled
[9]	RW	p9_en	VHD region 9 enable. 0: disabled 1: enabled
[8]	RW	p8_en	VHD region 8 enable. 0: disabled 1: enabled
[7]	RW	p7_en	VHD region 7 enable. 0: disabled 1: enabled
[6]	RW	p6_en	VHD region 6 enable. 0: disabled 1: enabled
[5]	RW	p5_en	VHD region 5 enable. 0: disabled 1: enabled
[4]	RW	p4_en	VHD region 4 enable. 0: disabled 1: enabled
[3]	RW	p3_en	VHD region 3 enable. 0: disabled 1: enabled
[2]	RW	p2_en	VHD region 2 enable. 0: disabled 1: enabled
[1]	RW	p1_en	VHD region 1 enable. 0: disabled 1: enabled
[0]	RW	p0_en	VHD region 0 enable. 0: disabled 1: enabled

VSDiCTRL

VSDiCTRL is a VSD control register (non-instant register). It is used to configure the layer information

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Offset Address	Register Name	Total Reset Value
0x3000+i x 0x1000 (i = 0–1)	VSDiCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_en	reserved											ifir_mode		vup_mode		reserved												ifmt			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	surface_en	Surface enable (non-instant register). 0: disabled 1: enabled
[30:20]	-	reserved	Reserved.
[19:18]	RW	ifir_mode	Horizontal chrominance IFIR mode. 00: reserved 01: chrominance IFIR copy mode 10: bilinear interpolation 11: 6-tap FIR
[17]	-	vup_mode	Register update mode. 0: update by field 1: update by frame
[16:4]	-	reserved	Reserved.
[3:0]	RW	ifmt	Input data format. 0x3: SPYCbCr420 0x4: SPYCbCr422 Other values: reserved

VSDiUPD

VSDiUPD is a VSD channel update enable register.

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Offset Address	Register Name	Total Reset Value
0x3004 + i x 0x1000 (i = 0–1)	VSDiUPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After updates, this bit is cleared automatically by the hardware.

VSDiCADDR

VSDiCADDR is a VSD current frame address register. In package pixel format, the address is the address of the frame buffer; in semi-planar pixel format, the address is the address of the luminance frame buffer.

Offset Address	Register Name	Total Reset Value
0x3010 + i x 0x1000 (i = 0–1)	VSDiCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_caddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_caddr	Address of the current frame.

VSDiCCADDR

VSDiCCADDR is a VSD current frame chrominance address register. In package pixel format, the address is invalid; in semi-planar pixel format, the address is the address of the luminance frame buffer.

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Offset Address	Register Name	Total Reset Value
0x3014 + i x 0x1000 (i = 0–1)	VSDiCCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_ccaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_ccaddr	Chrominance address of the current frame.

VSDiSTRIDE

VSDiSTRIDE is a VSD surface stride register.

Offset Address	Register Name	Total Reset Value
0x3024 + i x 0x1000 (i = 0–1)	VSDiSTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_cstride																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	surface_cstride	Stride of the chrominance frame buffer (valid in semi-planar format), 128-bit alignment.
[15:0]	RW	surface_stride	Stride of the frame buffer (valid in semi-planar format, luminance stride), 128-bit alignment.

VSDiIRESO

VSDiIRESO is a VSD input resolution register (non-instant register).

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Offset Address	Register Name	Total Reset Value
0x3028 + i x 0x1000 (i = 0–1)	VSDiIRESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ih												iw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	ih	Height (in line). The value is the actual height minus 1. The frame height is referenced.
[11:0]	RW	iw	Width (in pixel). The value is the actual width minus 1.

VSDiCBMPARA

VSDiCBMPARA is a VSD overlay parameter register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x3034 + i x 0x1000 (i = 0–1)	VSDiCBMPARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								galpha							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	galpha	Overlay global alpha value. The value ranges from 0 to 128. The value 128 indicates opaque, and the value 0 indicates full transparent.

VSDiDFPOS

VSDiDFPOS is a VSD surface start position (in the display window) register (non-instant register).

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Offset Address	Register Name	Total Reset Value
0x3060+i x 0x1000 (i = 0–1)	VSDiDFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_yfpos												disp_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	disp_yfpos	Start coordinates of the display column. The frame height is referenced and the unit is line.
[11:0]	RW	disp_xfpos	Start coordinates of the display row.

VSDiDLPOS

VSDiDLPOS is VSD surface end position (in the display window) register (non-instant register). The end position is in the unit of pixel.

Offset Address	Register Name	Total Reset Value
0x3064+i x 0x1000 (i = 0–1)	VSDiDLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_ylpos												disp_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	disp_ylpos	End coordinates of the display column. The frame height is referenced and the unit is line.
[11:0]	RW	disp_xlpos	End coordinates of the display row.

VSDIBK

VSDIBK is a video layer background color register.

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Offset Address	Register Name	Total Reset Value
0x3070 + i x 0x1000 (i = 0–1)	VSDIBK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vbk_alpha								vbk_y								vbk_cb								vbk_cr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	vbk_alpha	Levels 0–128 of the background filling color of the video layer.
[23:16]	RW	vbk_y	Y component.
[15:8]	RW	vbk_cb	Cb component.
[7:0]	RW	vbk_cr	Cr component.

VSDiCSCIDC

VSDiCSCIDC is a VSD input DC component register for CSC (instant register).

Offset Address	Register Name	Total Reset Value
0x3080 + i x 0x1000 (i = 0–1)	VSDiCSCIDC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				csc_en	cscidc2											cscidc1								cscidc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27]	RW	csc_en	CSC enable. 0: disabled 1: enabled
[26:18]	RW	cscidc2	DC parameter of input component 2. The MSB is the signed bit. The value is expressed as the complement.
[17:9]	RW	cscidc1	DC parameter of input component 1. The MSB is the signed bit. The value is expressed as the complement.
[8:0]	RW	cscidc0	DC parameter of input component 0. The MSB is the signed bit. The value is expressed as the complement.

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VSDiCSCODC

VSDiCSCODC is a VSD output DC component register for CSC (instant register).

Offset Address	Register Name	Total Reset Value
0x3084 + i x 0x1000 (i = 0–1)	VSDiCSCODC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	cscodc2		cscodc1		cscodc0		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved.
[26:18]	RW	cscodc2	DC parameter of output component 2. The MSB is the signed bit. The value is expressed as the complement.
[17:9]	RW	cscodc1	DC parameter of output component 1. The MSB is the signed bit. The value is expressed as the complement.
[8:0]	RW	cscodc0	DC parameter of output component 0. The MSB is the signed bit. The value is expressed as the complement.

VSDiCSCP0

VSDiCSCP0 is VSD CSC parameter 0 register (instant register).

Offset Address	Register Name	Total Reset Value
0x3088 + i x 0x1000 (i = 0–1)	VSDiCSCP0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	cscp01			reserved	cscp00		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp01	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.

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[12:0]	RW	cscp00	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

VSDiCSCP1

VSDiCSCP1 is VSD CSC parameter 1 register (instant register).

Offset Address	Register Name	Total Reset Value
0x308C + i x 0x1000 (i = 0–1)	VSDiCSCP1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp10												reserved				cscp02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp10	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp02	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

VSDiCSCP2

VSDiCSCP2 is VSD CSC parameter 2 register (instant register).

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Offset Address	Register Name	Total Reset Value
0x3090 + i x 0x1000 (i = 0–1)	VSDiCSCP2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp12												reserved				cscp11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp12	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp11	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

VSDiCSCP3

VSDiCSCP3 is VSD CSC parameter 3 register (instant register).

Offset Address	Register Name	Total Reset Value
0x3094+i x 0x1000 (i = 0–1)	VSDiCSCP3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp21												reserved				cscp20											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp21	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.

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[12:0]	RW	cscp20	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

VSDiCSCP4

VSDiCSCP4 is VSD CSC parameter 4 register (instant register).

Offset Address	Register Name	Total Reset Value
0x3098 + i x 0x1000 (i = 0–1)	VSDiCSCP4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cscp22											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved.
[12:0]	RW	cscp22	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

VSDIACM0

VSDIACM0 is VSD ACM control register 0.

Offset Address	Register Name	Total Reset Value
0x30A0 + i x 0x1000 (i = 0–1)	VSDIACM0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	acm3_en	acm2_en	acm1_en	acm0_en	acm_sec_blk				acm_fir_blk				acm_d_u_off				acm_c_u_off				acm_b_u_off				acm_a_u_off							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	**Access**	**Name**	**Description**
[31]	RW	acm3_en	ACM 3 enable.
[30]	RW	acm2_en	ACM 2 enable.
[29]	RW	acm1_en	ACM 1 enable.
[28]	RW	acm0_en	ACM 0 enable.

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[27:24]	RW	acm_sec_blk	Index value of the V component of ACM 0.
[23:20]	RW	acm_fir_blk	Index value of the U component of ACM 0.
[19:15]	RW	acm_d_u_off	Fourth offset value of the U component of ACM 0.
[14:10]	RW	acm_c_u_off	Third offset value of the U component of ACM 0.
[9:5]	RW	acm_b_u_off	Second offset value of the U component of ACM 0.
[4:0]	RW	acm_a_u_off	First offset value of the U component of ACM 0.

VSDIACM1

VSDIACM1 is VSD ACM control register 1.

Offset Address	Register Name	Total Reset Value
0x30A4 + i x 0x1000 (i = 0–1)	VSDIACM1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		acm_test_en	acm_d_v_off	acm_c_v_off	acm_b_v_off	acm_a_v_off	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20]	RW	acm_test_en	ACM comparison test enable. 0: ACM is enabled for the entire screen. 1: ACM is disabled for the left screen, and ACM is enabled for the right screen.
[19:15]	RW	acm_d_v_off	Fourth offset value of the V component of ACM 0.
[14:10]	RW	acm_c_v_off	Third offset value of the V component of ACM 0.
[9:5]	RW	acm_b_v_off	Second offset value of the V component of ACM 0.
[4:0]	RW	acm_a_v_off	First offset value of the V component of ACM 0.

VSDIACM2

VSDIACM2 is VSD ACM control register 2.

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Offset Address	Register Name	Total Reset Value
0x30A8 + i x 0x1000 (i = 0–1)	VSDIACM2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				acm_sec_blk				acm_fir_blk				acm_d_u_off				acm_c_u_off				acm_b_u_off				acm_a_u_off							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:24]	RW	acm_sec_blk	Index value of the V component of ACM 1.
[23:20]	RW	acm_fir_blk	Index value of the U component of ACM 1.
[19:15]	RW	acm_d_u_off	Fourth offset value of the U component of ACM 1.
[14:10]	RW	acm_c_u_off	Third offset value of the U component of ACM 1.
[9:5]	RW	acm_b_u_off	Second offset value of the U component of ACM 1.
[4:0]	RW	acm_a_u_off	First offset value of the U component of ACM 1.

VSDIACM3

VSDIACM3 is VSD ACM control register 3.

Offset Address	Register Name	Total Reset Value
0x30AC + i x 0x1000 (i = 0–1)	VSDIACM3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												acm_d_v_off				acm_c_v_off				acm_b_v_off				acm_a_v_off							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:15]	RW	acm_d_v_off	Fourth offset value of the V component of ACM 1.
[14:10]	RW	acm_c_v_off	Third offset value of the V component of ACM 1.
[9:5]	RW	acm_b_v_off	Second offset value of the V component of ACM 1.
[4:0]	RW	acm_a_v_off	First offset value of the V component of ACM 1.

VSDIACM4

VSDIACM4 is VSD ACM control register 4.

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Offset Address	Register Name	Total Reset Value
0x30B0 + i x 0x1000 (i = 0–1)	VSDIACM4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				acm_sec_blk				acm_fir_blk				acm_d_u_off				acm_c_u_off				acm_b_u_off				acm_a_u_off							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:24]	RW	acm_sec_blk	Index value of the V component of ACM 2.
[23:20]	RW	acm_fir_blk	Index value of the U component of ACM 2.
[19:15]	RW	acm_d_u_off	Fourth offset value of the U component of ACM 2.
[14:10]	RW	acm_c_u_off	Third offset value of the U component of ACM 2.
[9:5]	RW	acm_b_u_off	Second offset value of the U component of ACM 2.
[4:0]	RW	acm_a_u_off	First offset value of the U component of ACM 2.

VSDIACM5

VSDIACM5 is VSD ACM control register 5.

Offset Address	Register Name	Total Reset Value
0x30B4 + i x 0x1000 (i = 0–1)	VSDIACM5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												acm_d_v_off				acm_c_v_off				acm_b_v_off				acm_a_v_off							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:15]	RW	acm_d_v_off	Fourth offset value of the V component of ACM 2.
[14:10]	RW	acm_c_v_off	Third offset value of the V component of ACM 2.
[9:5]	RW	acm_b_v_off	Second offset value of the V component of ACM 2.
[4:0]	RW	acm_a_v_off	First offset value of the V component of ACM 2.

VSDIACM6

VSDIACM6 is VSD ACM control register 6.

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Offset Address	Register Name	Total Reset Value
0x30B8 + i x 0x1000 (i = 0–1)	VSDIACM6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				acm_sec_blk				acm_fir_blk				acm_d_u_off				acm_c_u_off				acm_b_u_off				acm_a_u_off							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:24]	RW	acm_sec_blk	Index value of the V component of ACM 3.
[23:20]	RW	acm_fir_blk	Index value of the U component of ACM 3.
[19:15]	RW	acm_d_u_off	Fourth offset value of the U component of ACM 3.
[14:10]	RW	acm_c_u_off	Third offset value of the U component of ACM 3.
[9:5]	RW	acm_b_u_off	Second offset value of the U component of ACM 3.
[4:0]	RW	acm_a_u_off	First offset value of the U component of ACM 3.

VSDIACM7

VSDIACM7 is VSD ACM control register 7.

Offset Address	Register Name	Total Reset Value
0x30BC + i x 0x1000 (i = 0–1)	VSDIACM7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												acm_d_v_off				acm_c_v_off				acm_b_v_off				acm_a_v_off							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:15]	RW	acm_d_v_off	Fourth offset value of the V component of ACM 3.
[14:10]	RW	acm_c_v_off	Third offset value of the V component of ACM 3.
[9:5]	RW	acm_b_v_off	Second offset value of the V component of ACM 3.
[4:0]	RW	acm_a_v_off	First offset value of the V component of ACM 3.

VSDIACCTHD1

VSDIACCTHD1 is ACC operation threshold 1 register for the VSD channel.

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Offset Address	Register Name	Total Reset Value
0x3100 + i x 0x1000 (i = 0–1)	VSDIACCTHD1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	acc_en	acc_mode	thd_med_low										thd_high												thd_low							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	acc_en	ACC enable (non-instant field). 0: disabled 1: enabled
[30]	RW	acc_mode	Output ACC correction enable (instant field). 0: The ACC table is generated by the hardware. 1: The ACC table is configured by the software.
[29:20]	RW	thd_med_low	Threshold for medium- and low-luminance.
[19:10]	RW	thd_high	Threshold for high luminance.
[9:0]	RW	thd_low	Threshold for low luminance.

VSDIACCTHD2

VSDIACCTHD2 is ACC operation threshold 2 register for the VSD channel.

Offset Address	Register Name	Total Reset Value
0x3104 + i x 0x1000 (i = 0–1)	VSDIACCTHD2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													acc_rst	acc_multiple										thd_med_high							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved.
[18]	RW	acc_rst	ACC reset.
[17:10]	RW	acc_multiple	ACC operation multiplier.

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[9:0]	RW	thd_med_high	Threshold for medium- and high-luminance.

VSDIACCLOW1

VSDIACCLOW1 is an ACC lookup table register 1 for low luminance.

Offset Address	Register Name	Total Reset Value
0x3110 + i x 0x1000 (i = 0–1)	VSDIACCLOWN	0x0000_0000

Bit	31 30	29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9 8	7 6 5 4	3 2 1 0
Name	reserved		table_data3n		table_data2n		table_data1n			
Reset	0 0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for low luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for low luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for low luminance.

VSDIACCLOW2

VSDIACCLOW2 is an ACC lookup table register 2 for low luminance.

Offset Address	Register Name	Total Reset Value
0x3114 + i x 0x1000 (i = 0–1)	VSDIACCLOW2	0x0000_0000

Bit	31 30	29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9 8	7 6 5 4	3 2 1 0
Name	reserved		table_data3n		table_data2n		table_data1n			
Reset	0 0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for low luminance.

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[19:10]	RW	table_data2n	Lookup table data 2 for low luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for low luminance.

VSDIACCLOW3

VSDIACCLOW3 is an ACC lookup table register 3 for low luminance.

Offset Address	Register Name	Total Reset Value
0x3110 + i x 0x1000 (i = 0–1)	VSDIACCLOW3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	table_data3n		table_data2n		table_data1n		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for low luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for low luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for low luminance.

VSDIACCMED1

VSDIACCMED1 is an ACC lookup table register 1 for medium luminance.

Offset Address	Register Name	Total Reset Value
0x3120 + i x 0x1000 (i = 0–1)	VSDIACCMED1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	table_data3n		table_data2n		table_data1n		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.

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[29:20]	RW	table_data3n	Lookup table data 3 for medium luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium luminance.

VSDIACCMED2

VSDIACCMED2 is an ACC lookup table register 2 for medium luminance.

Offset Address	Register Name	Total Reset Value
0x3124 + i x 0x1000 (i = 0–1)	VSDIACCMED2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for medium luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium luminance.

VSDIACCMED3

VSDIACCMED3 is an ACC lookup table register 3 for medium luminance.

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Offset Address	Register Name	Total Reset Value
0x3128 + i x 0x1000 (i = 0–1)	VSDIACCMED3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for medium luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium luminance.

VSDIACCHIGH1

VSDIACCHIGH1 is an ACC lookup table register 1 for high luminance.

Offset Address	Register Name	Total Reset Value
0x3130 + i x 0x1000 (i = 0–1)	VSDIACCHIGH1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for high luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for high luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for high luminance.

VSDIACCHIGH2

VSDIACCHIGH2 is an ACC lookup table register 2 for high luminance.

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Offset Address	Register Name	Total Reset Value
0x3134 + i x 0x1000 (i = 0–1)	VSDIACCHIGH2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for high luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for high luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for high luminance.

VSDIACCHIGH3

VSDIACCHIGH3 is an ACC lookup table register 3 for high luminance.

Offset Address	Register Name	Total Reset Value
0x3138 + i x 0x1000 (i = 0–1)	VSDIACCHIGH3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for high luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for high luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for high luminance.

VSDIACCML1

VSDIACCML1 is an ACC lookup table register 1 for medium- and low-luminance.

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Offset Address	Register Name	Total Reset Value
0x3140 + i x 0x1000 (i = 0–1)	VSDIACCML1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for medium- and low-luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium- and low-luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium- and low-luminance.

VSDIACCML2

VSDIACCML2 is an ACC lookup table register 2 for medium- and low-luminance.

Offset Address	Register Name	Total Reset Value
0x3144 + i x 0x1000 (i = 0–1)	VSDIACCML2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for medium- and low-luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium- and low-luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium- and low-luminance.

VSDIACCML3

VSDIACCML3 is an ACC lookup table register 3 for medium- and low-luminance.

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Offset Address	Register Name	Total Reset Value
0x3148 + i x 0x1000 (i = 0–1)	VSDIACCML3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for medium- and low-luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium- and low-luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium- and low-luminance.

VSDIACCMH1

VSDIACCMH1 is an ACC lookup table register 1 for medium- and high-luminance.

Offset Address	Register Name	Total Reset Value
0x3150 + i x 0x1000 (i = 0–1)	VSDIACCMH1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for medium- and high-luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium- and high-luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium- and high-luminance.

VSDIACCMH2

VSDIACCMH2 is an ACC lookup table register 2 for medium- and high-luminance.

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Offset Address	Register Name	Total Reset Value
0x3154 + i x 0x1000 (i = 0–1)	VSDIACCMH2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for medium- and high-luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium- and high-luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium- and high-luminance.

VSDIACCMH3

VSDIACCMH3 is an ACC lookup table register 3 for medium- and high-luminance.

Offset Address	Register Name	Total Reset Value
0x3158 + i x 0x1000 (i = 0–1)	VSDIACCMH3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				table_data3n								table_data2n								table_data1n											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	table_data3n	Lookup table data 3 for medium- and high-luminance.
[19:10]	RW	table_data2n	Lookup table data 2 for medium- and high-luminance.
[9:0]	RW	table_data1n	Lookup table data 1 for medium- and high-luminance.

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VSDIACC3LOW

VSDIACC3LOW is a low-threshold luminance statistical value register for three ACC regions. It is read-only.

Offset Address	Register Name	Total Reset Value
0x3160 + i x 0x1000 (i = 0–1)	VSDIACC3LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cnt3_low																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:0]	RO	cnt3_low	Low-threshold luminance statistics on three regions.

VSDIACC3MED

VSDIACC3MED is a medium-threshold luminance statistical value register for three ACC regions. It is read-only.

Offset Address	Register Name	Total Reset Value
0x3164 + i x 0x1000 (i = 0–1)	VSDIACC3MED	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cnt3_med																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:0]	RO	cnt3_med	Medium-threshold luminance statistics on three regions.

VSDIACC3HIGH

VSDIACC3HIGH is a high-threshold luminance statistical value register for three ACC regions. It is read-only.

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Offset Address	Register Name	Total Reset Value
0x3168 + i x 0x1000 (i = 0–1)	VSDIACC3HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cnt3_high																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:0]	RO	cnt3_high	High-threshold luminance statistics on three regions.

VSDIACC8MLOW

VSDIACC8MLOW is a low-threshold luminance statistical value register after the ACC middle region is divided into eight segments. It is read-only.

Offset Address	Register Name	Total Reset Value
0x316C + i x 0x1000 (i = 0–1)	VSDIACC8MLOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cnt8_med_low																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:0]	RO	cnt8_med_low	Low-threshold luminance statistics on the middle region.

VSDIACC8MHIGH

VSDIACC8MHIGH is a high-threshold luminance statistical value register after the ACC middle region is divided into eight segments. It is read-only.

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Offset Address	Register Name	Total Reset Value
0x3170 + i x 0x1000 (i = 0–1)	VSDIACC8MHIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cnt8_med_high																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:0]	RO	cnt8_med_high	High-threshold luminance statistics on the middle region.

VSDIACCTOTAL

VSDIACCTOTAL is an ACC pixel statistical value register. It is read-only.

Offset Address	Register Name	Total Reset Value
0x3174 + i x 0x1000 (i = 0–1)	VSDIACCTOTAL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												acc_pix_total																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:0]	RO	acc_pix_total	Total ACC pixel.

VSDiIFIRCOEF01

VSDiIFIRCOEF01 is a VSD IFIR filtering coefficients 0–1 register.

Offset Address	Register Name	Total Reset Value
0x3180+i x 0x1000 (i = 0–1)	VSDiIFIRCOEF01	0x000D_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef1								reserved				coef0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.

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[25:16]	RW	coef1	IFIR filtering coefficient 1.
[15:10]	-	reserved	Reserved.
[9:0]	RW	coef0	IFIR filtering coefficient 0.

VSDiIFIRCOEF23

VSDiIFIRCOEF23 is a VSD IFIR filtering coefficients 2–3 register.

Offset Address	Register Name	Total Reset Value
0x3184 + i x 0x1000 (i = 0–1)	VSDiIFIRCOEF23	0x0132_03C1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef3								reserved								coef2							
Reset	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	1

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	coef3	IFIR filtering coefficient 3.
[15:10]	-	reserved	Reserved.
[9:0]	RW	coef2	IFIR filtering coefficients 21.

VSDiIFIRCOEF45

VSDiIFIRCOEF45 is a VSD IFIR filtering coefficients 4–5 register.

Offset Address	Register Name	Total Reset Value
0x3188 + i x 0x1000 (i = 0–1)	VSDiIFIRCOEF45	0x003C_0132

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef5								reserved								coef4							
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	coef5	IFIR filtering coefficient 5.
[15:10]	-	reserved	Reserved.
[9:0]	RW	coef4	IFIR filtering coefficient 4.

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VSDiIFIRCOEF67

VSDiIFIRCOEF67 is a VSD IFIR filtering coefficients 6–7 register.

Offset Address	Register Name	Total Reset Value
0x318C + i x 0x1000 (i = 0–1)	VSDiIFIRCOEF67	0x0000_000D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef7								reserved								coef6							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	coef7	IFIR filtering coefficient 7.
[15:10]	-	reserved	Reserved.
[9:0]	RW	coef6	IFIR filtering coefficient 6.

VSDiPMRESO

VSDiPMRESO is a VSD region 0 resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x3400 + i x 0x1000 + m x 0x20 (i = 0–1) (m = 0 or m = 0–7)	VSDiPMRESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								h												w											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:12]	RW	h	Height (in line). The frame height is referenced. The value is the actual height minus 1. Note: The actual height must be an even number.
[11:0]	RW	w	Width (in pixel). The value is the actual width minus 1. Note: The actual width must be an even number.

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VSDiPMLADDR

VSDiPMLADDR is a VSD region 0 address register.

Offset Address	Register Name	Total Reset Value
0x3404 + i x 0x1000 + m x 0x20 (i = 0–1) (m = 0 or m = 0–7)	VSDiPMLADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Start address of VSD region m.

VSDiPMCADDR

VSDiPMCADDR is a VSD region 0 chrominance address register.

Offset Address	Register Name	Total Reset Value
0x3408 + i x 0x1000 + m x 0x20 (i = 0–1) (m = 0 or m = 0–7)	VSDiPMCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Chrominance start address of VSD region 0.

VSDiPMSTRIDE

VSDiPMSTRIDE is a VSD region 0 stride register.

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Offset Address	Register Name	Total Reset Value
0x340C + i x 0x1000 + m x 0x20 (i = 0–1) (m = 0 or m = 0–7)	VSDiPMSTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_cstride																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	surface_cstride	Stride of the chrominance buffer of VSD region 0 (valid in semi-planar format), 128-bit alignment.
[15:0]	RW	surface_stride	Stride of the buffer of VSD region 0 (valid in semi-planar format, luminance stride), 128-bit alignment.

VSDiPMVFPOS

VSDiPMVFPOS is a VSD region 0 video start position register. The start position is in the unit of pixel.

Offset Address	Register Name	Total Reset Value
0x3410 + i x 0x1000 + m x 0x20 (i = 0–1) (m = 0 or m = 0–7)	VSDiPMVFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								video_yfpos												video_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:12]	RW	video_yfpos	Start coordinates of the video column. The frame height is referenced and the unit is line.
[11:0]	RW	video_xfpos	Start coordinates of the video row.

VSDiPMVLPOS

VSDiPMVLPOS is a VSD region 0 video end position register (non-instant register). The end position is in the unit of pixel.

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Offset Address	Register Name	Total Reset Value
0x3414 + i x 0x1000 + m x 0x20 (i = 0–1) (m = 0 or m = 0–7)	VSDiPMVLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								video_ylpos												video_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:12]	RW	video_ylpos	Start coordinates of the video column. The frame height is referenced and the unit is line.
[11:0]	RW	video_xlpos	Start coordinates of the video row.

VSDi16REGIONEN

VSDi16REGIONEN is a VSD 16 region enable register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x3C04 + i x 0x1000 + m x 0x20 (i = 0–1) (m = 0 or m = 0–7)	VSDi16REGIONEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								p7_en	p6_en	p5_en	p4_en	p3_en	p2_en	p1_en	p0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7]	RW	p7_en	VSD0 region m enable. 0: disabled 1: enabled
[6]	RW	p6_en	VSD0 region m enable. 0: disabled 1: enabled

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[5]	RW	p5_en	VSD0 region m enable. 0: disabled 1: enabled
[4]	RW	p4_en	VSD0 region m enable. 0: disabled 1: enabled
[3]	RW	p3_en	VSD0 region m enable. 0: disabled 1: enabled
[2]	RW	p2_en	VSD0 region m enable. 0: disabled 1: enabled
[1]	RW	p1_en	VSD0 region m enable. 0: disabled 1: enabled
[0]	RW	p0_en	VSD0 or VSD1 region m enable. 0: disabled 1: enabled

WBC2CTRL

WBC2CTRL is a WBC2 control register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x8200	WBC2CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wbc2_en	reserved																	wbc2_dft	reserved				req_interval								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	wbc2_en	WBC2 enable. 0: disabled 1: enabled
[30:14]	-	reserved	Reserved.

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[13:12]	RW	wbc2_dft	Output data format of WBC2. 00: SPYCbCr422 01: SPYCbCr420 Other values: invalid
[11:10]	-	reserved	Reserved.
[9:0]	RW	req_interval	Minimum request interval of the WBC0 bus. It indicates req_interval clock cycles from the end of request n to the start of request n + 1.

WBC2UPD

WBC2UPD is a WBC2 channel update enable register.

Offset Address	Register Name	Total Reset Value
0x8204	WBC2UPD	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								regup
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	regup	Capture register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After updates, this bit is cleared automatically by the hardware.

WBC2ADDR

WBC2ADDR is a WBC2 capture address register.

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Offset Address	Register Name	Total Reset Value
0x8208	WBC2ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wbcaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wbcaddr	Frame buffer address. It is 4-byte-aligned and the lower two bits are invalid (seamless combination is supported).

WBC2STRIDE

WBC2STRIDE is a WBC2 capture stride register.

Offset Address	Register Name	Total Reset Value
0x820C	WBC2STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																wbc2stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	–	reserved	Reserved.
[15:0]	RW	wbc2stride	Frame buffer stride, 128-bit alignment.

WBC2ORESO

WBC2ORESO is a WBC2 output resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x8210	WBC2ORESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								oh												ow											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.

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[23:12]	RW	oh	Height (in line). The value is the actual height minus 1. Note: In interlaced output mode, the actual layer height must be an even number. There is no such limitation in progressive output mode.
[11:0]	RW	ow	Width (in pixel). The value is the actual width minus 1. Note: The actual layer width must be an even number.

WBC2CADDR

WBC2CADDR is a WBC2 write chrominance address register.

Offset Address	Register Name	Total Reset Value
0x8220	WBC2CADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wbccaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wbccaddr	Address of the frame chrominance buffer. It is 4-byte-aligned and the lower two bits are invalid (seamless combination is supported).

WBC2CSTRIDE

WBC2CSTRIDE is a WBC2 capture chrominance stride register.

Offset Address	Register Name	Total Reset Value
0x8224	WBC2CSTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																wbc2cstride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	–	reserved	Reserved.
[15:0]	RW	wbc2cstride	Stride of the frame chrominance buffer, 16-byte alignment.

WBC2HSP

WBC2HSP is a WBC2 horizontal scaling parameter register (non-instant register).

The scaling ratio is calculated as follows:

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Scaling ratio = Input width/Output width

Offset Address	Register Name	Total Reset Value
0x82C0	WBC2HSP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hlmsc_en	hchmsc_en	reserved					hlfir_en	hchfir_en	reserved			hfir_order	reserved			hratio															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hlmsc_en	Horizontal luminance scaling enable. 0: disabled 1: enabled
[30]	RW	hchmsc_en	Horizontal chrominance scaling enable. 0: disabled 1: enabled
[29:25]	-	reserved	Reserved.
[24]	RW	hlfir_en	Horizontal luminance scaling mode. 0: replication mode (filtering disabled) 1: filtering mode (filtering enabled)
[23]	RW	hchfir_en	Horizontal chrominance scaling mode. 0: replication mode (filtering disabled) 1: filtering mode (filtering enabled)
[22:20]	-	reserved	Reserved.
[19]	RW	hfir_order	Horizontal scaling sequence. 0: Horizontal scaling is performed before vertical scaling. 1: Horizontal scaling is performed after vertical scaling.
[18:16]	-	reserved	Reserved.
[15:0]	RW	hratio	Horizontal scaling ratio, in (u, 4, 12) format.

WBC2HLOFFSET

WBC2HLOFFSET is a WBC2 horizontal luminance offset register (non-instant register). It is used for pan-scan.

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Offset Address	Register Name	Total Reset Value
0x82C4	WBC2HLOFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hor_loffset															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16:0]	RW	hor_loffset	Horizontal luminance offset, in (s, 5, 12) format. The value is expressed as the complement.

WBC2HCOFFSET

WBC2HCOFFSET is a WBC2 horizontal chrominance offset register (non-instant register). It is used for pan-scan.

Offset Address	Register Name	Total Reset Value
0x82C8	WBC2HCOFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hor_coffset															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16:0]	RW	hor_coffset	Horizontal chrominance offset, in (s, 5, 12) format. The value is expressed as the complement.

WBC2VSP

WBC2VSP is a WBC2 vertical scaling parameter register.

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Offset Address	Register Name	Total Reset Value
0x82D8	WBC2VSP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vlmsc_en	vchmsc_en	reserved		vsc_luma_tap	vsc_chroma_tap	chroma_type	vlfir_en	vchfir_en	vsc_out_420	reserved																					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	vlmsc_en	Vertical luminance scaling enable. 0: disabled 1: enabled
[30]	RW	vchmsc_en	Vertical chrominance scaling enable. 0: disabled 1: enabled
[29:28]	RW	reserved	Reserved.
[27]	RW	vsc_luma_tap	Vertical luminance scaling tap. 0: 4-tap FIR 1: 2-tap FIR
[26]	RW	vsc_chroma_tap	Vertical chrominance scaling tap. 0: 4-tap FIR 1: 2-tap FIR
[25]	RW	chroma_type	Vertical ratio of luminance and chrominance. This field must be set to 0. 0: 422 1: reserved
[24]	RW	vlfir_en	Vertical luminance scaling mode. 0: replication mode (filtering disabled) 1: filtering mode (filtering enabled)
[23]	RW	vchfir_en	Vertical chrominance scaling mode. 0: replication mode (filtering disabled) 1: filtering mode (filtering enabled)
[22]	RW	vsc_out_420	Output format. 0: 422 1: 420

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[21:0]	-	reserved	Reserved.

WBC2VSR

WBC2VSR is a WBC2 vertical scaling ratio register (non-instant register).

The scaling ratio is calculated as follows:

Scaling ratio = Input height/Output height

Offset Address	Register Name	Total Reset Value
0x82DC	WBC2VSR	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vratio															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	vratio	Vertical scaling ratio, in (u, 4, 12) format.

WBC2VOFFSET

WBC2VOFFSET is a WBC2 vertical scaling offset register.

The vertical scaling offset is affected by field offset during pan-scanning and field offset when repeated frames occur. If no field offset occurs, vluma_offset is the lowest integral digit and the fractional part of offset_pan-scan. In YCbCr422 format, vchroma_offset is equal to vluma_offset; in YCbCr420 format, vchroma_offset is calculated as follows: vchroma_offset = scaling_chroma/2 – 0.25 If field offset is required (such as still frames or repeated frames) and the bottom field is repeated, the values of vluma_offset and vchroma_offset configured for the top field are the same as those in the case of no field offset. The field offset must be considered when scaling coefficients are configured for the bottom field.

Offset Address	Register Name	Total Reset Value
0x82E0	WBC2VOFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vluma_offset																vchroma_offset															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	vluma_offset	Vertical luminance offset, in (s, 4, 12) format. The value is expressed as the complement.

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[15:0]	RW	vchroma_offset	Vertical chrominance offset, in (s, 4, 12) format. The value is expressed as the complement.

WBC2ZMEORESO

WBC2ZMEORESO is a WBC2 zoom engine output resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x82E4	WBC2ZMEORESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								oh												ow											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	oh	Height (in line). The value is the actual height minus 1. In progressive mode, the frame height is referenced; in interlaced mode, the field height is referenced.
[11:0]	RW	ow	Width (in pixel). The value is the actual width minus 1. Note: The actual layer width must be an even number.

WBC2ZMEIRESO

WBC2ZMEIRESO is a WBC2 zoom engine input resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x82E8	WBC2ZMEIRESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ih												iw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	ih	Height (in line). The value is the actual height minus 1. In progressive mode, the frame height is referenced; in interlaced mode, the field height is referenced.
[11:0]	RW	iw	Width (in pixel). The value is the actual width minus 1. Note: The actual layer width must be an even number.

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G0CTRL

G0CTRL is a G0 control register (non-instant register). It is used to configure the layer information

Offset Address	Register Name	Total Reset Value
0x9000	G0CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_en	reserved			upd_mode	read_mode	dcmp_mode	dcmp_inter	reserved														bitext		ifmt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	surface_en	Surface enable (non-instant register). 0: disabled 1: enabled
[30:28]	-	reserved	Reserved.
[27]	RW	upd_mode	Update mode. 0: update by frame 1: update by field
[26]	RW	read_mode	Data read mode. 0: The read mode is automatically selected based on the interface read mode. That is, the progressive read mode is selected in progressive display mode, and the interlaced read mode is selected in interlaced display mode. 1: The progressive read mode is selected forcibly.
[25]	RW	dcmp_mode	Decompression mode (non-instant register). 0: non-decompression mode 1: decompression mode
[24]	RW	dcmp_inter	Interlaced decompression control (non-instant register). 0: progressive decompression 1: interlaced decompression
[23:10]	RW	reserved	Reserved.
[9:8]	RW	bitext	Bit extend mode of the input bitmap. 0X: lower bits stuffed with 0s 10: lower bits stuffed with the MSB 11: lower bits stuffed with upper bits

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[7:0]	RW	ifmt	Input data format. 0x49: ARGB1555 0x68: ARGB8888 Other values: reserved

G0UPD

G0UPD is the G0 channel update enable register.

Offset Address	Register Name	Total Reset Value
0x9004	G0UPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After updates, this bit is cleared automatically by the hardware.

G0ADDR

G0ADDR is the G0 address register. When the horizontal pixel offsets, the address is calculated according to the description of G0SFPOS.

Offset Address	Register Name	Total Reset Value
0x9008	G0ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Address of the surface frame buffer.

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G0STRIDE

G0STRIDE is the G0 stride register.

Offset Address	Register Name	Total Reset Value
0x900C	G0STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	–	reserved	Reserved.
[15:0]	RW	surface_stride	Stride of the frame buffer.

G0CBMPARA

G0CBMPARA is the G0 overlay parameter register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9010	G0CBMPARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		premult_en	palpha_en	reserved				galpha							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	-	reserved	Reserved.
[13]	RW	premult_en	Whether the input bitmap is a premultiply bitmap. 0: non-premultiply bitmap 1: premultiply bitmap
[12]	RW	palpha_en	Pixel alpha enable. 0: disabled 1: enabled
[11:8]	RW	reserved	Reserved.
[7:0]	RW	galpha	Overlay global alpha value. This value ranges from 0 to 255. The value 255 indicates opaque, and the value 0 indicates full transparent.

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G0CKEYMAX

G0CKEYMAX is the G0 maximum colorkey register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9014	G0CKEYMAX	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	va0		keyr_max		keyg_max		keyb_max	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	va0	Alpha0 value. When the data format is alphaRGB1555 and the alpha value is 0, the alpha0 value is used.
[23:16]	RW	keyr_max	Maximum value of colorkey R component.
[15:8]	RW	keyg_max	Maximum value of colorkey G component.
[7:0]	RW	keyb_max	Maximum value of colorkey B component.

G0CKEYMIN

G0CKEYMIN is the G0 minimum colorkey register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9018	G0CKEYMIN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	va1		keyr_min		keyg_min		keyb_min	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	va1	Alpha1 value. When the data format is alphaRGB1555 and the alpha value is 1, the alpha1 value is used.
[23:16]	RW	keyr_min	Minimum value of colorkey R component.
[15:8]	RW	keyg_min	Minimum value of colorkey G component.
[7:0]	RW	keyb_min	Minimum value of colorkey B component.

G0CMASK

G0CMASK is the G0 colorkey mask register (non-instant register). When the corresponding bit is 0, the colorkey is compared. In this case, this bit can be ignored.

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Offset Address	Register Name	Total Reset Value
0x901C	G0CMASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								kmsk_r								kmsk_g								kmsk_b							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RW	kmsk_r	R component of colorkey mask.
[15:8]	RW	kmsk_g	G component of colorkey mask.
[7:0]	RW	kmsk_b	B component of colorkey mask.

G0IRESO

G0IRESO is the G0 input resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9020	G0IRESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ih												iw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	ih	Height (in line). The value is the actual height minus 1. Note: In interlaced output mode, the actual layer height must be an even number. There is no such limitation in progressive output mode.
[11:0]	RW	iw	Width (in pixel). The value is the actual width minus 1. Note: The actual layer width must be an even number.

G0ORESO

G0ORESO is the G0 output resolution register (non-instant register).

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Offset Address	Register Name	Total Reset Value
0x9024	G0ORESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								oh												ow											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	oh	Height (in line). The value is the actual height minus 1. Note: In interlaced output mode, the actual layer height must be an even number. There is no such limitation in progressive output mode.
[11:0]	RW	ow	Width (in pixel). The value is the actual width minus 1. Note: The actual layer width must be an even number.

G0DFPOS

G0DFPOS is the G0 surface start position (in the display window) register (non-instant register). The start position is in the unit of pixel.

Offset Address	Register Name	Total Reset Value
0x902C	G0DFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_yfpos												disp_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	disp_yfpos	Column start coordinates.
[11:0]	RW	disp_xfpos	Row start coordinates.

G0DLPOS

G0DLPOS is the G0 surface end position (in the display window) register (non-instant register). The end position is in the unit of pixel.

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Offset Address	Register Name	Total Reset Value
0x9030	G0DLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_ylpos												disp_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	disp_ylpos	Column end coordinates.
[11:0]	RW	disp_xlpos	Row end coordinates.

G0CSCIDC

G0CSCIDC is the G0 input DC component register for CSC (instant register).

Offset Address	Register Name	Total Reset Value
0x90A0	G0CSCIDC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				csc_en	cscidc2											cscidc1								cscidc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27]	RW	csc_en	CSC enable. 0: disabled 1: enabled
[26:18]	RW	cscidc2	DC parameter of input component 2. The MSB is the signed bit. The value is expressed as the complement.
[17:9]	RW	cscidc1	DC parameter of input component 1. The MSB is the signed bit. The value is expressed as the complement.
[8:0]	RW	cscidc0	DC parameter of input component 0. The MSB is the signed bit. The value is expressed as the complement.

G0CSCODC

G0CSCODC is the G0 output DC component register for CSC (instant register).

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Offset Address	Register Name	Total Reset Value
0x90A4	G0CSCODC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscodc2												cscodc1								cscodc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved.
[26:18]	RW	cscodc2	DC parameter of output component 2. The MSB is the signed bit. The value is expressed as the complement.
[17:9]	RW	cscodc1	DC parameter of output component 1. The MSB is the signed bit. The value is expressed as the complement.
[8:0]	RW	cscodc0	DC parameter of output component 0. The MSB is the signed bit. The value is expressed as the complement.

G0CSCP0

G0CSCP0 is the G0 CSC parameter 0 register (instant register).

Offset Address	Register Name	Total Reset Value
0x90A8	G0CSCP0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp01												reserved				cscp00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp01	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp00	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

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G0CSCP1

G0CSCP1 is the G0 CSC parameter 1 register (instant register).

Offset Address	Register Name	Total Reset Value
0x90AC	G0CSCP1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp10												reserved				cscp02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp10	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp02	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

G0CSCP2

G0CSCP2 is the G0 CSC parameter 2 register (instant register).

Offset Address	Register Name	Total Reset Value
0x90B0	G0CSCP2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp12												reserved				cscp11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp12	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.

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[12:0]	RW	cscp11	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

G0CSCP3

G0CSCP3 is the G0 CSC parameter 3 register (instant register).

Offset Address	Register Name	Total Reset Value
0x90B4	G0CSCP3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp21												reserved				cscp20											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp21	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp20	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

G0CSCP4

G0CSCP4 is the G0 CSC parameter 4 register (instant register).

Offset Address	Register Name	Total Reset Value
0x90B8	G0CSCP4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cscp22											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved.

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[12:0]	RW	cscp22	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

G0DCMPBANKWIDTH

G0DCMPBANKWIDTH is the G0 compressed data bank width register.

Offset Address	Register Name	Total Reset Value
0x91B4	G0DCMPBANKWIDTH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				dcmp_bankwidth											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved.
[11:0]	RW	dcmp_bankwidth	Bank width of the compressed data, 128-bit alignment.

G0DCMPSTRIDE

G0DCMPSTRIDE is the G0 compressed data stride register.

Offset Address	Register Name	Total Reset Value
0x91B8	G0DCMPSTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dcmp_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	dcmp_stride	Stride of the compressed data, 128-bit alignment.

G0DCMPAADDR

G0DCMPAADDR is the G0 compressed data start address register of A component.

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Offset Address	Register Name	Total Reset Value
0x91BC	G0DCMPAADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcmp_addr_a																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dcmp_addr_a	Start address of the compressed data.

G0DCMPRADDR

G0DCMPRADDR is the G0 compressed data start address register of R component.

Offset Address	Register Name	Total Reset Value
0x91C0	G0DCMPRADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcmp_addr_r																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dcmp_addr_r	Start address of the compressed data.

G0DCMPGADDR

G0DCMPGADDR is the G0 compressed data start address register of G component.

Offset Address	Register Name	Total Reset Value
0x91C4	G0DCMPGADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcmp_addr_g																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dcmp_addr_g	Start address of the compressed data.

G0DCMPBADDR

G0DCMPBADDR is the G0 compressed data start address register of B component.

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Offset Address	Register Name	Total Reset Value
0x91C8	G0DCMPBADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcmp_addr_b																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dcmp_addr_b	Start address of the compressed data.

G2CTRL

G2CTRL is the G2 control register (non-instant register). It is used to configure the layer information

Offset Address	Register Name	Total Reset Value
0x9400	G2CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_en	reserved			upd_mode	read_mode	dcmp_mode	dcmp_inter	reserved														bitext		ifmt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	surface_en	Surface enable (non-instant register). 0: disabled 1: enabled
[30:28]	-	reserved	Reserved.
[27]	RW	upd_mode	Update mode. 0: update by frame 1: update by field
[26]	RW	read_mode	Data read mode. 0: The read mode is automatically selected based on the interface read mode. That is, the progressive read mode is selected in progressive display mode, and the interlaced read mode is selected in interlaced display mode. 1: The progressive read mode is selected forcibly.

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[25]	RW	dcmp_mode	Decompression mode (non-instant register). 0: non-decompression mode 1: decompression mode
[24]	RW	dcmp_inter	Interlaced decompression control (non-instant register). 0: progressive decompression 1: interlaced decompression
[23:10]	RW	reserved	Reserved.
[9:8]	RW	bitext	Bit extend mode of the input bitmap. 0X: lower bits stuffed with 0s 10: lower bits stuffed with the MSB 11: lower bits stuffed with upper bits
[7:0]	RW	ifmt	Input data format. 0x49: ARGB1555 0x68: ARGB8888 Other values: reserved

G2UPD

G2UPD is the G2 channel update enable register.

Offset Address	Register Name	Total Reset Value
0x9404	G2UPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After updates, this bit is cleared automatically by the hardware

G2ADDR

G2ADDR is the G2 address register. When the horizontal pixel offsets, the address is calculated according to the description of G2SFPOS.

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Offset Address	Register Name	Total Reset Value
0x9408	G2ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Address of the surface frame buffer.

G2STRIDE

G2STRIDE is the G2 stride register.

Offset Address	Register Name	Total Reset Value
0x940C	G2STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	–	reserved	Reserved.
[15:0]	RW	surface_stride	Stride of the frame buffer.

G2CBMPARA

G2CBMPARA is the G2 overlay parameter register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9410	G2CBMPARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		premult_en	palpha_en	reserved				galpha							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	-	reserved	Reserved.

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[13]	RW	premult_en	Whether the input bitmap is a premultiply bitmap. 0: non-premultiply bitmap 1: premultiply bitmap
[12]	RW	palpha_en	Pixel alpha enable. 0: disabled 1: enabled
[11:8]	RW	reserved	Reserved.
[7:0]	RW	galpha	Overlay global alpha value. This value ranges from 0 to 255. The value 255 indicates opaque, and the value 0 indicates full transparent.

G2CKEYMAX

G2CKEYMAX is the G2 maximum colorkey register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9414	G2CKEYMAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	va0								keyr_max								keyg_max								keyb_max							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	va0	Alpha0 value. When the data format is alphaRGB1555 and the alpha value is 0, the alpha0 value is used.
[23:16]	RW	keyr_max	Maximum value of colorkey R component.
[15:8]	RW	keyg_max	Maximum value of colorkey G component.
[7:0]	RW	keyb_max	Maximum value of colorkey B component.

G2CKEYMIN

G2CKEYMIN is the G2 minimum colorkey register (non-instant register).

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Offset Address	Register Name	Total Reset Value
0x9418	G2CKEYMIN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	va1		keyr_min		keyg_min		keyb_min	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	va1	Alpha1 value. When the data format is alphaRGB1555 and the alpha value is 1, the alpha1 value is used.
[23:16]	RW	keyr_min	Minimum value of colorkey R component.
[15:8]	RW	keyg_min	Minimum value of colorkey G component.
[7:0]	RW	keyb_min	Minimum value of colorkey B component.

G2CMASK

G2CMASK is the G2 colorkey mask register (non-instant register). When the corresponding bit is 0, the colorkey is compared. In this case, this bit can be ignored.

Offset Address	Register Name	Total Reset Value
0x941C	G2CMASK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		kmsk_r		kmsk_g		kmsk_b	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RW	kmsk_r	R component of colorkey mask.
[15:8]	RW	kmsk_g	G component of colorkey mask.
[7:0]	RW	kmsk_b	B component of colorkey mask.

G2IRESO

G2IRESO is the G2 input resolution register (non-instant register).

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Offset Address	Register Name	Total Reset Value
0x9420	G2IRESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ih												iw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	ih	Height (in line). The value is the actual height minus 1. Note: In interlaced output mode, the actual layer height must be an even number. There is no such limitation in progressive output mode.
[11:0]	RW	iw	Width (in pixel). The value is the actual width minus 1. Note: The actual layer width must be an even number.

G2ORESO

G2ORESO is the G2 output resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9424	G2ORESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								oh												ow											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	oh	Height (in line). The value is the actual height minus 1. Note: In interlaced output mode, the actual layer height must be an even number. There is no such limitation in progressive output mode.
[11:0]	RW	ow	Width (in pixel). The value is the actual width minus 1. Note: The actual layer width must be an even number.

G2DFPOS

G2DFPOS is the G2 surface start position (in the display window) register (non-instant register). The start position is in the unit of pixel.

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Offset Address	Register Name	Total Reset Value
0x942C	G2DFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_yfpos												disp_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	disp_yfpos	Column start coordinates.
[11:0]	RW	disp_xfpos	Row start coordinates.

G2DLPOS

G2DLPOS is the G2 surface end position (in the display window) register (non-instant register). The end position is in the unit of pixel.

Offset Address	Register Name	Total Reset Value
0x9430	G2DLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_ylpos												disp_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	disp_ylpos	Column end coordinates.
[11:0]	RW	disp_xlpos	Row end coordinates.

G2CSCIDC

G2CSCIDC is the G2 input DC component register for CSC (instant register).

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Offset Address	Register Name	Total Reset Value
0x94A0	G2CSCIDC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				csc_en	cscidc2											cscidc1								cscidc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27]	RW	csc_en	CSC enable. 0: disabled 1: enabled
[26:18]	RW	cscidc2	DC parameter of input component 2. The MSB is the signed bit. The value is expressed as the complement.
[17:9]	RW	cscidc1	DC parameter of input component 1. The MSB is the signed bit. The value is expressed as the complement.
[8:0]	RW	cscidc0	DC parameter of input component 0. The MSB is the signed bit. The value is expressed as the complement.

G2CSCODC

G2CSCODC is the G2 output DC component register for CSC (instant register).

Offset Address	Register Name	Total Reset Value
0x94A4	G2CSCODC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					cscodc2											cscodc1								cscodc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved.
[26:18]	RW	cscodc2	DC parameter of output component 2. The MSB is the signed bit. The value is expressed as the complement.
[17:9]	RW	cscodc1	DC parameter of output component 1. The MSB is the signed bit. The value is expressed as the complement.
[8:0]	RW	cscodc0	DC parameter of output component 0. The MSB is the signed bit. The value is expressed as the complement.

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G2CSCP0

G2CSCP0 is the G2 CSC parameter 0 register (instant register).

Offset Address	Register Name	Total Reset Value
0x94A8	G2CSCP0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp01												reserved				cscp00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp01	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp00	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

G2CSCP1

G2CSCP1 is the G2 CSC parameter 1 register (instant register).

Offset Address	Register Name	Total Reset Value
0x94AC	G2CSCP1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp10												reserved				cscp02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp10	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.

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[12:0]	RW	cscp02	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

G2CSCP2

G2CSCP2 is the G2 CSC parameter 2 register (instant register).

Offset Address	Register Name	Total Reset Value
0x94B0	G2CSCP2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp12												reserved				cscp11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp12	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp11	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

G2CSCP3

G2CSCP3 is the G2 CSC parameter 3 register (instant register).

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Offset Address	Register Name	Total Reset Value
0x94B4	G2CSCP3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp21												reserved				cscp20											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp21	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp20	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

G2CSCP4

G2CSCP4 is the G2 CSC parameter 4 register (instant register).

Offset Address	Register Name	Total Reset Value
0x94B8	G2CSCP4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cscp22											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved.
[12:0]	RW	cscp22	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

G3CTRL

G3CTRL is the G3 control register (non-instant register). It is used to configure the layer information

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Offset Address	Register Name	Total Reset Value
0x9600	G3CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_en	reserved			upd_mode	read_mode	dcmp_mode	dcmp_inter	reserved														bitext		ifmt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	surface_en	Surface enable (non-instant register). 0: disabled 1: enabled
[30:28]	-	reserved	Reserved.
[27]	RW	upd_mode	Update mode. 0: update by frame 1: update by field
[26]	RW	read_mode	Data read mode. 0: The read mode is automatically selected based on the interface read mode. That is, the progressive read mode is selected in progressive display mode, and the interlaced read mode is selected in interlaced display mode. 1: The progressive read mode is selected forcibly.
[25]	RW	dcmp_mode	Decompression mode (non-instant register). 0: non-decompression mode 1: decompression mode
[24]	RW	dcmp_inter	Interlaced decompression control (non-instant register). 0: progressive decompression 1: interlaced decompression
[23:10]	RW	reserved	Reserved.
[9:8]	RW	bitext	Bit extend mode of the input bitmap. 0X: lower bits stuffed with 0s 10: lower bits stuffed with the MSB 11: lower bits stuffed with upper bits
[7:0]	RW	ifmt	Input data format. 0x49: ARGB1555 0x68: ARGB8888 Other values: reserved

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G3UPD

G3UPD is the G3 channel update enable register.

Offset Address	Register Name	Total Reset Value
0x9604	G3UPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After updates, this bit is cleared automatically by the hardware

G3ADDR

G3ADDR is the G3 address register. When the horizontal pixel offsets, the address is calculated according to the description of G3SFPOS.

Offset Address	Register Name	Total Reset Value
0x9608	G3ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Address of the surface frame buffer.

G3STRIDE

G3STRIDE is the G3 stride register.

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Offset Address	Register Name	Total Reset Value
0x960C	G3STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	–	reserved	Reserved.
[15:0]	RW	surface_stride	Stride of the frame buffer.

G3CBMPARA

G3CBMPARA is the G3 overlay parameter register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9610	G3CBMPARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		premult_en	palpha_en	reserved				galpha							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	-	reserved	Reserved.
[13]	RW	premult_en	Whether the input bitmap is a premultiply bitmap. 0: non-premultiply bitmap 1: premultiply bitmap
[12]	RW	palpha_en	Pixel alpha enable. 0: disabled 1: enabled
[11:8]	RW	reserved	Reserved.
[7:0]	RW	galpha	Overlay global alpha value. This value ranges from 0 to 255. The value 255 indicates opaque, and the value 0 indicates full transparent.

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G3CKEYMAX

G3CKEYMAX is the G3 maximum colorkey register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9614	G3CKEYMAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	va0								keyr_max								keyg_max								keyb_max							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	va0	Alpha0 value. When the data format is alphaRGB1555 and the alpha value is 0, the alpha0 value is used.
[23:16]	RW	keyr_max	Maximum value of colorkey R component.
[15:8]	RW	keyg_max	Maximum value of colorkey G component.
[7:0]	RW	keyb_max	Maximum value of colorkey B component.

G3CKEYMIN

G3CKEYMIN is the G3 minimum colorkey register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9618	G3CKEYMIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	va1								keyr_min								keyg_min								keyb_min							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	va1	Alpha1 value. When the data format is alphaRGB1555 and the alpha value is 1, the alpha1 value is used.
[23:16]	RW	keyr_min	Minimum value of colorkey R component.
[15:8]	RW	keyg_min	Minimum value of colorkey G component.
[7:0]	RW	keyb_min	Minimum value of colorkey B component.

G3CMASK

G3CMASK is the G3 colorkey mask register (non-instant register). When the corresponding bit is 0, the colorkey is compared. In this case, this bit can be ignored.

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Offset Address	Register Name	Total Reset Value
0x961C	G3CMASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								kmsk_r								kmsk_g								kmsk_b							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RW	kmsk_r	R component of colorkey mask.
[15:8]	RW	kmsk_g	G component of colorkey mask.
[7:0]	RW	kmsk_b	B component of colorkey mask.

G3IRESO

G3IRESO is the G3 input resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9620	G3IRESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ih												iw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	ih	Height (in line). The value is the actual height minus 1. Note: In interlaced output mode, the actual layer height must be an even number. There is no such limitation in progressive output mode.
[11:0]	RW	iw	Width (in pixel). The value is the actual width minus 1. Note: The actual layer width must be an even number.

G3ORESO

G3ORESO is the G3 output resolution register (non-instant register).

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Offset Address	Register Name	Total Reset Value
0x9624	G3ORESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								oh												ow											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	oh	Height (in line). The value is the actual height minus 1. Note: In interlaced output mode, the actual layer height must be an even number. There is no such limitation in progressive output mode.
[11:0]	RW	ow	Width (in pixel). The value is the actual width minus 1. Note: The actual layer width must be an even number.

G3DFPOS

G3DFPOS is the G3 surface start position (in the display window) register (non-instant register). The start position is in the unit of pixel.

Offset Address	Register Name	Total Reset Value
0x962C	G3DFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_yfpos												disp_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	disp_yfpos	Column start coordinates.
[11:0]	RW	disp_xfpos	Row start coordinates.

G3DLPOS

G3DLPOS is the G3 surface end position (in the display window) register (non-instant register). The end position is in the unit of pixel.

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Offset Address	Register Name	Total Reset Value
0x9630	G3DLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_ylpos												disp_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	disp_ylpos	Column end coordinates.
[11:0]	RW	disp_xlpos	Row end coordinates.

G3CSCIDC

G3CSCIDC is the G3 input DC component register for CSC (instant register).

Offset Address	Register Name	Total Reset Value
0x96A0	G3CSCIDC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				csc_en	cscidc2											cscidc1								cscidc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27]	RW	csc_en	CSC enable. 0: disabled 1: enabled
[26:18]	RW	cscidc2	DC parameter of input component 2. The MSB is the signed bit. The value is expressed as the complement.
[17:9]	RW	cscidc1	DC parameter of input component 1. The MSB is the signed bit. The value is expressed as the complement.
[8:0]	RW	cscidc0	DC parameter of input component 0. The MSB is the signed bit. The value is expressed as the complement.

G3CSCODC

G3CSCODC is the G3 output DC component register for CSC (instant register).

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Offset Address	Register Name	Total Reset Value
0x96A4	G3CSCODC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscodc2												cscodc1								cscodc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved.
[26:18]	RW	cscodc2	DC parameter of output component 2. The MSB is the signed bit. The value is expressed as the complement.
[17:9]	RW	cscodc1	DC parameter of output component 1. The MSB is the signed bit. The value is expressed as the complement.
[8:0]	RW	cscodc0	DC parameter of output component 0. The MSB is the signed bit. The value is expressed as the complement.

G3CSCP0

G3CSCP0 is the G3 CSC parameter 0 register (instant register).

Offset Address	Register Name	Total Reset Value
0x96A8	G3CSCP0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp01												reserved				cscp00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp01	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp00	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

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G3CSCP1

G3CSCP1 is the G3 CSC parameter 1 register (instant register).

Offset Address	Register Name	Total Reset Value
0x96AC	G3CSCP1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp10												reserved				cscp02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp10	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp02	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

G3CSCP2

G3CSCP2 is the G3 CSC parameter 2 register (instant register).

Offset Address	Register Name	Total Reset Value
0x96B0	G3CSCP2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp12												reserved				cscp11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp12	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.

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[12:0]	RW	cscp11	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

G3CSCP3

G3CSCP3 is the G3 CSC parameter 3 register (instant register).

Offset Address	Register Name	Total Reset Value
0x96B4	G3CSCP3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp21												reserved				cscp20											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp21	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp20	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

G3CSCP4

G3CSCP4 is the G3 CSC parameter 4 register (instant register).

Offset Address	Register Name	Total Reset Value
0x96B8	G3CSCP4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cscp22											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved.

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[12:0]	RW	cscp22	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

HCCTRL

HCCTRL is the HC control register (non-instant register). It is used to configure the layer information

Offset Address	Register Name	Total Reset Value
0x9A00	HCCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_en	reserved			upd_mode	read_mode	reserved																bitext		ifmt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	surface_en	Surface enable (non-instant register). 0: disabled 1: enabled
[30:28]	-	reserved	Reserved.
[27]	RW	upd_mode	Update mode. 0: update by frame 1: update by field
[26]	RW	read_mode	Data read mode. 0: The read mode is automatically selected based on the interface read mode. That is, the progressive read mode is selected in progressive display mode, and the interlaced read mode is selected in interlaced display mode. 1: The progressive read mode is selected forcibly.
[25:10]	-	reserved	Reserved.
[9:8]	RW	bitext	Bit extend mode of the input bitmap. 0X: lower bits stuffed with 0s 10: lower bits stuffed with the MSB 11: lower bits stuffed with upper bits

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[7:0]	RW	ifmt	Input data format. 0x49: ARGB1555 0x68: ARGB8888 Other values: reserved

HCUPD

HCUPD is the HC channel update enable register.

Offset Address	Register Name	Total Reset Value
0x9A04	HCUPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After updates, this bit is cleared automatically by the hardware

HCADDR

HCADDR is the HC address register. When the horizontal pixel offsets, the address is calculated according to the description of HCSFPOS.

Offset Address	Register Name	Total Reset Value
0x9A08	HCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Address of the surface frame buffer.

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HCSTRIDE

HCSTRIDE is the HC stride register.

Offset Address	Register Name	Total Reset Value
0x9A0C	HCSTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	–	reserved	Reserved.
[15:0]	RW	surface_stride	Stride of the frame buffer.

HCCBMPARA

HCCBMPARA is the HC overlay parameter register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9A10	HCCBMPARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																key_mode	key_en	reserved	palpha_en	reserved				galpha							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15]	RW	key_mode	Color key mode. 0: The color is regarded as the colorkey when the following condition is met: Keymin ≤ Pixel ≤ Keymax 1: The color is regarded as the colorkey when either of the following conditions is met: Pixel ≤ Keymin or Pixel ≥ Keymax
[14]	RW	key_en	Colorkey enable. 0: disabled 1: enabled
[13]	–	reserved	Whether the input bitmap is a premultiply bitmap. 0: non-premultiply bitmap 1: premultiply bitmap

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[12]	RW	palpha_en	Pixel alpha enable. 0: disabled 1: enabled
[11:8]	–	reserved	Reserved.
[7:0]	RW	galpha	Overlay global alpha value. This value ranges from 0 to 255. The value 255 indicates opaque, and the value 0 indicates full transparent.

HCCKEYMAX

HCCKEYMAX is the HC maximum colorkey register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9A14	HCCKEYMAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	va0								keyr_max								keyg_max								keyb_max							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	va0	Alpha0 value. When the data format is alphaRGB1555 and the alpha value is 0, the alpha0 value is used.
[23:16]	RW	keyr_max	Maximum value of colorkey R component.
[15:8]	RW	keyg_max	Maximum value of colorkey G component.
[7:0]	RW	keyb_max	Maximum value of colorkey B component.

HCCKEYMIN

HCCKEYMIN is the HC minimum colorkey register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9A18	HCCKEYMIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	va1								keyr_min								keyg_min								keyb_min							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	va1	Alpha1 value. When the data format is alphaRGB1555 and the alpha value is 1, the alpha1 value is used.
[23:16]	RW	keyr_min	Minimum value of colorkey R component.

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[15:8]	RW	keyg_min	Minimum value of colorkey G component.
[7:0]	RW	keyb_min	Minimum value of colorkey B component.

HCCMASK

HCCMASK is the HC colorkey mask register (non-instant register). When the corresponding bit is 1, the colorkey is compared. In this case, this bit can be ignored.

Offset Address	Register Name	Total Reset Value
0x9A1C	HCCMASK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		kmsk_r		kmsk_g		kmsk_b	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	kmsk_r	R component of colorkey mask.
[15:8]	RW	kmsk_g	G component of colorkey mask.
[7:0]	RW	kmsk_b	B component of colorkey mask.

HCIRESO

HCIRESO is the HC input resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9A20	HCIRESO	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		ih			iw		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	ih	Height (in line). The value is the actual height minus 1. Note: In interlaced output mode, the actual layer height must be an even number. There is no such limitation in progressive output mode.
[11:0]	RW	iw	Width (in pixel). The value is the actual width minus 1. Note: The actual layer width must be an even number.

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HCDFPOS

HCDFPOS is the HC surface start position (in the display window) register (non-instant register). The start position is in the unit of pixel.

Offset Address	Register Name	Total Reset Value
0x9A2C	HCDFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_yfpos												disp_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	disp_yfpos	Column start coordinates.
[11:0]	RW	disp_xfpos	Row start coordinates.

HCDLPOS

HCDLPOS is the HC surface end position (in the display window) register (non-instant register). The end position is in the unit of pixel.

Offset Address	Register Name	Total Reset Value
0x9A30	HCDLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_ylpos												disp_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	disp_ylpos	Column end coordinates.
[11:0]	RW	disp_xlpos	Row end coordinates.

HCCSCIDC

HCCSCIDC is the HC input DC component register for CSC (instant register).

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Offset Address	Register Name	Total Reset Value
0x9AA0	HCCSCIDC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				csc_en	cscidc2											cscidc1								cscidc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27]	RW	csc_en	CSC enable. 0: disabled 1: enabled
[26:18]	RW	cscidc2	DC parameter of input component 2. The MSB is the signed bit. The value is expressed as the complement.
[17:9]	RW	cscidc1	DC parameter of input component 1. The MSB is the signed bit. The value is expressed as the complement.
[8:0]	RW	cscidc0	DC parameter of input component 0. The MSB is the signed bit. The value is expressed as the complement.

HCCSCODC

HCCSCODC is the HC output DC component register for CSC (instant register).

Offset Address	Register Name	Total Reset Value
0x9AA4	HCCSCODC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					cscodc2											cscodc1								cscodc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved.
[26:18]	RW	cscodc2	DC parameter of output component 2. The MSB is the signed bit. The value is expressed as the complement.
[17:9]	RW	cscodc1	DC parameter of output component 1. The MSB is the signed bit. The value is expressed as the complement.
[8:0]	RW	cscodc0	DC parameter of output component 0. The MSB is the signed bit. The value is expressed as the complement.

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HCCSCP0

HCCSCP0 is the HC CSC parameter 0 register (instant register).

Offset Address	Register Name	Total Reset Value
0x9AA8	HCCSCP0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp01												reserved				cscp00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp01	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp00	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

HCCSCP1

HCCSCP1 is the HC CSC parameter 1 register (instant register).

Offset Address	Register Name	Total Reset Value
0x9AAC	HCCSCP1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp10												reserved				cscp02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp10	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.

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[12:0]	RW	cscp02	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

HCCSCP2

HCCSCP2 is the HC CSC parameter 2 register (instant register).

Offset Address	Register Name	Total Reset Value
0x9AB0	HCCSCP2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp12												reserved				cscp11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp12	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp11	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

HCCSCP3

HCCSCP3 is the HC CSC parameter 3 register (instant register).

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Offset Address	Register Name	Total Reset Value
0x9AB4	HCCSCP3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp21												reserved				cscp20											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp21	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp20	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

HCCSCP4

HCCSCP4 is the HC CSC parameter 4 register (instant register).

Offset Address	Register Name	Total Reset Value
0x9AB8	HCCSCP4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cscp22											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved.
[12:0]	RW	cscp22	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

CBMBKG1

CBMBKG1 is the HD0 overlay background color register.

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Offset Address	Register Name	Total Reset Value
0x9E00	CBMBKG1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		cbm_bkgy		cbm_bkgcb		cbm_bkgcr	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	cbm_bkgy	Overlay background color of mixer 1, Y component.
[15:8]	RW	cbm_bkgcb	Overlay background color of mixer 1, Cb component.
[7:0]	RW	cbm_bkgcr	Overlay background color of mixer 1, Cr component.

CBMBKG2

CBMBKG2 is the HD1 overlay background color register.

Offset Address	Register Name	Total Reset Value
0x9E04	CBMBKG2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		cbm_bkgy		cbm_bkgcb		cbm_bkgcr	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	cbm_bkgy	Overlay background color of mixer 2, Y component.
[15:8]	RW	cbm_bkgcb	Overlay background color of mixer 2, Cb component.
[7:0]	RW	cbm_bkgcr	Overlay background color of mixer 2, Cr component.

CBMBKG3

CBMBKG3 is the SD0 overlay background color register.

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Offset Address	Register Name	Total Reset Value
0x9E08	CBMBKG3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cbm_bkgy								cbm_bkgcb								cbm_bkgcr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	cbm_bkgy	Overlay background color of mixer 3, Y component.
[15:8]	RW	cbm_bkgcb	Overlay background color of mixer 3, Cb component.
[7:0]	RW	cbm_bkgcr	Overlay background color of mixer 3, Cr component.

CBMBKG4

CBMBKG4 is the SD1 overlay background color register.

Offset Address	Register Name	Total Reset Value
0x9E0C	CBMBKG4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cbm_bkgy								cbm_bkgcb								cbm_bkgcr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	cbm_bkgy	Overlay background color of mixer 4, Y component.
[15:8]	RW	cbm_bkgcb	Overlay background color of mixer 4, Cb component.
[7:0]	RW	cbm_bkgcr	Overlay background color of mixer 4, Cr component.

CBMATTR

CBMATTR is a crossbar configuration register.

sur_attr_x indicates that layer X is bound to mixer 1 or mixer 2.

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Offset Address	Register Name	Total Reset Value
0x9E10	CBMATTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sur_attr3				sur_attr2				sur_attr1				sur_attr0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:12]	RW	sur_attr3	G4 link. 0x0: mixer 1 for DHD0 0x1: mixer 2 for DHD1 0x2: mixer 3 for DSD0 0x3: mixer 4 for DSD1 Other values: invalid
[11:8]	RW	sur_attr2	HC1 link. 0x0: mixer 1 for DHD0 0x1: mixer 2 for DHD1 0x2: mixer 3 for DSD0 0x3: mixer 4 for DSD1 Other values: invalid
[7:4]	RW	sur_attr1	HC0 link. 0x0: mixer 1 for DHD0 0x1: mixer 2 for DHD1 0x2: mixer 3 for DSD0 0x3: mixer 4 for DSD1 Other values: invalid
[3:0]	RW	sur_attr0	VHD2 link. 0x0: mixer 1 for DHD0 0x1: mixer 2 for DHD1 0x4: DSD5 Other values: invalid

CBMMIX1

CBMMIX1 is the mixer 1 priority configuration register (non-instant register). The register configuration takes effect only when the VSYNC signal is valid.

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Offset Address	Register Name	Total Reset Value
0x9E14	CBMMIX1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								mixer_prio5				mixer_prio4				mixer_prio3				mixer_prio2				mixer_prio1				mixer_prio0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:20]	RW	mixer_prio5	Priority 5 of the overlay layer of mixer 1. 0x0: no overlay layer 0x1: VHD0 0x3: VHD2 0x9: G0 0xD: G4 0xE: HC0 0xF: HC1 Other values: reserved
[19:16]	RW	mixer_prio4	Priority 4 of the overlay layer of mixer 1. 0x0: no overlay layer 0x1: VHD0 0x3: VHD2 0x9: G0 0xD: G4 0xE: HC0 0xF: HC1 Other values: invalid
[15:12]	RW	mixer_prio3	Priority 3 of the overlay layer of mixer 1. 0x0: no overlay layer 0x1: VHD0 0x3: VHD2 0x9: G0 0xD: G4 0xE: HC0 0xF: HC1 Other values: invalid

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[11:8]	RW	mixer_prio2	Priority 2 of the overlay layer of mixer 1. 0x0: no overlay layer 0x1: VHD0 0x3: VHD2 0x9: G0 0xD: G4 0xE: HC0 0xF: HC1 Other values: reserved
[7:4]	RW	mixer_prio1	Priority 1 of the overlay layer of mixer 1. 0x0: no overlay layer 0x1: VHD0 0x3: VHD2 0x9: G0 0xD: G4 0xE: HC0 0xF: HC1 Other values: invalid
[3:0]	RW	mixer_prio0	Priority 0 of the overlay layer of mixer 1. 0x0: no overlay layer 0x1: VHD0 0x2: VHD2 0x3: G0 0x4: G4 0x5: HC0 0x6: HC1 Other values: invalid

CBMMIX2

CBMMIX2 is the mixer 2 priority configuration register (non-instant register). The register configuration takes effect only when the VSYNC signal is valid.

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Offset Address	Register Name	Total Reset Value
0x9E18	CBMMIX2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								mixer_prio5				mixer_prio4				mixer_prio3				mixer_prio2				mixer_prio1				mixer_prio0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:20]	RW	mixer_prio5	Priority 5 of the overlay layer of mixer 2. 0x0: no overlay layer 0x2: VHD1 0x3: VHD2 0xA: G1 0xD: G4 0xE: HC0 0xF: HC1 Other values: invalid
[19:16]	RW	mixer_prio4	Priority 4 of the overlay layer of mixer 2. 0x0: no overlay layer 0x2: VHD1 0x3: VHD2 0xA: G1 0xD: G4 0xE: HC0 0xF: HC1 Other values: invalid
[15:12]	RW	mixer_prio3	Priority 3 of the overlay layer of mixer 2. 0x0: no overlay layer 0x1: VHD0 0x3: VHD2 0x9: G0 0xD: G4 0xE: HC0 0xF: HC1 Other values: invalid

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[11:8]	RW	mixer_prio2	Priority 2 of the overlay layer of mixer 2. 0x0: no overlay layer 0x2: VHD1 0x3: VHD2 0xA: G1 0xD: G4 0xE: HC0 0xF: HC1 Other values: invalid
[7:4]	RW	mixer_prio1	Priority 1 of the overlay layer of mixer 2. 0x0: no overlay layer 0x2: VHD1 0x3: VHD2 0xA: G1 0xD: G4 0xE: HC0 0xF: HC1 Other values: invalid
[3:0]	RW	mixer_prio0	Priority 0 of the overlay layer of mixer 2. 0x0: no overlay layer 0x2: VHD1 0x3: VHD2 0xA: G1 0xD: G4 0xE: HC0 0xF: HC1 Other values: invalid

CBMMIX3

CBMMIX3 is the mixer 3 priority configuration register (non-instant register). The register configuration takes effect only when the VSYNC signal is valid.

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Offset Address	Register Name	Total Reset Value
0x9E1C	CBMMIX3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												mixer_prio4				mixer_prio3				mixer_prio2				mixer_prio1				mixer_prio0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved.
[19:16]	RW	mixer_prio4	Priority 4 of the overlay layer of mixer 3. 0x0: no overlay layer 0x4: VSD0 0xB: G2 0xD: G4 0xE: HC0 0xF: HC1 Other values: reserved
[15:12]	RW	mixer_prio3	Priority 3 of the overlay layer of mixer 3. 0x0: no overlay layer 0x4: VSD0 0xB: G2 0xD: G4 0xE: HC0 0xF: HC1 Other values: reserved
[11:8]	RW	mixer_prio2	Priority 2 of the overlay layer of mixer 3. 0x0: no overlay layer 0x1: VSD0 0x2: G2 0x3: G4 0x4: HC0 0x5: HC1 Other values: reserved

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[7:4]	RW	mixer_prio1	Priority 1 of the overlay layer of mixer 3. 0x0: no overlay layer 0x4: VSD0 0xB: G2 0xD: G4 0xE: HC0 0xF: HC1 Other values: reserved
[3:0]	RW	mixer_prio0	Priority 0 of the overlay layer of mixer 3. 0x0: no overlay layer 0x4: VSD0 0xB: G2 0xD: G4 0xE: HC0 0xF: HC1 Other values: reserved

CBMMIX4

CBMMIX4 is the mixer 4 priority configuration register (non-instant register). The register configuration takes effect only when the VSYNC signal is valid.

Offset Address	Register Name	Total Reset Value
0x9E20	CBMMIX4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												mixer_prio4				mixer_prio3				mixer_prio2				mixer_prio1				mixer_prio0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved.
[19:16]	RW	mixer_prio4	Priority 4 of the overlay layer of mixer 4. 0x0: no overlay layer 0x5: VSD1 0xC: G3 0xD: G4 0xE: HC0 0xF: HC1 Other values: invalid

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[15:12]	RW	mixer_prio3	Priority 3 of the overlay layer of mixer 4. 0x0: no overlay layer 0x5: VSD1 0xC: G3 0xD: G4 0xE: HC0 0xF: HC1 Other values: invalid
[11:8]	RW	mixer_prio2	Priority 2 of the overlay layer of mixer 4. 0x0: no overlay layer 0x5: VSD1 0xC: G3 0xD: G4 0xE: HC0 0xF: HC1 Other values: invalid
[7:4]	RW	mixer_prio1	Priority 1 of the overlay layer of mixer 4. 0x0: no overlay layer 0x5: VSD1 0xC: G3 0xD: G4 0xE: HC0 0xF: HC1 Other values: invalid
[3:0]	RW	mixer_prio0	Priority 0 of the overlay layer of mixer 4. 0x0: no overlay layer 0x5: VSD2 0xC: G3 0xD: G4 0xE: HC0 0xF: HC1 Other values: invalid

DHDCTRL

DHDCTRL is the DHD global control register.

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CAUTION

You must configure this register before configuring DHDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xA000	DHDCTRL	0x0001_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intf_en	slave_md	multi32_md	reserved	fpga_lmt_en	fpga_lmt_width							reserved			clipen	reserved	gmmen	reserved		idv	ihs	ivs	iop	synm	intfb	intfdm						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31]	RW	intf_en	Display interface enable (instant field). Data is output over the interface only when this field is enabled. 0: disabled 1: enabled
[30]	RW	slave_md	Master/slave mode select when chips are cascaded. The first cascaded chip must be set to master mode and other chips are set to slave mode. If no chip is cascaded, the chip must be set to master mode. 0: master mode 1: slave mode
[29]	RW	multi32_md	32-region mode or 64-region mode when chips are cascaded. 0: 64-region mode 1: 32-region mode
[28]	-	reserved	Reserved.
[27]	RW	fpga_lmt_en	Debug field. As the frequency of the FPGA clock bus is limited, the 1080i picture cannot be displayed. After this bit is enabled, the picture with 1280-pixel width can be displayed over the 1080i interface. 0: disabled 1: enabled
[26:20]	RW	fpga_lmt_width	Debug field. When fpga_lmt_en is enabled, the active region width of the VDP interface depends on this field. The actual width of the active region is calculated as follows: Actual width of the active region = fpga_lmt_width x 16

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[19:17]	-	reserved	Reserved.
[16]	RW	clipen	Output clip enable (instant field). 0: disabled 1: enabled
[15]	-	reserved	Reserved.
[14]	RW	gmmen	Output gamma correction enable (instant field). 0: disabled 1: enabled
[13:11]	-	reserved	Reserved.
[10]	RW	idv	Output phase reverse enable for the data valid signal (instant field). 0: disabled 1: enabled
[9]	RW	ihs	Output phase reverse enable for the horizontal sync pulse (instant field). 0: disabled 1: enabled
[8]	RW	ivs	Output phase reverse enable for the vertical sync pulse (instant field). 0: disabled 1: enabled
[7]	RW	iop	Progressive or interlaced display (instant field). 0: interlaced display 1: progressive display
[6]	RW	synm	Sync mode (instant field). 0: timing label mode (such as BT.656) 1: sync signal mode (such as LCD display)
[5:4]	RW	intfb	Bit width mode of the output interface (instant field). 00: single-component mode (each clock outputs one component) 01: 2-component mode (each clock outputs two components) 10: 3-component mode (each clock outputs three components) 11: reserved
[3:0]	RW	intfdm	Interface data format (instant field). 0x0: YCbCr422 0x1–0xB: invalid 0xC: RGB888/YCbCr444 output Other values: invalid

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DHDVSYNC

DHDVSYNC is the DHD vertical timing register. In interlaced output mode, this register indicates the top vertical sync timing; in progressive output mode, this register indicates the frame vertical sync timing. The setting of this register takes effect immediately after configuration. That is, the timing of the VSYNC pin is affected immediately.

CAUTION

You must configure this register before configuring DHDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xA004	DHDVSYNC	0x0011_321B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vfb								vbb								vact											
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:20]	RW	vfb	In interlaced output mode: top vertical front blanking (TVFB) In progressive output mode: vertical front blanking (VFB) Unit: line
[19:12]	RW	vbb	In interlaced output mode: top vertical back blanking (TVBB) In progressive output mode: vertical back blanking (VBB) + vertical pulse width (VPW) Unit: line
[11:0]	RW	vact	In interlaced output mode: height of an active picture in the top field In progressive output format: height of an active picture in a frame. The register value is the actual value minus 1. Unit: line

DHDHSYNC1

DHDHSYNC1 is DHD horizontal timing register 1. In interlaced or progressive output mode, this register is the horizontal sync timing configuration register. The setting of this register takes effect immediately after configuration. That is, the timing of the HSYNC pin is affected immediately.

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CAUTION

You must configure this register before configuring DHDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xA008	DHDHSYNC1	0x00BF_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hbb																hact															
Reset	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	hbb	Horizontal back blanking (HBB). Unit: pixel
[15:0]	RW	hact	Number of horizontal pixels in an active region.

DHDHSYNC2

DHDHSYNC2 is DHD horizontal timing register 2. In interlaced or progressive output mode, this register is the horizontal sync timing configuration register. The setting of this register takes effect immediately after configuration. That is, the timing of the HSYNC pin is affected immediately.

CAUTION

You must configure this register before configuring DHDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xA00C	DHDHSYNC2	0x0000_020F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hmid																hfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	hmid	Width of the bottom vertical sync valid signal (in pixel).

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[15:0]	RW	hfb	Horizontal front blanking (HFB). Unit: pixel

DHDVPLUS

DHDVPLUS is the DHD interlaced bottom vertical timing register. In interlaced output mode, this register indicates the bottom vertical sync timing.

CAUTION

You must configure this register before configuring DHDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xA010	DHDVPLUS	0x0021_321B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				bvfb								bvbb								bvact											
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:20]	RW	bvfb	In interlaced output mode: bottom vertical front blanking (BVFB) Unit: line
[19:12]	RW	bvbb	In interlaced output mode: bottom vertical back blanking (BVBB) + VPW Unit: line
[11:0]	RW	bvact	In interlaced output mode: height of an active picture in the bottom field. The register value is the actual value minus 1. Unit: line

DHDPWR

DHDPWR is the DHD sync signal pulse width register.

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CAUTION

You must configure this register before configuring DHDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xA014	DHDPWR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								vpw								hpw															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	vpw	VPW minus 1. Unit: pixel
[15:0]	RW	hpw	Horizontal pulse width (HPW) minus 1. Unit: pixel

DHDVTTHD

DHDVTTHD is the DHD vertical timing threshold register (instant register). It can be used to set two thresholds for generating two interrupts separately.

Offset Address	Register Name	Total Reset Value
0xA01C	DHDVTTHD	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																thd1_mode	reserved			vtmgthd1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15]	RW	thd1_mode	Threshold 1 interrupt generation mode. 0: frame mode. The threshold count is in the unit of frame. 1: field mode. The threshold count is in the unit of field in interlaced display mode.
[14:13]	-	reserved	Reserved.

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[12:0]	RW	vtmgthd1	Vertical timing threshold 1. When the vertical timing counter reaches this threshold, the VOINTSTA[dhdvtthd_int1] interrupt is triggered.

DHDCLIPL

DHDCLIPL is the DHD clip lower threshold register (instant register).

Offset Address	Register Name	Total Reset Value
0xA040	DHDCLIPL	0x4100_4010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clipen	dfir_en	clipcl2										clipcl1							clipcl0											
Reset	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31]	RW	clipen	Clip enable. 0: disabled 1: enabled
[30]	RW	dfir_en	Horizontal chrominance down scaling enable. 0: disabled 1: enabled
[29:20]	RW	clipcl2	Lower threshold Y/R of component 2, unsigned integer.
[19:10]	RW	clipcl1	Lower threshold Cb/G of component 1, unsigned integer.
[9:0]	RW	clipcl0	Lower threshold Cr/B of component 0, unsigned integer.

DHDCLIPH

DHDCLIPH is the DHD clip upper threshold register (instant register). For example, the output data needs to be clipped in BT.656 output mode.

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Offset Address	Register Name	Total Reset Value
0xA044	DHDCLIPH	0x0EB0_00F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				clipch2												clipch1								clipch0							
Reset	0	0	0	0	1	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved.
[29:20]	RW	clipch2	Upper threshold Y/R of component 2, unsigned integer.
[19:10]	RW	clipch1	Upper threshold Cb/G of component 1, unsigned integer.
[9:0]	RW	clipch0	Upper threshold Cr/B of component 0, unsigned integer.

DHDSTATE

DHDSTATE is the DHD status register.

Offset Address	Register Name	Total Reset Value
0xA0F0	DHDSTATE	0x0000_0110

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													bottom_field	vblank	vback_blank
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved.
[2]	RO	bottom_field	DHD top/bottom field flag. 0: top field 1: bottom field
[1]	RO	vblank	DHD blanking region flag. 0: active region 1: blanking region

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[0]	RO	vback_blank	DHD back blanking region flag. 0: non-back blanking region 1: back blanking region

DSDCTRL

DSD is the DSD global control register.

CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xA800	DSDCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intf_en	reserved																				idv	ihs	ivs	iop	synm	intfb	intfdm				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	intf_en	Display interface enable (instant register). Data is output over the interface only when this bit is enabled. 0: disabled 1: enabled
[30:11]	-	reserved	Reserved.
[10]	RW	idv	Output phase reverse enable for the data valid signal (instant field). 0: disabled 1: enabled
[9]	RW	ihs	Output phase reverse enable for the horizontal sync pulse (instant field). 0: disabled 1: enabled

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[8]	RW	ivs	Output phase reverse enable for the vertical sync pulse (instant field). 0: disabled 1: enabled
[7]	RW	iop	Progressive or interlaced display (instant field). 0: interlaced display 1: progressive display
[6]	RW	synm	Sync mode (instant field). 0: timing label mode (such as BT.656) 1: sync signal mode (such as LCD display)
[5:4]	RW	intfb	Bit width mode of the output interface (instant field). 00: single-component mode (each clock outputs one component) Other values: invalid
[3:0]	RW	intfdm	Interface data format (instant field). 0x0: YCbCr422 Other values: invalid

DSDVSYNC

DSDVSYNC is the DSD vertical timing register. In interlaced output mode, this register indicates the top vertical sync timing; in progressive output mode, this register indicates the frame vertical sync timing. The setting of this register takes effect immediately after configuration. That is, the timing of the VSYNC pin is affected immediately.

CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xA804	DSDVSYNC	0x0011_511F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vfb								vbb								vact											
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.

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[27:20]	RW	vfb	In interlaced output mode: TVFB In progressive output mode: VFB Unit: line
[19:12]	RW	vbb	In interlaced output mode: TVBB In progressive output mode: VBB + VPW Unit: line
[11:0]	RW	vact	In interlaced output mode: height of an active picture in the top field In progressive output format: height of an active picture in a frame. The register value is the actual value minus 1. Unit: line

DSDHSYNC1

DSDHSYNC1 is DSD horizontal timing register 1. In interlaced or progressive output mode, this register is the horizontal sync timing configuration register. The setting of this register takes effect immediately after configuration. That is, the timing of the HSYNC pin is affected immediately.

CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xA808	DSDHSYNC1	0x0107_02CF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hbb																hact															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	hbb	HBB. Unit: pixel
[15:0]	RW	hact	Number of horizontal pixels in an active region.

DSDHSYNC2

DSDHSYNC2 is DSD horizontal timing register 2. In interlaced or progressive output mode, this register is the horizontal sync timing configuration register. The setting of this register

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takes effect immediately after configuration. That is, the timing of the HSYNC pin is affected immediately.

CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xA80C	DSDHSYNC2	0x0000_0017

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	hfb	HFB. Unit: pixel

DSDVPLUS

DSDVPLUS is the DSD interlaced bottom vertical timing register. In interlaced output mode, this register indicates the bottom vertical sync timing.

CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

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Offset Address	Register Name	Total Reset Value
0xA810	DSDVPLUS	0x0011_611F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				bvfb								bvbb								bvact											
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	1	0	0	0	0	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:20]	RW	bvfb	In interlaced output mode: BVFB Unit: line
[19:12]	RW	bvbb	In interlaced output mode: BVBB + VPW Unit: line
[11:0]	RW	bvact	In interlaced output mode: height of an active picture in the bottom field. The register value is the actual value minus 1. Unit: line

DSDPWR

DSDPWR is the DSD sync signal pulse width register.

CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xA814	DSDPWR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								vpw								hpw															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	vpw	VPW minus 1. Unit: pixel

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[15:0]	RW	hpw	HPW minus 1. Unit: pixel

DSDVTTHD

DSDVTTHD is the DSD vertical timing threshold register (instant register). It can be used to set two thresholds for generating two interrupts separately.

Offset Address	Register Name	Total Reset Value
0xA81C	DSDVTTHD	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																thd1_mode	reserved			vtmgthd1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15]	RW	thd1_mode	Threshold 1 interrupt generation mode. 0: frame mode. The threshold count is in the unit of frame. 1: field mode. The threshold count is in the unit of field in interlaced display mode.
[14:13]	-	reserved	Reserved.
[12:0]	RW	vtmgthd1	Vertical timing threshold 1. When the vertical timing counter reaches this threshold, the VOINTSTA[dsdvtthd_int1] interrupt is triggered.

DSDCLIPL

DSDCLIPL is the DSD clip lower threshold register (instant register).

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Offset Address	Register Name	Total Reset Value
0xA840	DSDCLIPL	0x4010_1010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clipen	dfir_en	clipcl2										clipcl1												clipcl0							
Reset	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31]	RW	clipen	Output clip enable (instant field). 0: disabled 1: enabled
[30]	RW	dfir_en	Horizontal chrominance down scaling enable. 0: disabled 1: enabled
[29:20]	RW	clipcl2	Lower threshold Y/R of component 2, unsigned integer.
[19:10]	RW	clipcl1	Lower threshold Cb/G of component 1, unsigned integer.
[9:0]	RW	clipcl0	Lower threshold Cr/B of component 0, unsigned integer.

DSDCLIPH

DSDCLIPH is the DSD clip upper threshold register (instant register). For example, the output data needs to be clipped in BT.656 output mode.

Offset Address	Register Name	Total Reset Value
0xA844	DSDCLIPH	0x00EB_F0F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		clipch2										clipch1												clipch0							
Reset	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved.
[29:20]	RW	clipch2	Upper threshold Y/R of component 2, unsigned integer.
[19:10]	RW	clipch1	Upper threshold Cb/G of component 1, unsigned integer.
[9:0]	RW	clipch0	Upper threshold Cr/B of component 0, unsigned integer.

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DSDSTATE

DSDSTATE is the DSD status register.

Offset Address	Register Name	Total Reset Value
0xA8F0	DSDSTATE	0x0000_0110

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													bottom_field	vblank	vback_blank
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved.
[2]	RW	bottom_field	DSD top/bottom field flag. 0: top field 1: bottom field
[1]	RW	vblank	DSD blanking region flag. 0: active region 1: blanking region
[0]	RW	vback_blank	DSD back blanking region flag. 0: non-back blanking region 1: back blanking region

DSD1CTRL

DSD1CTRL is the DSD1 global control register.

CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

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Offset Address	Register Name	Total Reset Value
0xAC00	DSD1CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intf_en	reserved																				idv	ihs	ivs	iop	synm	intfb		intfdm			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	intf_en	Display interface enable (instant register). Data is output over the interface only when this bit is enabled. 0: disabled 1: enabled
[30:11]	-	reserved	Reserved.
[10]	RW	idv	Output phase reverse enable for the data valid signal (instant field). 0: disabled 1: enabled
[9]	RW	ihs	Output phase reverse enable for the horizontal sync pulse (instant field). 0: disabled 1: enabled
[8]	RW	ivs	Output phase reverse enable for the vertical sync pulse (instant field). 0: disabled 1: enabled
[7]	RW	iop	Progressive or interlaced display (instant field). 0: interlaced display 1: progressive display
[6]	RW	synm	Sync mode (instant field). 0: timing label mode (such as BT.656) 1: sync signal mode (such as LCD display)
[5:4]	RW	intfb	Bit width mode of the output interface (instant field). 00: single-component mode (each clock outputs one component) Other values: reserved
[3:0]	RW	intfdm	Interface data format (instant field). 0x0: YCbCr422 Other values: reserved

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DSD1VSYNC

DSD1VSYNC is the DSD1 vertical timing register. In interlaced output mode, this register indicates the top vertical sync timing; in progressive output mode, this register indicates the frame vertical sync timing. The setting of this register takes effect immediately after configuration. That is, the timing of the VSYNC pin is affected immediately.

CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xAC04	DSD1VSYNC	0x0011_511F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vfb								vbb								vact											
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:20]	RW	vfb	In interlaced output mode: TVFB In progressive output mode: VFB Unit: line
[19:12]	RW	vbb	In interlaced output mode: TVBB In progressive output mode: VBB + VPW Unit: line
[11:0]	RW	vact	In interlaced output mode: height of an active picture in the top field In progressive output format: height of an active picture in a frame. The register value is the actual value minus 1. Unit: line

DSD1HSYNC1

DSD1HSYNC1 is DSD1 horizontal timing register 1. In interlaced or progressive output mode, this register is the horizontal sync timing configuration register. The setting of this register takes effect immediately after configuration. That is, the timing of the HSYNC pin is affected immediately.

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CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xAC08	DSD1HSYNC1	0x0107_02CF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hbb																hact															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	hbb	HBB. Unit: pixel
[15:0]	RW	hact	Number of horizontal pixels in an active region.

DSD1HSYNC2

DSD1HSYNC2 is DSD1 horizontal timing register 2. In interlaced or progressive output mode, this register is the horizontal sync timing configuration register. The setting of this register takes effect immediately after configuration. That is, the timing of the HSYNC pin is affected immediately.

CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xAC0C	DSD1HSYNC2	0x0000_0017

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.

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[15:0]	RW	hfb	HFB. Unit: pixel

DSD1VPLUS

DSD1VPLUS is the DSD1 bottom vertical sync timing register in interlaced output mode.

CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xAC10	DSD1VPLUS	0x0011_611F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				bvfb								bvbb								bvact											
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	1	0	0	0	0	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:20]	RW	bvfb	In interlaced output mode: BVFB Unit: line
[19:12]	RW	bvbb	In interlaced output mode: BVBB + VPW Unit: line
[11:0]	RW	bvact	In interlaced output mode: height of an active picture in the bottom field. The register value is the actual value minus 1. Unit: line

DSD1PWR

DSD1PWR is the DSD1 sync signal pulse width register.

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CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xAC14	DSD1PWR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								vpw								hpw															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	vpw	VPW minus 1. Unit: pixel
[15:0]	RW	hpw	HPW minus 1. Unit: pixel

DSD1VTTHD

DSD1VTTHD is the DSD1 vertical timing threshold register (instant register). It can be used to set two thresholds for generating two interrupts separately.

Offset Address	Register Name	Total Reset Value
0xAC1C	DSD1VTTHD	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																thd1_mode	reserved			vtmgthd1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15]	RW	thd1_mode	Threshold 1 interrupt generation mode. 0: frame mode. The threshold count is in the unit of frame. 1: field mode. The threshold count is in the unit of field in interlaced display mode.

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[14:13]	-	reserved	Reserved.
[12:0]	RW	vtmgthd1	Vertical timing threshold 1. When the vertical timing counter reaches this threshold, the VOINTSTA[dsdvtthd_int1] interrupt is triggered.

DSD1CLIPL

DSD1CLIPL is the DSD1 clip lower threshold register (instant register).

Offset Address	Register Name	Total Reset Value
0xAC40	DSD1CLIPL	0x4010_1010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clipen	dfir_en	clipcl2										clipcl1										clipcl0									
Reset	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31]	RW	clipen	Output clip enable (instant field). 0: disabled 1: enabled
[30]	RW	dfir_en	Horizontal chrominance down scaling enable. 0: disabled 1: enabled
[29:20]	RW	clipcl2	Lower threshold Y/R of component 2, unsigned integer.
[19:10]	RW	clipcl1	Lower threshold Cb/G of component 1, unsigned integer.
[9:0]	RW	clipcl0	Lower threshold Cr/B of component 0, unsigned integer.

DSD1CLIPH

DSD1CLIPH is the DSD1 clip upper threshold register (instant register). For example, the output data needs to be clipped in BT.656 output mode.

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Offset Address	Register Name	Total Reset Value
0xAC44	DSD1CLIPH	0x00EB_F0F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				clipch2												clipch1								clipch0							
Reset	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved.
[29:20]	RW	clipch2	Upper threshold Y/R of component 2, unsigned integer.
[19:10]	RW	clipch1	Upper threshold Cb/G of component 1, unsigned integer.
[9:0]	RW	clipch0	Upper threshold Cr/B of component 0, unsigned integer.

DSD1STATE

DSD1STATE is the DSD1 status register.

Offset Address	Register Name	Total Reset Value
0xACF0	DSD1STATE	0x0000_0110

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													bottom_field	vblank	vback_blank
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved.
[2]	RW	bottom_field	DSD1 top/bottom field flag. 0: top field 1: bottom field
[1]	RW	vblank	DSD1 blanking region flag. 0: active region 1: blanking region

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[0]	RW	vback_blank	DSD1 back blanking region flag. 0: non-back blanking region 1: back blanking region

DATE_COEFF0

DATE_COEFF0 is the DATE norm parameter configuration register.

Offset Address	Register Name	Total Reset Value
0xC200	DATE_COEFF0	0x5284_14FC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clpf_sel		dis_ire	reserved			scanline	rgb_en	vbi_lpf_en	fm_sel	style_sel				sync_mode_sel		sync_mode_scart	length_sel	agc_amp_sel	luma_dl				reserved	oversam_en		lunt_en	oversam2_en	chlp_en	sylp_en	chgain_en	tt_seq
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	clpf_sel	Bandwidth select of the chrominance low-pass filter. 00: 1.1 MHz (NTSC) 01: 1.3 MHz (PAL) 10: 1.6 MHz (for test) 11: reserved
[29]	RW	dis_ire	For the (M) NTSC and (M, N) PAL norms, the black level is 7.5 IRE higher than the blanking level; for other norms, the black level is equal to the blanking level. This bit controls whether the black level is 7.5 IRE higher than the blanking level. 0: The black level is 7.5 IRE higher than the blanking level. 1: The black level is equal to the blanking level.
[28:26]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[25]	RW	scanline	Number of scanned lines in each frame based on norms. For the (M) NTSC, NTSC-J, and (M) PAL norm, each line contains 525 lines; for the (B, D, J, H, I) PAL, (N) PAL, and (Nc) PAL norms, each frame contains 625 lines. 0: 525 lines in a frame 1: 625 lines in a frame

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[24]	RW	rgb_en	When intf_sel is set to 100, this bit determines whether the component signal is RGB or YPbPr. 0: YPbPr 1: RGB
[23]	RW	vbi_lpf_en	VBI data low-pass filtering enable. 0: disabled 1: enabled
[22]	RW	fm_sel	FMSECAM frequency modulation select. 0: sin used for SECAM frequency modulation 1: cos used for SECAM frequency modulation
[21:18]	RW	style_sel	CVBS/S-Video output signal norm when this bit works with the scanline bit. When the scanline bit is 0 (525 scanned lines in a frame), the definition of the style_sel bit is as follows: 0x1: (M) NTSC 0x2: NTSC-J 0x4: (M) PAL Other values: reserved When the scanline bit is 1 (625 scanned lines in a frame), the definition of the style_sel bit is as follows: 0x1: (B, D, G, H, I) PAL 0x2: (N) PAL 0x4: (Nc) PAL 0x8: SECAM Other values: reserved
[17:16]	RW	sync_mode_sel	bit[17]: specifies whether there are sync signals in three channels during component output. This bit takes effect only when the sync_mode_scart bit is set to 0. bit[17] is valid only when the intf_sel is set to 100 (component output enabled). The definition of bit[17] is as follows: 0: Only one channel contains sync signals using component output. 1: Three channels contain sync signals during component output. When bit[17] is set to 0, the sync channel must be the Y channel for YPbPr output and G channel for RGB output. bit[16]: specifies whether there are blanking radixes during RGB output. bit[16] is valid only when the intf_sel is set to 100 and the rgb_en bit is set to 1. The definition of bit[16] is as follows: 0: There are no blanking radixes during RGB output. 1: There are blanking radixes during RGB output.

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[15]	RW	sync_mode_scart	Overlay sync control of the components of three channels. 0: Component sync output is configured based on sync_mode_sel[1]. 1: The components of the three channels are not overlaid and synchronized. In this case, sync_mode_sel bit[1] must be set to 0.
[14]	RW	length_sel	Active width of each video line (in pixel). 0: output according to the active line width in BT.601 mode 1: output according to the active line width in BT.470 mode. When this bit is set to 0, the active width of the line is 720 pixels. When this bit is set to 1, the active width of the line is 704 pixels for the 625-line norm or 712 pixels for the 525-line norm. Currently, the BT.601 mode and BT.470 mode cannot be changed dynamically. You can change the mode only after reset. The BT.601 mode is recommended and this mode is the default value after power-on reset.
[13]	RW	agc_amp_sel	AGC pulse select. 0: The AGC pulse is generated based on the on-chip default value (recommended). 1: The AGC pulse is generated based on DATE_COEFF1[amp_outside].
[12:9]	RW	luma_dl	Forward or backward offset of the chrominance signal relative to the luminance signal, in the unit of half a pixel width. bit[12]: offset direction of the chrominance signal relative to the luminance signal. 0: backward offset 1: forward offset bit[11:9]: absolute offset of the chrominance signal relative to the luminance signal. The value is in binary format and ranges from 0 to 7. 000: The chrominance signal is aligned with the luminance signal. No adjustment is required. 001–111: The chrominance signal offsets from the luminance signal forward or backward by one to seven units.
[8]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[7:6]	RW	oversam_en	Level-1 oversampling enable. Both the luminance oversampling and chrominance oversampling are controlled. bit[7]: luminance oversampling enable. 0: disabled 1: enabled bit[6]: chrominance oversampling enable. 0: disabled 1: enabled

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[5]	RW	lunt_en	Luminance notch enable. 0: disabled 1: enabled
[4]	RW	oversam2_en	Level-2 oversampling enable. Both the luminance channel and chrominance channel are controlled. 0: disabled 1: enabled
[3]	RW	chlp_en	Chrominance low-pass filtering enable. 0: disabled 1: enabled
[2]	RW	sylp_en	Sync low-pass filtering enable. 0: disabled 1: enabled
[1]	RW	chgain_en	Chrominance gain enable. 0: disabled 1: enabled
[0]	RW	tt_seq	Sequence of transmitting the bits of the teletext data. 0: from upper bits to lower bits 1: from lower bits to upper bits

DATE_COEFF1

DATE_COEFF1 is the DATE amplitude configuration register.

Offset Address	Register Name	Total Reset Value
0xC204	DATE_COEFF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c_gain				cvbs_limit_en	wss_seq	vps_seq	cgms_seq	cc_seq	c_limit_en	amp_outside									date_test_en	date_test_mode	dac_test										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	c_gain	Adjustment of the chrominance sync gain amplitude.

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[28]	RW	cvbs_limit_en	CVBS amplitude limit enable. 0: disabled 1: enabled
[27]	RW	wss_seq	Sequence of transmitting the bits of the WSS data. 0: from upper bits to lower bits 1: from lower bits to upper bits
[26]	RW	vps_seq	Sequence of transmitting the bits of the VPS data. 0: from upper bits to lower bits 1: from lower bits to upper bits
[25]	RW	cgms_seq	Sequence of transmitting the bits of the CGMS data. 0: from upper bits to lower bits 1: from lower bits to upper bits
[24]	RW	cc_seq	Sequence of transmitting the bits of the closed caption data. 0: from upper bits to lower bits 1: from lower bits to upper bits
[23]	RW	c_limit_en	Chrominance amplitude limit enable. 0: disabled 1: enabled
[22:13]	RW	amp_outside	Pulse amplitude input of the external AGC.
[12]	RW	date_test_en	Test valid signal. 0: invalid 1: valid
[11:10]	RW	date_test_mode	Test mode signal.
[9:0]	RW	dac_test	DAC test value input.

DATE_COEFF7

DATE_COEFF7 is a DATE teletext configuration register.

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Offset Address	Register Name	Total Reset Value
0xC21C	DATE_COEFF7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt22_enf1	tt21_enf1	tt20_enf1	tt19_enf1	tt18_enf1	tt17_enf1	tt16_enf1	tt15_enf1	tt14_enf1	tt13_enf1	tt12_enf1	tt11_enf1	tt10_enf1	tt09_enf1	tt08_enf1	tt07_enf1	tt22_enf2	tt21_enf2	tt20_enf2	tt19_enf2	tt18_enf2	tt17_enf2	tt16_enf2	tt15_enf2	tt14_enf2	tt13_enf2	tt12_enf2	tt11_enf2	tt10_enf2	tt09_enf2	tt08_enf2	tt07_enf2
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	tt22_enf1	Control of the teletext in line 22 in the odd field. 0: disabled 1: enabled
[30]	RW	tt21_enf1	Control of the teletext in line 21 in the odd field. 0: disabled 1: enabled
[29]	RW	tt20_enf1	Control of the teletext in line 20 in the odd field. 0: disabled 1: enabled
[28]	RW	tt19_enf1	Control of the teletext in line 19 in the odd field. 0: disabled 1: enabled
[27]	RW	tt18_enf1	Control of the teletext in line 18 in the odd field. 0: disabled 1: enabled
[26]	RW	tt17_enf1	Control of the teletext in line 17 in the odd field. 0: disabled 1: enabled
[25]	RW	tt16_enf1	Control of the teletext in line 16 in the odd field. 0: disabled 1: enabled
[24]	RW	tt15_enf1	Control of the teletext in line 15 in the odd field. 0: disabled 1: enabled
[23]	RW	tt14_enf1	Control of the teletext in line 14 in the odd field. 0: disabled 1: enabled

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[22]	RW	tt13_enf1	Control of the teletext in line 13 in the odd field. 0: disabled 1: enabled
[21]	RW	tt12_enf1	Control of the teletext in line 12 in the odd field.0: disabled 1: enabled
[20]	RW	tt11_enf1	Control of the teletext in line 11 in the odd field.0: disabled 1: enabled
[19]	RW	tt10_enf1	Control of the teletext in line 10 in the odd field. 0: disabled 1: enabled
[18]	RW	tt09_enf1	Control of the teletext in line 9 in the odd field. 0: disabled 1: enabled
[17]	RW	tt08_enf1	Control of the teletext in line 8 in the odd field. 0: disabled 1: enabled
[16]	RW	tt07_enf1	Control of the teletext in line 7 in the odd field. 0: disabled 1: enabled
[15]	RW	tt22_enf2	Control of teletext in line 22 in the even field. 0: disabled 1: enabled
[14]	RW	tt21_enf2	Control of teletext in line 21 in the even field. 0: disabled 1: enabled
[13]	RW	tt20_enf2	Control of teletext in line 20 in the even field. 0: disabled 1: enabled
[12]	RW	tt19_enf2	Control of teletext in line 19 in the even field. 0: disabled 1: enabled
[11]	RW	tt18_enf2	Control of teletext in line 18 in the even field. 0: disabled 1: enabled
[10]	RW	tt17_enf2	Control of teletext in line 17 in the even field. 0: disabled 1: enabled

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[9]	RW	tt16_enf2	Control of teletext in line 16 in the even field. 0: disabled 1: enabled
[8]	RW	tt15_enf2	Control of teletext in line 15 in the even field. 0: disabled 1: enabled
[7]	RW	tt14_enf2	Control of teletext in line 14 in the even field. 0: disabled 1: enabled
[6]	RW	tt13_enf2	Control of teletext in line 13 in the even field. 0: disabled 1: enabled
[5]	RW	tt12_enf2	Control of teletext in line 12 in the even field. 0: disabled 1: enabled
[4]	RW	tt11_enf2	Control of teletext in line 11 in the even field. 0: disabled 1: enabled
[3]	RW	tt10_enf2	Control of teletext in line 10 in the even field. 0: disabled 1: enabled
[2]	RW	tt09_enf2	Control of teletext in line 9 in the even field. 0: disabled 1: enabled
[1]	RW	tt08_enf2	Control of teletext in line 8 in the even field. 0: disabled 1: enabled
[0]	RW	tt07_enf2	Control of teletext in line 7 in the even field. 0: disabled 1: enabled

DATE_COEFF8

DATE_COEFF8 is a DATE teletext configuration register.

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Offset Address	Register Name	Total Reset Value
0xC220	DATE_COEFF8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt_staddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tt_staddr	Start address of the teletext data.

DATE_COEFF9

DATE_COEFF9 is a DATE teletext configuration register.

Offset Address	Register Name	Total Reset Value
0xC224	DATE_COEFF9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt_edaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tt_edaddr	End address of the teletext data.

DATE_COEFF10

DATE_COEFF10 is a DATE teletext configuration register.

CAUTION

The teletext function is supported in both 625-line mode and 525-line mode. The tt_mode bit is set to 01 in 625-line mode or 10 in 525-line mode.

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Offset Address	Register Name	Total Reset Value
0xC228	DATE_COEFF10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt_ready	reserved																			nabts_100ire	full_page	tt_highest	tt_mode	tt_pktoff							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	tt_ready	When software sets related parameters through the bus, this bit is set to 1 and the teletext module starts to work. When the teletext module completes data transfer, this bit is set to 0. The bit status can be queried through software for the next configuration.
[30:13]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[12]	RW	nabts_100ire	NABTS-NTSC data height. 0: 70 IRE 1: 100 IRE
[11]	RW	full_page	Teletext data transmission mode. 0: normal mode. The teletext data is transmitted from the blanking line. 1: full page mode. The teletext data can also be transmitted from the active video region.
[10]	RW	tt_highest	Teletext priority control. 0: The teletext data has the highest priority. 1: The teletext data has the lowest priority.
[9:8]	RW	tt_mode	Teletext mode. This field is set to 01 in 625-line mode, indicating WST-PAL. This field is set to 10 in 525-line mode, indicating NABTS-NTSC.
[7:0]	RW	tt_pktoff	Offset address of the teletext packet.

DATE_COEFF11

DATE_COEFF11 is a DATE closed caption configuration register.

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Offset Address	Register Name	Total Reset Value
0xC22C	DATE_COEFF11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										cc_enf1	cc_enf2	date_clf1								date_clf2											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RW	reserved	Reserved.
[21]	RW	cc_enf1	Closed caption odd field enable. 0: disabled 1: enabled
[20]	RW	cc_enf2	Closed caption even field enable. 0: disabled 1: enabled
[19:10]	RW	date_clf1	Configuration line of the closed caption odd field.
[9:0]	RW	date_clf2	Configuration line of the closed caption even field.

DATE_COEFF12

DATE_COEFF12 is a DATE closed caption configuration register.

Offset Address	Register Name	Total Reset Value
0xC230	DATE_COEFF12	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cc_f1data																cc_f2data															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cc_f1data	Data of the closed caption odd field.
[15:0]	RW	cc_f2data	Data of the closed caption even field.

DATE_COEFF13

DATE_COEFF13 is a DATE CGMS configuration register.

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Offset Address	Register Name	Total Reset Value
0xC234	DATE_COEFF13	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										cg_enf1	cg_enf2	cg_f1data																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[21]	RW	cg_enf1	CGMS odd field enable. 0: disabled 1: enabled
[20]	RW	cg_enf2	CGMS even field enable. 0: disabled 1: enabled
[19:0]	RW	cg_f1data	Data of the CGMS odd field.

DATE_COEFF14

DATE_COEFF14 is a DATE CGMS configuration register.

Offset Address	Register Name	Total Reset Value
0xC238	DATE_COEFF14	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cg_f2data																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[19:0]	RW	cg_f2data	Data of the CGMS even field.

DATE_COEFF15

DATE_COEFF15 is a DATE WSS configuration register.

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CAUTION

The WSS is available only in 625-line mode and is fixed at line 23.

Offset Address	Register Name	Total Reset Value
0xC23C	DATE_COEFF15	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	wss_en	wss_data													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[14]	RW	wss_en	WSS enable. 0: disabled 1: enabled
[13:0]	RW	wss_data	WSS data.

DATE_COEFF16

DATE_COEFF16 is a DATE VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC240	DATE_COEFF16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							vps_en	vps_data																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[24]	RW	vps_en	VPS enable. 0: disabled 1: enabled
[23:0]	RW	vps_data	VPS data from bit 23 to bit 0. Bit 0 is the LSB.

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DATE_COEFF17

DATE_COEFF17 is a DATE VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC244	DATE_COEFF17	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vps_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	vps_data	VPS data from bit 55 to bit 24. Bit 0 is the LSB.

DATE_COEFF18

DATE_COEFF18 is a DATE VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC248	DATE_COEFF18	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vps_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	vps_data	VPS data from bit 87 to bit 56. Bit 0 is the LSB.

DATE_COEFF19

DATE_COEFF19 is a DATE VPS configuration register.

CAUTION

The VPS is available only in 625-line mode and is fixed at line 16.

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Offset Address	Register Name	Total Reset Value
0xC24C	DATE_COEFF19	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				vps_data			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[15:0]	RW	vps_data	VPS data from bit 103 to bit 88. Bit 0 is the LSB.

DATE_COEFF20

DATE_COEFF20 is a DATE teletext configuration register.

Offset Address	Register Name	Total Reset Value
0xC250	DATE_COEFF20	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved							tt06_enf1	tt06_enf2	tt05_enf2	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[2]	RW	tt06_enf1	Control of teletext in line 6 in the odd field. 0: disabled 1: enabled
[1]	RW	tt06_enf2	Control of teletext in line 6 in the even field. 0: disabled 1: enabled
[0]	RW	tt05_enf2	Control of teletext in line 5 in the even field. 0: disabled 1: enabled

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DATE_COEFF21

DATE_COEFF21 is the DATE output matrix control register.

Offset Address	Register Name	Total Reset Value
0xC254	DATE_COEFF21	0x0060_00A1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									dac5_in_sel			reserved	dac4_in_sel			reserved	dac3_in_sel			reserved	dac2_in_sel			reserved	dac1_in_sel			reserved	dac0_in_sel		
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1

Bits	Access	Name	Description
[31:23]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[22:20]	RW	dac5_in_sel	DAC5 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[19]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[18:16]	RW	dac4_in_sel	DAC4 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[15]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.

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[14:12]	RW	dac3_in_sel	DAC3 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[11]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[10:8]	RW	dac2_in_sel	DAC2 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[7]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[6:4]	RW	dac1_in_sel	DAC1 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[3]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.

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[2:0]	RW	dac0_in_sel	DAC0 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0

DATE_COEFF22

DATE_COEFF22 is the DATE DTO initial phase configuration register.

Offset Address	Register Name	Total Reset Value
0xC258	DATE_COEFF22	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					video_phase_delta										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[10:0]	RW	video_phase_delta	DTO initial phase.

DATE_COEFF23

DATE_COEFF23 is the DATE video output delay configuration register.

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Offset Address	Register Name	Total Reset Value
0xC25C	DATE_COEFF23	0x0065_4321

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									dac5_out_dly			reserved	dac4_out_dly			reserved	dac3_out_dly			reserved	dac2_out_dly			reserved	dac1_out_dly			reserved	dac0_out_dly		
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1

Bits	Access	Name	Description
[31:23]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[22:20]	RW	dac5_out_dly	DAC5 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.
[19]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[18:16]	RW	dac4_out_dly	DAC4 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.
[15]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[14:12]	RW	dac3_out_dly	DAC3 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.
[11]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[10:8]	RW	dac2_out_dly	DAC2 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.
[7]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[6:4]	RW	dac1_out_dly	DAC1 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.
[3]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.

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[2:0]	RW	dac0_out_dly	DAC0 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.

DATE_ISRMASK

DATE_ISRMASK is the DATE interrupt mask register.

Offset Address	Register Name	Total Reset Value
0xC280	DATE_ISRMASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[0]	RW	tt_mask	Teletext interrupt mask. 0: enabled 1: masked

DATE_ISRSTATE

DATE_ISRSTATE is the DATE interrupt status register.

Offset Address	Register Name	Total Reset Value
0xC284	DATE_ISRSTATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.

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[0]	W1C	tt_status	Teletext interrupt flag. After the DATE module reads all the teletext data, the bit is set to 1. Writing 1 to this bit clears this bit.

DATE_ISR

DATE_ISR is the DATE interrupt register.

Offset Address	Register Name	Total Reset Value
0xC288	DATE_ISR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[0]	RW	tt_int	Teletext interrupt. It is the interrupt status after tt_status is masked by tt_mask. 0: No interrupt is generated. 1: An interrupt is generated.

DATE_VERSION

DATE_VERSION is the DATE version register.

Offset Address	Register Name	Total Reset Value
0xC290	DATE_VERSION	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:0]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.

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DATE1_COEFF0

DATE1_COEFF0 is the DATE1 norm parameter configuration register.

Offset Address	Register Name	Total Reset Value
0xC400	DATE1_COEFF0	0x5284_14FC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clpf_sel		dis_ire	reserved			scanline	rgb_en	vbi_lpf_en	fm_sel	style_sel				sync_mode_sel		sync_mode_scart	length_sel	agc_amp_sel	luma_dl				reserved	oversam_en		lunt_en	oversam2_en	chlp_en	sylp_en	chgain_en	tt_seq
Reset	0	1	0	1	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	1	0	0

Bits	Access	Name	Description
[31:30]	RW	clpf_sel	Bandwidth select of the chrominance low-pass filter. 00: 1.1 MHz (NTSC) 01: 1.3 MHz (PAL) 10: 1.6 MHz (for test) 11: reserved
[29]	RW	dis_ire	For the (M) NTSC and (M, N) PAL norms, the black level is 7.5 IRE higher than the blanking level; for other norms, the black level is equal to the blanking level. This bit controls whether the black level is 7.5 IRE higher than the blanking level. 0: The black level is 7.5 IRE higher than the blanking level. 1: The black level is equal to the blanking level.
[28:26]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[25]	RW	scanline	Number of scanned lines in each frame based on norms. For the (M) NTSC, NTSC-J, and (M) PAL norm, each line contains 525 lines; for the (B, D, J, H, I) PAL, (N) PAL, and (Nc) PAL norms, each frame contains 625 lines. 0: 525 lines in a frame 1: 625 lines in a frame
[24]	RW	rgb_en	When intf_sel is set to 100, this bit determines whether the component signal is RGB or YPbPr. 0: YPbPr 1: RGB

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[23]	RW	vbi_lpf_en	VBI data low-pass filtering enable. 0: disabled 1: enabled
[22]	RW	fm_sel	FMSECAM frequency modulation select. 0: sin used for SECAM frequency modulation 1: cos used for SECAM frequency modulation
[21:18]	RW	style_sel	CVBS/S-Video output signal norm when this bit works with the scanline bit. When the scanline bit is 0 (525 scanned lines in a frame), the definition of the style_sel bit is as follows: 0x1: (M) NTSC 0x2: NTSC-J 0x4: (M) PAL Other values: reserved When the scanline bit is 1 (625 scanned lines in a frame), the definition of the style_sel bit is as follows: 0x1: (B, D, G, H, I) PAL 0x2: (N) PAL 0x4: (Nc) PAL 0x8: SECAM Other values: reserved
[17:16]	RW	sync_mode_sel	bit[17]: specifies whether there are sync signals in three channels during component output. This bit takes effect only when the sync_mode_scart bit is set to 0. bit[17] is valid only when the intf_sel is set to 100 (component output enabled). The definition of bit[17] is as follows: 0: Only one channel contains sync signals using component output. 1: Three channels contain sync signals during component output. When bit[17] is set to 0, the sync channel must be the Y channel for YPbPr output and G channel for RGB output. bit[16]: specifies whether there are blanking radixes during RGB output. bit[16] is valid only when the intf_sel is set to 100 and the rgb_en bit is set to 1. The definition of bit[16] is as follows: 0: There are no blanking radixes during RGB output. 1: There are blanking radixes during RGB output.
[15]	RW	sync_mode_scart	Overlay sync control of the components of three channels. 0: Component sync output is configured based on sync_mode_sel[1]. 1: The components of the three channels are not overlaid and synchronized. In this case, sync_mode_sel bit[1] must be set to 0.

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[14]	RW	length_sel	Active width of each video line (in pixel). 0: output according to the active line width in BT.601 mode 1: output according to the active line width in BT.470 mode. When this bit is set to 0, the active width of the line is 720 pixels. When this bit is set to 1, the active width of the line is 704 pixels for the 625-line norm or 712 pixels for the 525-line norm. Currently, the BT.601 mode and BT.470 mode cannot be changed dynamically. You can change the mode only after reset. The BT.601 mode is recommended and this mode is the default value after power-on reset.
[13]	RW	agc_amp_sel	AGC pulse select. 0: The AGC pulse is generated based on the on-chip default value (recommended). 1: The AGC pulse is generated based on DATE_COEFF1[amp_outside].
[12:9]	RW	luma_dl	Forward or backward offset of the chrominance signal relative to the luminance signal, in the unit of half a pixel width. bit[12]: offset direction of the chrominance signal relative to the luminance signal. 0: backward offset 1: forward offset bit[11:9]: absolute offset of the chrominance signal relative to the luminance signal. The value is in binary format and ranges from 0 to 7. 000: The chrominance signal is aligned with the luminance signal. No adjustment is required. 001–111: The chrominance signal offsets from the luminance signal forward or backward by one to seven units.
[8]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[7:6]	RW	oversam_en	Level-1 oversampling enable. Both the luminance oversampling and chrominance oversampling are controlled. bit[7]: luminance oversampling enable. 0: disabled 1: enabled bit[6]: chrominance oversampling enable. 0: disabled 1: enabled
[5]	RW	lunt_en	Luminance notch enable. 0: disabled 1: enabled

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[4]	RW	oversam2_en	Level-2 oversampling enable. Both the luminance channel and chrominance channel are controlled. 0: disabled 1: enabled
[3]	RW	chlp_en	Chrominance low-pass filtering enable. 0: disabled 1: enabled
[2]	RW	sylp_en	Sync low-pass filtering enable. 0: disabled 1: enabled
[1]	RW	chgain_en	Chrominance gain enable. 0: disabled 1: enabled
[0]	RW	tt_seq	Sequence of transmitting the bits of the teletext data. 0: from upper bits to lower bits 1: from lower bits to upper bits

DATE1_COEFF1

DATE1_COEFF1 is the DATE1 amplitude configuration register.

Offset Address	Register Name	Total Reset Value
0xC404	DATE1_COEFF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c_gain			cvbs_limit_en	wss_seq	vps_seq	cgms_seq	cc_seq	c_limit_en	amp_outside										date_test_en	date_test_mode	dac_test										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	c_gain	Adjustment of the chrominance sync gain amplitude.
[28]	RW	cvbs_limit_en	CVBS amplitude limit enable. 0: disabled 1: enabled

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[27]	RW	wss_seq	Sequence of transmitting the bits of the WSS data. 0: from upper bits to lower bits 1: from lower bits to upper bits
[26]	RW	vps_seq	Sequence of transmitting the bits of the VPS data. 0: from upper bits to lower bits 1: from lower bits to upper bits
[25]	RW	cgms_seq	Sequence of transmitting the bits of the CGMS data. 0: from upper bits to lower bits 1: from lower bits to upper bits
[24]	RW	cc_seq	Sequence of transmitting the bits of the closed caption data. 0: from upper bits to lower bits 1: from lower bits to upper bits
[23]	RW	c_limit_en	Chrominance amplitude limit enable. 0: disabled 1: enabled
[22:13]	RW	amp_outside	Pulse amplitude input of the external AGC.
[12]	RW	date_test_en	Test valid signal. 0: invalid 1: valid
[11:10]	RW	date_test_mode	Test mode signal.
[9:0]	RW	dac_test	DAC test value input.

DATE1_COEFF7

DATE1_COEFF7 is a DATE1 teletext configuration register.

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Offset Address	Register Name	Total Reset Value
0xC41C	DATE1_COEFF7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt22_enf1	tt21_enf1	tt20_enf1	tt19_enf1	tt18_enf1	tt17_enf1	tt16_enf1	tt15_enf1	tt14_enf1	tt13_enf1	tt12_enf1	tt11_enf1	tt10_enf1	tt09_enf1	tt08_enf1	tt07_enf1	tt22_enf2	tt21_enf2	tt20_enf2	tt19_enf2	tt18_enf2	tt17_enf2	tt16_enf2	tt15_enf2	tt14_enf2	tt13_enf2	tt12_enf2	tt11_enf2	tt10_enf2	tt09_enf2	tt08_enf2	tt07_enf2
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	tt22_enf1	Control of teletext in line 22 in the odd field. 0: disabled 1: enabled
[30]	RW	tt21_enf1	Control of teletext in line 21 in the odd field. 0: disabled 1: enabled
[29]	RW	tt20_enf1	Control of teletext in line 20 in the odd field. 0: disabled 1: enabled
[28]	RW	tt19_enf1	Control of teletext in line 19 in the odd field. 0: disabled 1: enabled
[27]	RW	tt18_enf1	Control of teletext in line 18 in the odd field. 0: disabled 1: enabled
[26]	RW	tt17_enf1	Control of teletext in line 17 in the odd field. 0: disabled 1: enabled
[25]	RW	tt16_enf1	Control of teletext in line 16 in the odd field. 0: disabled 1: enabled
[24]	RW	tt15_enf1	Control of teletext in line 15 in the odd field. 0: disabled 1: enabled
[23]	RW	tt14_enf1	Control of teletext in line 14 in the odd field. 0: disabled 1: enabled

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[22]	RW	tt13_enf1	Control of teletext in line 13 in the odd field. 0: disabled 1: enabled
[21]	RW	tt12_enf1	Control of teletext in line 12 in the odd field. 0: disabled 1: enabled
[20]	RW	tt11_enf1	Control of teletext in line 11 in the odd field. 0: disabled 1: enabled
[19]	RW	tt10_enf1	Control of teletext in line 10 in the odd field. 0: disabled 1: enabled
[18]	RW	tt09_enf1	Control of teletext in line 9 in the odd field. 0: disabled 1: enabled
[17]	RW	tt08_enf1	Control of teletext in line 8 in the odd field. 0: disabled 1: enabled
[16]	RW	tt07_enf1	Control of teletext in line 7 in the odd field. 0: disabled 1: enabled
[15]	RW	tt22_enf2	Control of teletext in line 22 in the even field. 0: disabled 1: enabled
[14]	RW	tt21_enf2	Control of teletext in line 21 in the even field. 0: disabled 1: enabled
[13]	RW	tt20_enf2	Control of teletext in line 20 in the even field. 0: disabled 1: enabled
[12]	RW	tt19_enf2	Control of teletext in line 19 in the even field. 0: disabled 1: enabled
[11]	RW	tt18_enf2	Control of teletext in line 18 in the even field. 0: disabled 1: enabled

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[10]	RW	tt17_enf2	Control of teletext in line 17 in the even field. 0: disabled 1: enabled
[9]	RW	tt16_enf2	Control of teletext in line 16 in the even field. 0: disabled 1: enabled
[8]	RW	tt15_enf2	Control of teletext in line 15 in the even field. 0: disabled 1: enabled
[7]	RW	tt14_enf2	Control of teletext in line 14 in the even field. 0: disabled 1: enabled
[6]	RW	tt13_enf2	Control of teletext in line 13 in the even field. 0: disabled 1: enabled
[5]	RW	tt12_enf2	Control of teletext in line 12 in the even field. 0: disabled 1: enabled
[4]	RW	tt11_enf2	Control of teletext in line 11 in the even field. 0: disabled 1: enabled
[3]	RW	tt10_enf2	Control of teletext in line 10 in the even field. 0: disabled 1: enabled
[2]	RW	tt09_enf2	Control of teletext in line 9 in the even field. 0: disabled 1: enabled
[1]	RW	tt08_enf2	Control of teletext in line 8 in the even field. 0: disabled 1: enabled
[0]	RW	tt07_enf2	Control of teletext in line 7 in the even field. 0: disabled 1: enabled

DATE1_COEFF8

DATE1_COEFF8 is a DATE1 teletext configuration register.

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Offset Address	Register Name	Total Reset Value
0xC420	DATE1_COEFF8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt_staddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tt_staddr	Start address of the teletext data.

DATE1_COEFF9

DATE1_COEFF9 is a DATE1 teletext configuration register.

Offset Address	Register Name	Total Reset Value
0xC424	DATE1_COEFF9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt_edaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tt_edaddr	End address of the teletext data.

DATE1_COEFF10

DATE1_COEFF10 is a DATE1 teletext configuration register.

CAUTION

The teletext function is supported in both 625-line mode and 525-line mode. The tt_mode bit is set to 01 in 625-line mode or 10 in 525-line mode.

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Offset Address	Register Name	Total Reset Value
0xC428	DATE1_COEFF10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt_ready	reserved																		nabts_100ire	full_page	tt_highest	tt_mode		tt_pktoff							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	tt_ready	When software sets related parameters through the bus, this bit is set to 1 and the teletext module starts to work. When the teletext module completes data transfer, this bit is set to 0. The bit status can be queried through software for the next configuration.
[30:13]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[12]	RW	nabts_100ire	NABTS-NTSC data height. 0: 70 IRE 1: 100 IRE
[11]	RW	full_page	Teletext data transmission mode. 0: normal mode. The teletext data is transmitted from the blanking line. 1: full page mode. The teletext data can also be transmitted from the active video region.
[10]	RW	tt_highest	Teletext priority control. 0: The teletext data has the highest priority. 1: The teletext data has the lowest priority.
[9:8]	RW	tt_mode	Teletext mode. This field is set to 01 in 625-line mode, indicating WST-PAL. This field is set to 10 in 525-line mode, indicating NABTS-NTSC.
[7:0]	RW	tt_pktoff	Offset address of the teletext packet.

DATE1_COEFF11

DATE1_COEFF11 is a DATE1 closed caption configuration register.

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Offset Address	Register Name	Total Reset Value
0xC42C	DATE1_COEFF11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										cc_enf1	cc_enf2	date_clf1								date_clf2											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RW	reserved	Reserved.
[21]	RW	cc_enf1	Closed caption odd field enable. 0: disabled 1: enabled
[20]	RW	cc_enf2	Closed caption even field enable. 0: disabled 1: enabled
[19:10]	RW	date_clf1	Configuration line of the closed caption odd field.
[9:0]	RW	date_clf2	Configuration line of the closed caption even field.

DATE1_COEFF12

DATE1_COEFF12 is a DATE1 closed caption configuration register.

Offset Address	Register Name	Total Reset Value
0xC430	DATE1_COEFF12	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cc_f1data																cc_f2data															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cc_f1data	Data of the closed caption odd field.
[15:0]	RW	cc_f2data	Data of the closed caption even field.

DATE1_COEFF13

DATE1_COEFF13 is a DATE1 CGMS configuration register.

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Offset Address	Register Name	Total Reset Value
0xC434	DATE1_COEFF13	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										cg_enf1	cg_enf2	cg_f1data																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[21]	RW	cg_enf1	CGMS odd field enable. 0: disabled 1: enabled
[20]	RW	cg_enf2	CGMS even field enable. 0: disabled 1: enabled
[19:0]	RW	cg_f1data	Data of the CGMS odd field.

DATE1_COEFF14

DATE1_COEFF14 is a DATE1 CGMS configuration register.

Offset Address	Register Name	Total Reset Value
0xC438	DATE1_COEFF14	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cg_f2data																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[19:0]	RW	cg_f2data	Data of the CGMS even field.

DATE1_COEFF15

DATE1_COEFF15 is a DATE1 WSS configuration register.

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CAUTION

The WSS is available only in 625-line mode and is fixed at line 23.

Offset Address	Register Name	Total Reset Value
0xC43C	DATE1_COEFF15	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	wss_en	wss_data													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[14]	RW	wss_en	WSS enable. 0: disabled 1: enabled
[13:0]	RW	wss_data	WSS data.

DATE1_COEFF16

DATE1_COEFF16 is a DATE1 VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC440	DATE1_COEFF16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							vps_en	vps_data																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[24]	RW	vps_en	VPS enable. 0: disabled 1: enabled
[23:0]	RW	vps_data	VPS data from bit 23 to bit 0. Bit 0 is the LSB.

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DATE1_COEFF17

DATE1_COEFF17 is a DATE1 VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC444	DATE1_COEFF17	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vps_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	vps_data	VPS data from bit 55 to bit 24. Bit 0 is the LSB.

DATE1_COEFF18

DATE1_COEFF18 is a DATE1 VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC448	DATE1_COEFF18	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vps_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	vps_data	VPS data from bit 87 to bit 56. Bit 0 is the LSB.

DATE1_COEFF19

DATE1_COEFF19 is a DATE1 VPS configuration register.

CAUTION

The VPS is available only in 625-line mode and is fixed at line 16.

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Offset Address	Register Name	Total Reset Value
0xC44C	DATE1_COEFF19	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vps_data															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[15:0]	RW	vps_data	VPS data from bit 103 to bit 88. Bit 0 is the LSB.

DATE1_COEFF20

DATE1_COEFF20 is a DATE1 teletext configuration register.

Offset Address	Register Name	Total Reset Value
0xC450	DATE1_COEFF20	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													tt06_enf1	tt06_enf2	tt05_enf2
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[2]	RW	tt06_enf1	Control of teletext in line 6 in the odd field. 0: disabled 1: enabled
[1]	RW	tt06_enf2	Control of teletext in line 6 in the even field. 0: disabled 1: enabled
[0]	RW	tt05_enf2	Control of teletext in line 5 in the even field. 0: disabled 1: enabled

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DATE1_COEFF21

DATE1_COEFF21 is the DATE1 output matrix control register.

Offset Address	Register Name	Total Reset Value
0xC454	DATE1_COEFF21	0x0060_00A1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									dac5_in_sel			reserved	dac4_in_sel			reserved	dac3_in_sel			reserved	dac2_in_sel			reserved	dac1_in_sel			reserved	dac0_in_sel		
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1

Bits	Access	Name	Description
[31:23]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[22:20]	RW	dac5_in_sel	DAC5 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[19]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[18:16]	RW	dac4_in_sel	DAC4 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[15]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.

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[14:12]	RW	dac3_in_sel	DAC3 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[11]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[10:8]	RW	dac2_in_sel	DAC2 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[7]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[6:4]	RW	dac1_in_sel	DAC1 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[3]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.

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[2:0]	RW	dac0_in_sel	DAC0 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0

DATE1_COEFF22

DATE1_COEFF22 is the DATE1 DTO initial phase configuration register.

Offset Address	Register Name	Total Reset Value
0xC458	DATE1_COEFF22	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					video_phase_delta										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[10:0]	RW	video_phase_delta	DTO initial phase.

DATE1_COEFF23

DATE1_COEFF23 is the DATE1 video output delay configuration register.

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Offset Address	Register Name	Total Reset Value
0xC45C	DATE1_COEFF23	0x0065_4321

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									dac5_out_dly			reserved	dac4_out_dly			reserved	dac3_out_dly			reserved	dac2_out_dly			reserved	dac1_out_dly			reserved	dac0_out_dly		
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1

Bits	Access	Name	Description
[31:23]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[22:20]	RW	dac5_out_dly	DAC5 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.
[19]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[18:16]	RW	dac4_out_dly	DAC4 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.
[15]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[14:12]	RW	dac3_out_dly	DAC3 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.
[11]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[10:8]	RW	dac2_out_dly	DAC2 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.
[7]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[6:4]	RW	dac1_out_dly	DAC1 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.
[3]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.

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[2:0]	RW	dac0_out_dly	DAC0 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.

DATE1_ISRMASK

DATE1_ISRMASK is the DATE1 interrupt mask register.

Offset Address	Register Name	Total Reset Value
0xC480	DATE1_ISRMASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[0]	RW	tt_mask	Teletext interrupt mask. 0: enabled 1: masked

DATE1_ISRSTATE

DATE1_ISRSTATE is the DATE1 interrupt status register.

Offset Address	Register Name	Total Reset Value
0xC484	DATE1_ISRSTATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.

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[0]	W1C	tt_status	Teletext interrupt flag. After the DATE module reads all the teletext data, the bit is set to 1. Writing 1 to this bit clears this bit.

DATE1_ISR

DATE1_ISR is the DATE1 interrupt register.

Offset Address	Register Name	Total Reset Value
0xC488	DATE1_ISR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[0]	RW	tt_int	Teletext interrupt. It is the interrupt status after tt_status is masked by tt_mask. 0: No interrupt is generated. 1: An interrupt is generated.

DATE1_VERSION

DATE1_VERSION is the DATE1 version register.

Offset Address	Register Name	Total Reset Value
0xC490	DATE1_VERSION	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:0]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.

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VOCTRL

VO_CTRL is a VO control register.

Offset Address	Register Name	Total Reset Value
0xCE00	VOCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vo_ck_gt_en	reserved									bus_dbg_en		outstd_wid0				reserved			vo_id_sel	outstd_rid0				outstd_rid1				arb_mode			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	-	vo_ck_gt_en	Clock gating enable. 0: disabled 1: enabled
[30:22]	-	reserved	Reserved.
[21:20]	RW	bus_dbg_en	Bus debugging enable. 00: normal mode 01: read-write loopback mode for bus test 10: write loopback mode for bus test Other values: reserved
[19:16]	RW	outstd_wid0	Outstanding of ID0 of the AXI bus write channel.
[15:13]	-	reserved	Reserved.
[12]	RW	vo_id_sel	VDP VHD ID select. 0: real-time mode ID (0) 1: offline mode ID (1)
[11:8]	RW	outstd_rid0	Outstanding of ID0 of the AXI bus read channel.
[7:4]	RW	outstd_rid1	Outstanding of ID1 of the AXI bus read channel.
[3:0]	RW	arb_mode	Arbitration mode of requesting data for each internal surface bus of the VOU. 0000: The polling mode is used. 0001: The graphics layer takes priority. Other values: reserved

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VOINTSTA

VOINTSTA is a VO interrupt status register. It is a read-only register.

Offset Address	Register Name	Total Reset Value
0xCE04	VOINTSTA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	be_int	reserved												dsd5uf_int	dsd4uf_int	dsd3uf_int	dsd2uf_int	dsd1uf_int	dhd1uf_int	reserved	wbc2_te_int	dsdvtthd5_int	dsdvtthd4_int	dsdvtthd3_int	dhduf_int	reserved	dhdvtthd2_int	dhdvtthd1_int	dsduf_int	dsdvtthd2_int	dsdvtthd1_int	dsdvtthd0_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	be_int	Bus error interrupt (AXI_Master). 0: No interrupt is generated. 1: An interrupt is generated.
[30:19]	-	reserved	Reserved.
[18]	RW	dsd5uf_int	DSD5 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[17]	RW	dsd4uf_int	DSD4 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RW	dsd3uf_int	DSD3 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[15]	RW	dsd2uf_int	DSD2 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[14]	RW	dsd1uf_int	DSD1 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[13]	RW	dhd1uf_int	DHD1 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[12]	-	reserved	Reserved.

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[11]	RO	wbc2_te_int	WBC2 task completion interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[10]	-	dsdvtthd5_int	DSD5 vertical timing interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	dsdvtthd4_int	DSD4 vertical timing interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	dsdvtthd3_int	DSD3 vertical timing interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	dhduf_int	DHD low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[6]	-	reserved	Reserved.
[5]	RO	dhdvtthd2_int	DHD1 vertical timing interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	dhdvtthd1_int	DHD0 vertical timing interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	dsduf_int	DSD low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	dsdvtthd2_int	DSD2 vertical timing interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	dsdvtthd1_int	DSD1 vertical timing interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	dsdvtthd0_int	DSD0 vertical timing interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

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VOMSKINTSTA

VOMSKINTSTA is a VO masked interrupt status register. Writing 1 clears this register.

Offset Address	Register Name	Total Reset Value
0xCE08	VOMSKINTSTA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	be_int	reserved												dsd5uf_int	dsd4uf_int	dsd3uf_int	dsd2uf_int	dsd1uf_int	dhd1uf_int	reserved	wbc2_te_int	dsdvtthd5_int	dsdvtthd4_int	dsdvtthd3_int	dhduf_int	reserved	dhdvtthd2_int	dhdvtthd1_int	dsduf_int	dsdvtthd2_int	dsdvtthd1_int	dsdvtthd0_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWC	be_int	Bus error interrupt (AXI_Master). 0: No interrupt is generated. 1: An interrupt is generated.
[30:19]	-	reserved	Reserved.
[18]	RW	dsd5uf_int	DSD5 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[17]	RW	dsd4uf_int	DSD4 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RW	dsd3uf_int	DSD3 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[15]	RW	dsd2uf_int	DSD2 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[14]	RW	dsd1uf_int	DSD1 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[13]	RW	dhd1uf_int	DHD1 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[12]	-	reserved	Reserved.

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[11]	RO	wbc2_te_int	WBC2 task completion interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[10]	-	dsdvtthd5_int	DSD5 vertical timing interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	dsdvtthd4_int	DSD4 vertical timing interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	dsdvtthd3_int	DSD3 vertical timing interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	dhduf_int	DHD low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[6]	-	reserved	Reserved.
[5]	RO	dhdvtthd2_int	DHD1 vertical timing interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	dhdvtthd1_int	DHD0 vertical timing interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	dsduf_int	DSD low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	dsdvtthd2_int	DSD2 vertical timing interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	dsdvtthd1_int	DSD1 vertical timing interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	dsdvtthd0_int	DSD0 vertical timing interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

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VOINTMSK

VOINTMSK is a VDP interrupt mask register. It corresponds to VOINTSTA. When the corresponding bit is set to 1, the interrupt is enabled; when the corresponding bit is set to 0, the interrupt is masked.

Offset Address	Register Name	Total Reset Value
0xCE0C	VOINTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	be_intmsk	reserved												dsd5uf_intmsk	dsd4uf_intmsk	dsd3uf_intmsk	dsd2uf_intmsk	dsd1uf_intmsk	dhd1uf_intmsk	reserved	wbc2_te_intmsk	dsdvtthd5_intmsk	dsdvtthd4_intmsk	dsdvtthd3_intmsk	dhduf_intmsk	reserved	dhdvtthd2_intmsk	dhdvtthd1_intmsk	dsduf_intmsk	dsdvtthd2_intmsk	dsdvtthd1_intmsk	dsdvtthd0_intmsk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	R/W	be_intmsk	Bus error interrupt (AXI_Master). 0: No interrupt is generated. 1: An interrupt is generated.
[30:19]	-	reserved	Reserved.
[18]	RW	dsd5uf_intmsk	DSD5 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[17]	RW	dsd4uf_intmsk	DSD4 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RW	dsd3uf_intmsk	DSD3 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[15]	RW	dsd2uf_intmsk	DSD2 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[14]	RW	dsd1uf_intmsk	DSD1 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[13]	RW	dhd1uf_intmsk	DHD1 low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

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[12]	-	reserved	Reserved.
[11]	RO	wbc2_te_intmsk	WBC2 task completion interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[10]	R/W	dsdvtthd5_intmsk	DSD5 vertical timing interrupt 3. 0: No interrupt is generated. 1: An interrupt is generated.
[9]	R/W	dsdvtthd4_intmsk	DSD4 vertical timing interrupt 2. 0: No interrupt is generated. 1: An interrupt is generated.
[8]	R/W	dsdvtthd3_intmsk	DSD3 vertical timing interrupt 1. 0: No interrupt is generated. 1: An interrupt is generated.
[7]	R/W	dhduf_intmsk	DHD low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[6]	-	reserved	Reserved.
[5]	R/W	dhdvtthd2_intmsk	DHD vertical timing interrupt 2. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	R/W	dhdvtthd1_intmsk	DHD vertical timing interrupt 1. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	R/W	dsduf_intmsk	DSD low-bandwidth alarm interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	R/W	dsdvtthd2_intmsk	DSD2 vertical timing interrupt 3. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	R/W	dsdvtthd1_intmsk	DSD1 vertical timing interrupt 2. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	R/W	dsdvtthd0_intmsk	DSD0 vertical timing interrupt 1. 0: No interrupt is generated. 1: An interrupt is generated.

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VOUVERSION1

VOUVERSION1 is VDP version register 1.

Offset Address	Register Name	Total Reset Value
0xCE10	VOUVERSION1	0x7675_6F76

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vouversion0																															
Reset	0	1	1	1	0	1	1	0	0	1	1	1	0	1	0	1	0	1	1	0	1	1	1	1	0	1	1	1	0	1	1	0

Bits	Access	Name	Description
[31:0]	RO	vouversion0	VDP version.

VOUVERSION2

VOUVERSION2 is VDP version register 2.

Offset Address	Register Name	Total Reset Value
0xCE14	VOUVERSION2	0x3030_3134

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vouversion1																															
Reset	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:0]	RO	vouversion1	VDP version.

VOMUXDATA

VOMUXDATA is a VO interface multiplexing data register (VOPINTEST).

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Offset Address	Register Name	Total Reset Value
0xCE18	VOMUXDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pin_test_en	pin_test_mode				vsync_value	hsync_value	dv_value	pin_test_data																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	pin_test_en	Pin test mode enable. 0: disabled 1: enabled The values of Vo_pdata, Vo_vsync, Vo_hsync, and Vo_dv are defined by bit[23:0], bit[26], bit[25], and bit[24] of VOMUXDATA respectively.
[30:27]	RW	pin_test_mode	Reserved.
[26]	RW	vsync_value	Configured vertical timing in test mode.
[25]	RW	hsync_value	Configured horizontal timing in test mode.
[24]	RW	dv_value	Configured data valid timing in test mode.
[23:0]	RW	pin_test_data	Test data in test mode. All DACs use bit[9:0]. When the component width is greater than 8 bits, the MSB is the stuffed bit, for example, 36-bit output[35:24] = {[23:16], [23:20]}.

VOMUX

VOMUX is a VO interface multiplexing register.

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Offset Address	Register Name	Total Reset Value
0xCE1C	VOMUX	0x0004_001B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								bt1120_sel_yc	hdmi_vid							reserved											hddate_in_sel_hd0	vga_in_sel_hd0	dac1_sel		bt1120_sel_hd0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23]	RW	bt1120_sel_yc	BT.1120 Y/C position select. 0: The upper eight bits are used to transmit the Y component, and the lower eight bits are used to transmit the C component. 1: The upper eight bits are used to transmit the C component, and the lower eight bits are used to transmit the Y component.
[22:16]	RW	hdmi_vid	The reverse requirements on the HDMI input interface timing can be met only when the reverse enable register is ORed with the INIF timing reverse register. bit[22]: VSYNC signal reverse enable. 0: disabled 1: enabled bit[21]: HSYNC signal reverse enable. 0: disabled 1: enabled bit[20]: data valid sync signal reverse enable. 0: disabled 1: enabled bit[19]: reserved bit[18:17]: HDMI video output format select. The default value is 00. The RGB or YCbCr format is selected by configuring the DHD. 00: YCbCr444, 30-bit sync separation mode 01: RGB444, 30-bit sync separation mode 10: YCbCr422, 20-bit sync separation mode 11: YCbCr422, 10-bit sync separation mode bit[16]: HDMI data source. 0: DHD1 output 1: DHD0 output

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[15:5]	-	reserved	Reserved.
[4]	RW	hddate_in_sel_hd0	HDDATE output select. 0: DHD1 video 1: DHD0 video
[3]	RW	vga_in_sel_hd0	VGA output select. 0: DHD1 video 1: DHD0 video
[2:1]	RW	dac1_sel	DAC1 output select. The default value is 01. 00: HD analog video (HDDATE) 01: digital analog video (VGA) 10 and 11: reserved
[0]	RW	bt1120_sel_hd0	BT.1120 output select. 0: DHD1 output 1: DHD0 output

VGACSCIDC

VGACSCIDC is a VGA input DC component register for CSC (instant register).

Offset Address	Register Name	Total Reset Value
0xCE24	VGACSCIDC	0x0000_0000

Bit	31 30 29 28	27	26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	csc_en	cscidc2		cscidc1		cscidc0		
Reset	0 0 0 0	0	0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27]	RW	csc_en	CSC enable. 0: disabled 1: enabled
[26:18]	RW	cscidc2	DC parameter of input component 2. The MSB is the signed bit. The value is expressed as the complement.
[17:9]	RW	cscidc1	DC parameter of input component 1. The MSB is the signed bit. The value is expressed as the complement.
[8:0]	RW	cscidc0	DC parameter of input component 0. The MSB is the signed bit. The value is expressed as the complement.

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VGACSCODC

VGACSCODC is a VGA output DC component register for CSC (instant register).

Offset Address	Register Name	Total Reset Value
0xCE28	VGACSCODC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscodc2												cscodc1								cscodc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved.
[26:18]	RW	cscodc2	DC parameter of output component 2. The MSB is the signed bit. The value is expressed as the complement.
[17:9]	RW	cscodc1	DC parameter of output component 1. The MSB is the signed bit. The value is expressed as the complement.
[8:0]	RW	cscodc0	DC parameter of output component 0. The MSB is the signed bit. The value is expressed as the complement.

VGACSCP0

VGACSCP0 is the VGA CSC parameter 0 register (instant register).

Offset Address	Register Name	Total Reset Value
0xCE2C	VGACSCP0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp01												reserved				cscp00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp01	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp00	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

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VGACSCP1

VGACSCP1 is the VGA CSC parameter 1 register (instant register).

Offset Address	Register Name	Total Reset Value
0xCE30	VGACSCP1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp10												reserved				cscp02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp10	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp02	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

VGACSCP2

VGACSCP2 is the VGA CSC parameter 2 register (instant register).

Offset Address	Register Name	Total Reset Value
0xCE34	VGACSCP2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp12												reserved				cscp11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp12	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

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[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp11	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

VGACSCP3

VGACSCP3 is the VGA CSC parameter 3 register (instant register).

Offset Address	Register Name	Total Reset Value
0xCE38	VGACSCP3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp21												reserved				cscp20											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp21	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp20	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

VGACSCP4

VGACSCP4 is the VGA CSC parameter 4 register (instant register).

Offset Address	Register Name	Total Reset Value
0xCE3C	VGACSCP4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cscp22											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved.

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[12:0]	RW	cscp22	5.8 data format that consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complement.

VOPARAUP

VOPARAUP is a scaling/gamma/ACC coefficient update enable register. Software needs to configure the coefficients and enable coefficient update. The VDP reads coefficients from the DDR through the AXI master and stores the coefficients in the VOU.

Offset Address	Register Name	Total Reset Value
0xCE40	VOPARAUP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dhd1_gamma_upd	g1_vcoef_upd	g1_hcoef_upd	g0_vcoef_upd	g0_hcoef_upd	g1_lut_upd	g0_lut_upd	wbc2_vcoef_upd	wbc2_hcoef_upd	dhd_gamma_upd	video_acc_upd	vhd1_vcoef_upd	vhd1_hcoef_upd	vhd_vcoef_upd	vhd_hcoef_upd
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved.
[14]	RW	dhd1_gamma_upd	Indicates whether the DHD1 gamma correction operation lookup table needs to be updated. This bit is cleared automatically after the hardware updates the table. 0: not updated 1: updated
[13]	RW	g1_vcoef_upd	Indicates whether the G1 VFIR coefficient needs to be updated. This bit is cleared automatically after the hardware updates the coefficient. 0: not updated 1: updated
[12]	RW	g1_hcoef_upd	Indicates whether the G1 HFIR coefficient needs to be updated. This bit is cleared automatically after the hardware updates the coefficient. 0: not updated 1: updated

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[11]	RW	g0_vcoef_upd	Indicates whether the G0 VFIR coefficient needs to be updated. This bit is cleared automatically after the hardware updates the coefficient. 0: not updated 1: updated
[10]	RW	g0_hcoef_upd	Indicates whether the G0 HFIR coefficient needs to be updated. This bit is cleared automatically after the hardware updates the coefficient. 0: not updated 1: updated
[9]	RW	g1_lut_upd	Indicates whether G1 LUT needs to be updated. This bit is cleared automatically after the hardware updates G1 LUT. 0: not updated 1: updated
[8]	RW	g0_lut_upd	Indicates whether G0 LUT needs to be updated. This bit is cleared automatically after the hardware updates G0 LUT. 0: not updated 1: updated
[7]	RW	wbc2_vcoef_upd	Indicates whether the WBC2 vertical luminance and chrominance filtering coefficients need to be updated. This bit is cleared automatically after the hardware updates coefficients. 0: not updated 1: updated
[6]	RW	wbc2_hcoef_upd	Indicates whether the WBC2 horizontal luminance and chrominance filtering coefficients need to be updated. This bit is cleared automatically after the hardware updates coefficients. 0: not updated 1: updated
[5]	RW	dhd_gamma_upd	Indicates whether the DHD gamma correction operation lookup table needs to be updated. This bit is cleared automatically after the hardware updates the table. 0: not updated 1: updated
[4]	RW	video_acc_upd	Indicates whether the ACC operation lookup table of the video layer needs to be updated. This bit is cleared automatically after the hardware updates the table. 0: not updated 1: updated
[3]	RW	vhd1_vcoef_upd	Indicates whether the VHD1 vertical luminance and chrominance filtering coefficients need to be updated. This bit is cleared automatically after the hardware updates the coefficients. 0: not updated 1: updated

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[2]	RW	vhd1_hcoef_upd	Indicates whether the VHD1 horizontal luminance and chrominance filtering coefficients need to be updated. This bit is cleared automatically after the hardware updates the coefficients. 0: not updated 1: updated
[1]	RW	vhd_vcoef_upd	Indicates whether the VHD vertical luminance and chrominance filtering coefficients need to be updated. This bit is cleared automatically after the hardware updates the coefficients. 0: not updated 1: updated
[0]	RW	vhd_hcoef_upd	Indicates whether the VHD horizontal luminance and chrominance filtering coefficients need to be updated. This bit is cleared automatically after the hardware updates the coefficients. 0: not updated 1: updated

VHDHCOEFAD

VHDHCOEFAD is a VHD horizontal luminance and chrominance filtering coefficient address register.

Offset Address	Register Name	Total Reset Value
0xCE44	VHDHCOEFAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef_addr	Start address of the local memory for storing coefficients.

VHDVCOEFAD

VHDVCOEFAD is a VHD vertical luminance and horizontal chrominance filtering coefficient address register.

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Offset Address	Register Name	Total Reset Value
0xCE48	VHDVCOEFAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef_addr	Start address of the local memory for storing coefficients.

ACCAD

ACCAD is an ACC coefficient lookup table address register of the video channel.

Offset Address	Register Name	Total Reset Value
0xCE54	ACCAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef_addr	Start address of the local memory for storing coefficients.

WBC2HCOEFAD

WBC2HCOEFAD is a WBC2 horizontal luminance and chrominance filtering coefficient address register.

Offset Address	Register Name	Total Reset Value
0xCE58	WBC2HCOEFAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef_addr	Start address of the local memory for storing coefficients.

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WBC2VCOEFAD

WBC2VCOEFAD is a WBC2 vertical luminance and horizontal chrominance filtering coefficient address register.

Offset Address	Register Name	Total Reset Value
0xCE5C	WBC2VCOEFAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef_addr	Start address of the local memory for storing coefficients.

DHDGAMMAAD

DHDGAMMAAD is a DHD gamma correction coefficient address register.

Offset Address	Register Name	Total Reset Value
0xCE78	DHDGAMMAAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef_addr	Start address of the local memory for storing coefficients.

DACCTRL0_2

DACCTRL0_2 is the DAC0–2 control register.

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Offset Address	Register Name	Total Reset Value
0xCEE0	DACCTRL0_2	0x0703_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			enextref	envbg	endac2	endac1	endac0	enctr2	enctr1	enctr0	ensc2	ensc1	ensc0	dac2gc						dac1gc								dac0gc			
Reset	0	0	0	0	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28]	RW	enextref	DAC0–2 extref enable. 0: disabled 1: enabled
[27]	RW	envbg	DAC0–2 VBG enable. 0: disabled 1: enabled
[26]	RW	endac2	DAC2 power-down enable. 0: disabled 1: enabled
[25]	RW	endac1	DAC1 power-down enable. 0: disabled 1: enabled
[24]	RW	endac0	DAC0 power-down enable. 0: disabled 1: enabled
[23]	RW	enctr2	DAC2 analog bias test control.
[22]	RW	enctr1	DAC1 analog bias test control.
[21]	RW	enctr0	DAC0 analog bias test control.
[20]	RW	ensc2	DAC2 connection detection enable. During connection detection, the digital signals transmitted to the DAC are configured by using the VOMUX register. 0: disabled 1: enabled
[19]	RW	ensc1	DAC1 connection detection enable. During connection detection, the digital signals transmitted to the DAC are configured by using the VOMUX register. 0: disabled 1: enabled

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[18]	RW	ensc0	DAC0 connection detection enable. During connection detection, the digital signals transmitted to the DAC are configured by using the VOMUX register. 0: disabled 1: enabled
[17:12]	RW	dac2gc	Gain control of the DAC2 output full-scale current.
[11:6]	RW	dac1gc	Gain control of the DAC1 output full-scale current.
[5:0]	RW	dac0gc	Gain control of the DAC0 output full-scale current.

DACCTRL3_5

DACCTRL3_5 is the DAC3-5 control register.

Offset Address	Register Name	Total Reset Value
0xCEE4	DACCTRL3_5	0x0703_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			enextref	envbg	endac5	endac4	endac3	enctr5	enctr4	enctr3	ensc5	ensc4	ensc3	dac5gc						dac4gc								dac3gc			
Reset	0	0	0	0	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28]	RW	enextref	DAC3–5 extref enable. 0: disabled 1: enabled
[27]	RW	envbg	DAC3–5 VBG enable. 0: disabled 1: enabled
[26]	RW	endac5	DAC5 power-down enable. 0: disabled 1: enabled
[25]	RW	endac4	DAC4 power-down enable. 0: disabled 1: enabled
[24]	RW	endac3	DAC3 power-down enable. 0: disabled 1: enabled

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[23]	RW	enctr5	DAC5 analog bias test control.
[22]	RW	enctr4	DAC4 analog bias test control.
[21]	RW	enctr3	DAC3 analog bias test control.
[20]	RW	ensc5	DAC5 connection detection enable. During connection detection, the digital signals transmitted to the DAC are configured by using the VOMUX register. 0: disabled 1: enabled
[19]	RW	ensc4	DAC4 connection detection enable. During connection detection, the digital signals transmitted to the DAC are configured by using the VOMUX register. 0: disabled 1: enabled
[18]	RW	ensc3	DAC3 connection detection enable. During connection detection, the digital signals transmitted to the DAC are configured by using the VOMUX register. 0: disabled 1: enabled
[17:12]	RW	dac5gc	Gain control of the DAC5 output full-scale current.
[11:6]	RW	dac4gc	Gain control of the DAC4 output full-scale current.
[5:0]	RW	dac3gc	Gain control of the DAC3 output full-scale current.

DACSTAT0_2

DACSTAT0_2 is the DAC0–2 status register.

Offset Address	Register Name	Total Reset Value
0xCEE8	DACSTAT0_2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													cableout2	cableout1	cableout0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RO	cableout2	DAC2 connection detection status.
[1]	RO	cableout1	DAC1 connection detection status.

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[0]	RO	cableout0	DAC0 connection detection status.

DACSTAT3_5

DACSTAT3_5 is the DAC3-5 status register.

Offset Address	Register Name	Total Reset Value
0xCEEC	DACSTAT3_5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													cableout5	cableout4	cableout3
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RO	cableout5	DAC5 connection detection status.
[1]	RO	cableout4	DAC4 connection detection status.
[0]	RO	cableout3	DAC3 connection detection status.

DACBANDGAP

DACBANDGAP is a band gap test register.

Offset Address	Register Name	Total Reset Value
0xCEF0	DACBANDGAP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								bandgap_bgtrim				bandgap_en	bandgap_test		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.

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[7:5]	RW	bandgap_bgtrim	Band gap test.
[4]	RW	bandgap_en	Band gap test.
[3:0]	RW	bandgap_test	Band gap test.

VOLPTIMER

VOLPTIMER is a low-power timer register.

Offset Address	Register Name	Total Reset Value
0xCEF4	VOLPTIMER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								timer							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	RW	timer	Low-power status timer (instant field). bit[7:0]: standby status timer bit[3:0]: retention status timer

VOLPMODE0

VOLPMODE0 is low-power mode register 0.

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Offset Address	Register Name	Total Reset Value
0xCEF8	VOLPMODE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dsd5_lp_mode		dsd4_lp_mode		dsd3_lp_mode		dsd2_lp_mode		dsd1_lp_mode		dsd0_lp_mode		dhd1_lp_mode		dhd0_lp_mode		vsd4_lp_mode		vsd3_lp_mode		vsd2_lp_mode		vsd1_lp_mode		vsd0_lp_mode		vhd2_lp_mode		vhd1_lp_mode		vhd0_lp_mode	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	dsd5_lp_mode	DSD5 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[29:28]	RW	dsd4_lp_mode	DSD4 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[27:26]	RW	dsd3_lp_mode	DSD3 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[25:24]	RW	dsd2_lp_mode	DSD2 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[23:22]	RW	dsd1_lp_mode	DSD1 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[21:20]	RW	dsd0_lp_mode	DSD0 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode

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[19:18]	RW	dhd1_lp_mode	DHD1 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[17:16]	RW	dhd0_lp_mode	DHD0 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[15:14]	RW	vsd4_lp_mode	VSD4 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[13:12]	RW	vsd3_lp_mode	VSD3 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[11:10]	RW	vsd2_lp_mode	VSD2 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[9:8]	RW	vsd1_lp_mode	VSD1 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[7:6]	RW	vsd0_lp_mode	VSD0 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[5:4]	RW	vhd2_lp_mode	VHD2 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[3:2]	RW	vhd1_lp_mode	VHD1 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode

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[1:0]	RW	vhd0_lp_mode	VHD0 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode

VOLPMODE1

VOLPMODE1 is low-power mode register 1.

Offset Address	Register Name	Total Reset Value
0xCEFC	VOLPMODE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														wbc2_lp_mode		para_lp_mode		hc1_lp_mode		hc0_lp_mode		g4_lp_mode		g3_lp_mode		g2_lp_mode		g1_lp_mode		g0_lp_mode	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RW	reserved	Reserved.
[17:16]	RW	wbc2_lp_mode	WBC2 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[15:14]	RW	para_lp_mode	PARA low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[13:12]	RW	hc1_lp_mode	HC1 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[11:10]	RW	hc0_lp_mode	HC0 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode

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[9:8]	RW	g4_lp_mode	G4 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[7:6]	RW	g3_lp_mode	G3 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[5:4]	RW	g2_lp_mode	G2 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[3:2]	RW	g1_lp_mode	G1 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode
[1:0]	RW	g0_lp_mode	G0 low-power mode select (instant field). 00: normal mode 10: retention mode 01 and 11: power-down mode

VHDHLCOEF

VHDHLCOEF is a VHD horizontal luminance scaling/filtering coefficient register.

Each filtering coefficient is 10 bits consisting of one signed bit and nine fractional bits. The MSB is the signed bit and the lower nine bits are the absolute values of the fractional bits. As the coefficients are stored in the on-chip memory, the default value is variable.

The VHD horizontal luminance scaling coefficients have eight taps and 32 phases. As the coefficients are symmetrical, there are 17 groups of coefficients. That is, 8-tap coefficients of phases 0–16 are stored. Each register address has two 10-bit coefficients. Therefore, four 32-bit register addresses are required for storing the 8-tap coefficients of each phase.

Offset Address	Register Name	Total Reset Value
0xD000–0xD10C	VHDHLCOEF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								hlcoefn2								reserved								hlcoefn1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.

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[25:16]	RW	hlcoefn2	Horizontal luminance scaling/filtering coefficient. Indicates the tap-2 coefficients when bits[3:0] of the register address are 0x0. Indicates the tap-4 coefficients when bits[3:0] of the register address are 0x4. Indicates the tap-6 coefficients when bits[3:0] of the register address are 0x8. Indicates the tap-8 coefficients when bits[3:0] of the register address are 0xC.
[15:10]	-	reserved	Reserved.
[9:0]	RW	hlcoefn1	Horizontal luminance scaling/filtering coefficient. Indicates the tap-1 coefficients when bits[3:0] of the register address are 0x0. Indicate the tap-3 coefficients when bits[3:0] of the register address are 0x4. Indicates the tap-5 coefficients when bits[3:0] of the register address are 0x8. Indicates the tap-7 coefficients when bits[3:0] of the register address are 0xC.

VHDHCCOEF

VHDHCCOEF is a VHD horizontal chrominance scaling/filtering coefficient register.

For details about the storage format, see the description of the VHDHLCOEF register. The VHD horizontal luminance scaling coefficients have four taps and 32 phases. As the coefficients are symmetrical, there are 17 groups of coefficients. That is, 4-tap coefficients of phases 0–16 are stored. Each register address has two 10-bit coefficients. Therefore, two 32-bit register addresses are required for storing the 4-tap coefficients of each phase.

Offset Address	Register Name	Total Reset Value
0xD200–0xD284	VHDHCCOEF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								hccoefn2								reserved								hccoefn1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	hccoefn2	Horizontal chrominance scaling/filtering coefficient. Indicates the tap-2 coefficients when bits[3:0] of the register address are 0x0 or 0x8. Indicates the tap-4 coefficients when bits[3:0] of the register address are 0x4 or 0xC.

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[15:10]	-	reserved	Reserved.
[9:0]	RW	hccoefn1	Horizontal chrominance scaling/filtering coefficient. Indicates the tap-1 coefficients when bits[3:0] of the register address are 0x0 or 0x8. Indicates the tap-3 coefficients when bits[3:0] of the register address are 0x4 or 0xC.

VHDVLCOEF

VHDVLCOEF is a VHD vertical luminance scaling/filtering coefficient register.

For details about the storage format, see the description of the VHDHLCOEF register. The VHD vertical luminance scaling coefficients have six taps and 32 phases. As the coefficients are symmetrical, there are 17 groups of coefficients. That is, 4-tap coefficients of phases 0–16 are stored. Each register address has two 10-bit coefficients. Therefore, four 32-bit register addresses are required for storing the 6-tap coefficients of each phase.

Offset Address	Register Name	Total Reset Value
0xD400–0xD50C	VHDVLCOEF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								vlcoefn2								reserved								vlcoefn1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	vlcoefn2	Vertical luminance scaling/filtering coefficient. Indicates the tap-2 coefficients when bit[3:0] of the register address are 0x0. Indicate the tap-4 coefficients when bits[3:0] of the register address are 0x4. Indicates the tap-6 coefficients when bits[3:0] of the register address are 0x8. Indicates a reserved field when bits[3:0] of the register address is 0xC.
[15:10]	-	reserved	Reserved.

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[9:0]	RW	vlcoefn1	Vertical luminance scaling/filtering coefficient. Indicates the tap-1 coefficients when bits[3:0] of the register address are 0x0. Indicate the tap-3 coefficients when bits[3:0] of the register address are 0x4. Indicates the tap-5 coefficients when bits[3:0] of the register address are 0x8. Indicates a reserved field when bits[3:0] of the register address is 0xC.

VHDVCCOEF

VHDVCCOEF is a VHD vertical chrominance scaling/filtering coefficient register.

For details about the storage format, see the description of the VHDHLCOEF register. The VHD horizontal chrominance scaling coefficients have four taps and 32 phases. As the coefficients are symmetrical, there are 17 groups of coefficients. That is, 4-tap coefficients of phases 0–16 are stored. Each register address has two 10-bit coefficients. Therefore, two 32-bit register addresses are required for storing the 4-tap coefficients of each phase.

Offset Address	Register Name	Total Reset Value
0xD600–0xD684	VHDVCCOEF	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	vccoefn2			reserved		vccoefn1	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	vccoefn2	Vertical luminance scaling/filtering coefficient. Indicates the tap-2 coefficients when bits[3:0] of the register address are 0x0 or 0x8. Indicates the tap-4 coefficients when bits[3:0] of the register address are 0x4 or 0xC.
[15:10]	-	reserved	Reserved.
[9:0]	RW	vccoefn1	Vertical luminance scaling/filtering coefficient. Indicates the tap-1 coefficients when bits[3:0] of the register address are 0x0 or 0x8. Indicates the tap-3 coefficients when bits[3:0] of the register address are 0x4 or 0xC.

WBCHLCOEF

WBCHLCOEF is a WBC horizontal luminance scaling/filtering coefficient register.

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Each filtering coefficient is 10 bits consisting of one signed bit and nine fractional bits. The MSB is the signed bit and the lower nine bits are the absolute values of the fractional bits. As the coefficients are stored in the on-chip memory, the default value is variable.

The WBC horizontal luminance scaling coefficients have eight taps and 32 phases. As the coefficients are symmetrical, there are 17 groups of coefficients. That is, 8-tap coefficients of phases 0–16 are stored. Each register address has two 10-bit coefficients. Therefore, four 32-bit register addresses are required for storing the 8-tap coefficients of each phase.

Offset Address	Register Name	Total Reset Value
0xE000–0xE10C	WBCHLCOEF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								hlcoefn2								reserved								hlcoefn1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	hlcoefn2	Horizontal luminance scaling/filtering coefficient. Indicates the tap-2 coefficients when bit[3:0] of the register address are 0x0. Indicate the tap-4 coefficients when bits[3:0] of the register address are 0x4. Indicates the tap-6 coefficients when bits[3:0] of the register address are 0x8. Indicates the tap-8 coefficients when bits[3:0] of the register address are 0xC.
[15:10]	-	reserved	Reserved.
[9:0]	RW	hlcoefn1	Horizontal luminance scaling/filtering coefficient. Indicates the tap-1 coefficients when bits[3:0] of the register address are 0x0. Indicate the tap-3 coefficients when bits[3:0] of the register address are 0x4. Indicates the tap-5 coefficients when bits[3:0] of the register address are 0x8. Indicates the tap-7 coefficients when bits[3:0] of the register address are 0xC.

WBCHCCOEF

WBCHCCOEF is a WBC horizontal chrominance scaling/filtering coefficient register.

For details about the storage format, see the description of the WBCHLCOEF register. The VHD horizontal luminance scaling coefficients have four taps and 32 phases. As the coefficients are symmetrical, there are 17 groups of coefficients. That is, 4-tap coefficients of phases 0–16 are stored. Each register address has two 10-bit coefficients. Therefore, two 32-bit register addresses are required for storing the 4-tap coefficients of each phase.

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Offset Address	Register Name	Total Reset Value
0xE200–0xE284	WBCHCCOEF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								hccoefn2								reserved								hccoefn1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	hccoefn2	Horizontal chrominance scaling/filtering coefficient. Indicates the tap-2 coefficients when bits[3:0] of the register address are 0x0 or 0x8. Indicates the tap-4 coefficients when bits[3:0] of the register address are 0x4 or 0xC.
[15:10]	-	reserved	Reserved.
[9:0]	RW	hccoefn1	Horizontal chrominance scaling/filtering coefficient. Indicates the tap-1 coefficients when bits[3:0] of the register address are 0x0 or 0x8. Indicates the tap-3 coefficients when bits[3:0] of the register address are 0x4 or 0xC.

WBCVLCOEF

WBCVLCOEF is a WBC vertical luminance scaling/filtering coefficient register.

For details about the storage format, see the description of the WBCHLCOEF register. The VHD vertical luminance scaling coefficients have six taps and 32 phases. As the coefficients are symmetrical, there are 17 groups of coefficients. That is, 4-tap coefficients of phases 0–16 are stored. Each register address has two 10-bit coefficients. Therefore, four 32-bit register addresses are required for storing the 6-tap coefficients of each phase.

Offset Address	Register Name	Total Reset Value
0xE400–0xE50C	WBCVLCOEF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								vlcoefn2								reserved								vlcoefn1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.

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[25:16]	RW	vlcoefn2	Vertical luminance scaling/filtering coefficient. Indicates the tap-2 coefficients when bit[3:0] of the register address are 0x0. Indicate the tap-4 coefficients when bits[3:0] of the register address are 0x4. Indicates the tap-6 coefficients when bits[3:0] of the register address are 0x8. Indicates a reserved field when bits[3:0] of the register address is 0xC.
[15:10]	-	reserved	Reserved.
[9:0]	RW	vlcoefn1	Vertical luminance scaling/filtering coefficient. Indicates the tap-1 coefficients when bits[3:0] of the register address are 0x0. Indicate the tap-3 coefficients when bits[3:0] of the register address are 0x4. Indicates the tap-5 coefficients when bits[3:0] of the register address are 0x8. Indicates a reserved field when bits[3:0] of the register address is 0xC.

WBCVCCOEF

WBCVCCOEF is a WBC vertical chrominance scaling/filtering coefficient register.

For details about the storage format, see the description of the WBCHLCOEF register. The VHD horizontal chrominance scaling coefficients have four taps and 32 phases. As the coefficients are symmetrical, there are 17 groups of coefficients. That is, 4-tap coefficients of phases 0–16 are stored. Each register address has two 10-bit coefficients. Therefore, two 32-bit register addresses are required for storing the 4-tap coefficients of each phase.

Offset Address	Register Name	Total Reset Value
0xE600–0xE684	WBCVCCOEF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								vccoefn2								reserved								vccoefn1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	vccoefn2	Vertical luminance scaling/filtering coefficient. Indicates the tap-2 coefficients when bits[3:0] of the register address are 0x0 or 0x8. Indicates the tap-4 coefficients when bits[3:0] of the register address are 0x4 or 0xC.

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[15:10]	-	reserved	Reserved.
[9:0]	RW	vccoefn1	Vertical luminance scaling/filtering coefficient. Indicates the tap-1 coefficients when bits[3:0] of the register address are 0x0 or 0x8. Indicates the tap-3 coefficients when bits[3:0] of the register address are 0x4 or 0xC.

DHDGAMMAN

DHDGAMMAN is a DHD gamma lookup table coefficient register.

As the coefficients are stored in the on-chip memory, the default value is variable.

Offset Address	Register Name	Total Reset Value
0xE800–0xE880	DHDGAMMAN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		gamma_datarn										gamma_datagn								gamma_databn											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	reserved	Reserved.
[29:20]	RW	gamma_datarn	Segment n (n = 0–32) of the R component in the gamma table.
[19:10]	RW	gamma_datagn	Segment n (n = 0–32) of the G component in the gamma table.
[9:0]	RW	gamma_databn	Segment n (n = 0–32) of the B component in the gamma table.

VHDHLTICOEF

VHDHLTICOEF is a VHD HLTI filtering coefficient register.

Each filtering coefficient is 10 bits consisting of one signed bit and nine fractional bits. The MSB is the signed bit and the lower nine bits are the absolute values of the fractional bits. As the coefficients are stored in the on-chip memory, the default value is not defined.

The VHD HLTI coefficients have 2 taps and 32 phases. As the coefficients are symmetrical, there are 17 groups of coefficients. That is, 2-tap coefficients of phases 0–16 are stored. Each register address stores two 10-bit coefficients.

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Offset Address	Register Name	Total Reset Value
0xF000–0xF040	VHDHLTICOEF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												hlticoefn2										hlticoefn1									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:10]	RW	hlticoefn2	HLTI filtering coefficient 2.
[9:0]	RW	hlticoefn1	HLTI filtering coefficient 1.

VHDHCTICOEF

VHDHCTICOEF is a VHD HCTI filtering coefficient register.

Each filtering coefficient is 10 bits consisting of one signed bit and nine fractional bits. The MSB is the signed bit and the lower nine bits are the absolute values of the fractional bits. As the coefficients are stored in the on-chip memory, the default value is not defined.

The VHD HCTI coefficients have 2 taps and 32 phases. As the coefficients are symmetrical, there are 17 groups of coefficients. That is, 2-tap coefficients of phases 0–16 are stored. Each register address stores two 10-bit coefficients.

Offset Address	Register Name	Total Reset Value
0xF100–0xF140	VHDHCTICOEF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												hcticoefn2										hcticoefn1									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:10]	RW	hcticoefn2	HCTI filtering coefficient 2.
[9:0]	RW	hcticoefn1	HCTI filtering coefficient 1.

VHDVLTICOEF

VHDVLTICOEF is a VLTI filtering coefficient register.

Each filtering coefficient is 10 bits consisting of one signed bit and nine fractional bits. The MSB is the signed bit and the lower nine bits are the absolute values of the fractional bits. As the coefficients are stored in the on-chip memory, the default value is not defined.

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The VHD VLTI coefficients have 2 taps and 32 phases. As the coefficients are symmetrical, there are 17 groups of coefficients. That is, 2-tap coefficients of phases 0–16 are stored. Each register address stores two 10-bit coefficients.

Offset Address	Register Name	Total Reset Value
0xF200–0xF240	VHDVLTICOEF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												vlticoefn2												vlticoefn1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:10]	RW	vlticoefn2	VLTI filtering coefficient 2.
[9:0]	RW	vlticoefn1	VLTI filtering coefficient 1.

VHDVCTICOEF

VHDVCTICOEF is a VHD VCTI filtering coefficient register.

Each filtering coefficient is 10 bits consisting of one signed bit and nine fractional bits. The MSB is the signed bit and the lower nine bits are the absolute values of the fractional bits. As the coefficients are stored in the on-chip memory, the default value is not defined.

The VHD VCTI coefficients have 2 taps and 32 phases. As the coefficients are symmetrical, there are 17 groups of coefficients. That is, 2-tap coefficients of phases 0–16 are stored. Each register address stores two 10-bit coefficients.

Offset Address	Register Name	Total Reset Value
0xF300–0xF340	VHDVCTICOEF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												vcticoefn2												vcticoefn1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:10]	RW	vcticoefn2	VCTI filtering coefficient 2.
[9:0]	RW	vcticoefn1	VCTI filtering coefficient 1.

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Contents

12 Audio Encoding 12-1
12.1 Overview 12-1
12.2 Features 12-1
12.3 Function Description 12-2
12.4 Operating Mode 12-3
12.5 Register Summary 12-3
12.6 Register Description 12-5
12.7 Linked List Structure 12-20

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Figures

Figure 12-1 Functional Block Diagram of VOIE 12-2
Figure 12-2 Structure of the corresponding linked list 12-21
Figure 12-3 Storage structure of the StCrtl 12-21
Figure 12-4 Channel variable structure of the G726 12-22
Figure 12-5 Channel variable structure of the ADPCM 12-22

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Tables

Table 12-1 Summary of the VOIE registers (base address: 0x2064_0000) 12-3

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12 Audio Encoding

12.1 Overview

The voice engine (VOIE) module encodes, compresses, and outputs 16-bit linear pulse code modulation (PCM) audio data. It supports data inputs at the sampling rate of 8 kHz, 16 kHz, 32 kHz, or 48 kHz and G726, G711A/U, and ADPCM outputs.

12.2 Features

The VOIE module has the following features:

- Inputs audio sampling format which supports 16-bit linear PCM in little endian mode.
- Supports the sampling rate of 8 kHz, 16 kHz, 32 kHz, or 48 kHz.
- Supports the audio frame length of 10 ms, 20 ms, 30 ms, 40 ms, 50 ms, or 60 ms.
- Supports at most 17 input audio channels for each frame (including 16 channels for encoding outputs and one channel for talkback).
- Supports 80–2880 (an integral multiple of 80) input sampling points of each frame.
- Supports the ITU-G.726 protocol providing 40 kbit/s, 32 kbit/s, 24 kbit/s, and 16 kbit/s encoding compression ratios.
- Supports ITU-G.711A/U encoding output.
- Supports the ADPCM encoding outputs in ADPCM_DVI4 and ADPCM_ORG_DVI4 encapsulation modes.
- Supports HiSilicon frame header output after encoding.
- Checks the input frames, discards the frames with errors, and reports interrupts.
- Checks the input frame length and encoding mode, discards the frames incompliant with configuration requirements, and the interrupts.
- Supports encoding of consecutive frames.

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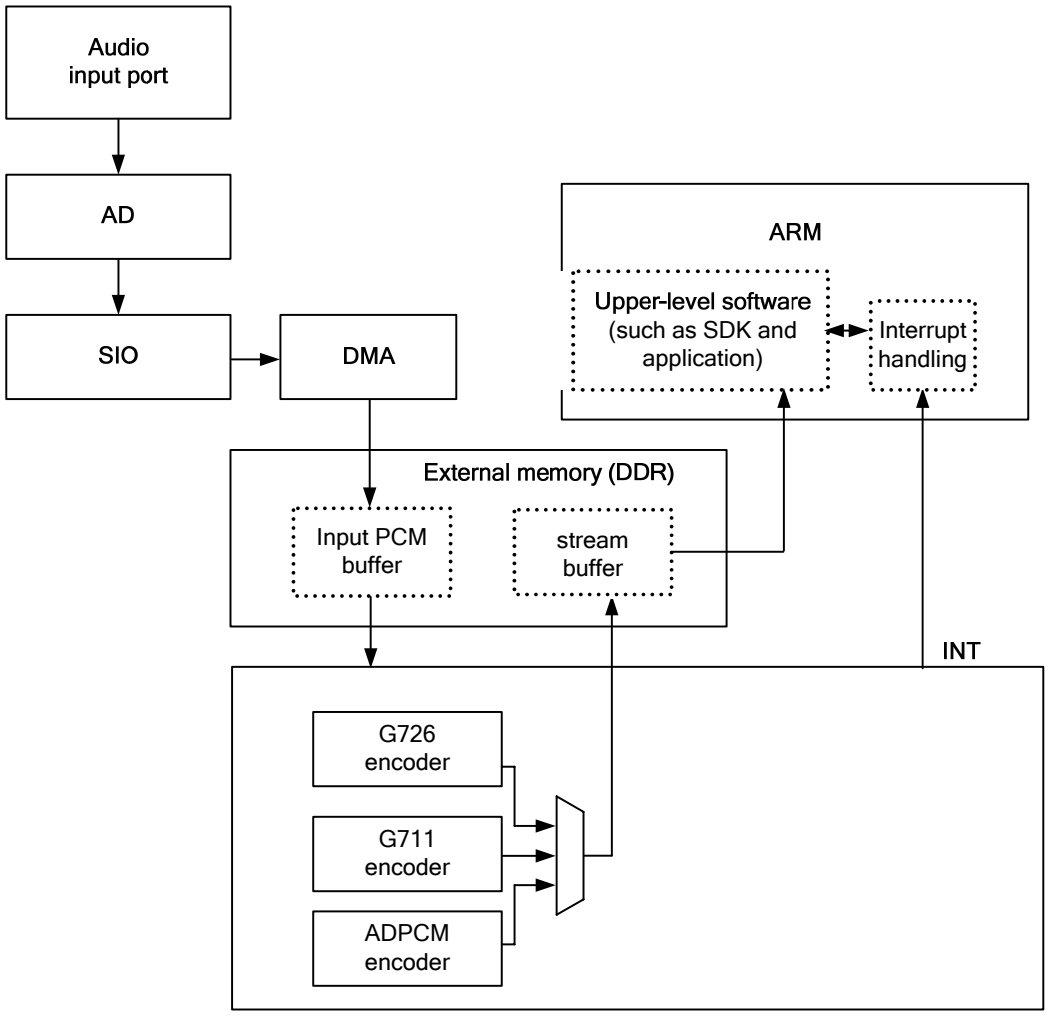
12.3 Function Description

Figure 12-1 shows the functional block diagram of the VOIE.

Figure 12-1 Functional Block Diagram of VOIE



The VOIE consists of the G726 encoder, G711 encoder, and ADPCM encoder. The encoder is selected based on the configured encoding mode.

Before the VOIE starts encoding, the audio data is input through the audio-to-digital converter (ADC), and is stored in the audio data buffer over the SIO interface (for details, see the SIO operating mode). Then the data is transferred to the DDR in DMA mode. After encoding, the VOIE stores the encoded streams in the stream buffer, and reports an interrupt, indicating that encoding of a frame of audio data is complete.

For details about encoding modes, see section 12.6 "Register Description."

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12.4 Operating Mode

The VOIE reads the linked list and voice frame data of a frame from the DDR and writes the streams to the DDR after the data is encoded by the encoder.

Before the VOIE is enabled for video encoding, the software allocates three types of buffers for the VOIE in an external DDR SDRAM:

- Input voice data buffer

  The VOIE reads the voice data to be encoded from this buffer during encoding. This buffer is written by the DMA.

- Encoding linked list configuration buffer

  When VOIE is started but encoding does not start, the VOIE reads the configuration information about the current channel from this buffer. The configuration information includes the data source address, the destination address, the channel variable address, the address of the next channel linked list, and the encoding control configuration information.

- Channel variable buffer

  The VOIE reads channel variables and check information from this buffer during encoding (the information is not required during the G711 encoding.) and refreshes the information after encoding.

  For details about the structures of the linked list and channel variables, see section 12.7 "Linked List Structure." G726_check in Figure 12-4 is the no-carry accumulated sum of the variables of eleven 32-bit channel registers. The value of ADPCM_check in Figure 12-5 is the same as the value of 32-bit channel variable registers in ADPCM encoding mode.

12.5 Register Summary

Table 12-1 describes the VOIE registers.

Table 12-1 Summary of the VOIE registers (base address: 0x2064_0000)

Offset addresses	Register	Description	Page
0x0000	VOIE_INTSTAT	Interrupt status register	12-5
0x0004	VOIE_INTMASK	Interrupt mask register	12-6
0x0008	VOIE_RAWINT	Raw interrupt status register	12-7
0x000C	VOIE_INTCLR	Interrupt clear register	12-7
0x0010	VIOE_START	Encoding start signal register	12-9
0x0014	VOIE_OUTSTDING	Outstanding configuration register	12-9
0x0020	VOIE_MODE	VOIE working mode register	12-10
0x0028	VOIE_CFG	First linked list address register	12-10
0x0030	VOIE_LLICFG0	Linked list member register (SrcPhyAddr)	12-10

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Offset addresses	Register	Description	Page
0x0034	VOIE_LLICFG1	Linked list member register (DstPhyAddr)	12-11
0x0038	VOIE_LLICFG2	Linked list member register (StatePhyAddr)	12-11
0x003C	VOIE_LLICFG3	Linked list member register (NextLLiAddr)	12-12
0x0040	VOIE_LLICFG4	Linked list member register (StCtrl)	12-12
0x0050	VOIE_LLISTATE0	G726 encoding channel variable register 0	12-14
0x0054	VOIE_LLISTATE1	G726 encoding channel variable register 1	12-14
0x0058	VOIE_LLISTATE2	G726 encoding channel variable register 2	12-15
0x005C	VOIE_LLISTATE3	G726 encoding channel variable register 3	12-15
0x0060	VOIE_LLISTATE4	G726 encoding channel variable register 4	12-16
0x0064	VOIE_LLISTATE5	G726 encoding channel variable register 5	12-16
0x0068	VOIE_LLISTATE6	G726 encoding channel variable register 6	12-17
0x006C	VOIE_LLISTATE7	G726 encoding channel variable register 7	12-17
0x0070	VOIE_LLISTATE8	G726 encoding channel variable register 8	12-18
0x0074	VOIE_LLISTATE9	G726 encoding channel variable register 9	12-18
0x0078	VOIE_LLISTATE10	G726 encoding channel variable register 10	12-19
0x007C	VOIE_STATE_CHK 0	G726 channel variable check register	12-19
0x0080	VOIE_LLISTATE11	ADPCM encoding channel variable register 11	12-20
0x0084	VOIE_STATE_CHK 1	ADPCM channel variable check register	12-20

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12.6 Register Description

VOIE_INTSTAT

VOIE_INTSTAT is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0000	VOIE_INTSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							cfgErr	reserved							chkErr	reserved							VoieEndofSingle	reserved							VoieEndOfFrame
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved.
[24]	RO	cfgErr	Configuration error flag. 0: correct 1: error
[23:17]	RO	reserved	Reserved.
[16]	RO	chkErr	Channel variable check error flag. 0: correct 1: error
[15:9]	RO	reserved	Reserved.
[8]	RO	VoieEndofSingle	Single channel encoding completion flag. 0: incomplete 1: complete
[7:1]	RO	reserved	Reserved.
[0]	RO	VoieEndOfFrame	Frame encoding completion flag. 0: incomplete 1: complete

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VOIE_INTMASK

VOIE_INTMASK is an interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0004	VOIE_INTMASK	0x0101_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							cfgErrMask	reserved							chkErrMask	reserved							VoieEndofSingleMask	reserved							VoieEndOfPicMask
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved.
[24]	RW	cfgErrMask	Configuration error flag mask enable. 0: enabled 1: disabled
[23:17]	RO	reserved	Reserved.
[16]	RW	chkErrMask	Check error flag mask enable. 0: enabled 1: disabled
[15:9]	RO	reserved	Reserved.
[8]	RW	VoieEndofSingleMask	Single channel encoding completion mask enable. 0: enabled 1: disabled
[7:1]	RO	reserved	Reserved.
[0]	RW	VoieEndOfPicMask	Frame encoding completion mask enable. 0: enabled 1: disabled

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VOIE_RAWINT

VOIE_RAWINT is a raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0008	VOIE_RAWINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							cfgErr	reserved							chkErr	reserved							VoieEndofSingle	reserved							VoieEndOfFrame
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved.
[24]	RO	cfgErr	Configuration error flag. 0: correct 1: incorrect
[23:17]	RO	reserved	Reserved.
[16]	RO	chkErr	Channel variable check error flag. 0: correct 1: error
[15:9]	RO	reserved	Reserved.
[8]	RO	VoieEndofSingle	Single channel encoding completion flag. 0: incomplete 1: complete
[7:1]	RO	reserved	Reserved.
[0]	RO	VoieEndOfFrame	Frame encoding completion flag. 0: incomplete 1: complete

VOIE_INTCLR

VOIE_INTCLR is an interrupt clear register.

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Offset Address	Register Name	Total Reset Value
0x000C	VOIE_INTCLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							cfgErrClr	reserved							chkErrClr	reserved							VoieEndofSingleClr	reserved							VoieEndOfFrameClr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved.
[24]	WC	cfgErrClr	Configuration error source interrupt clear. Writing 1 clears this bit.
[23:17]	RO	reserved	Reserved.
[16]	WC	chkErrClr	Channel variable check error flag source interrupt clear. Writing 1 clears this bit.
[15:9]	RO	reserved	Reserved.
[8]	WC	VoieEndofSingleClr	Single channel encoding completion source interrupt clear. Writing 1 clears this bit.
[7:1]	RO	reserved	Reserved.
[0]	WC	VoieEndOfFrameClr	Frame encoding completion source interrupt clear. Writing 1 clears this bit.

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VIOE_START

VIOE_START is an encoding start signal register.

Offset Address	Register Name	Total Reset Value
0x0010	VIOE_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	WO	Start	Encoding start signal. 0: not start 1: start

VOIE_OUTSTDING

VOIE_OUTSTDING is an outstanding configuration register.

Offset Address	Register Name	Total Reset Value
0x0014	VOIE_OUTSTDING	0x0000_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												xxx			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3:0]	RW	xxx	Outstanding depth of the AXI port. The depth range is 0–7.

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VOIE_MODE

VOIE_MODE is a VOIE working mode register.

Offset Address	Register Name	Total Reset Value
0x0020	VOIE_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													memClkGateEn	clkGateEn		reserved							accesslockEn	reserved							timeEn
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved.
[18]	RW	memClkGateEn	Memory clock gating enable. Note: This field is invalid and can be ignored.
[17:16]	RW	clkGateEn	Clock gating enable Note: This field is invalid and can be ignored.
[15:9]	RO	reserved	Reserved.
[8]	RW	accesslockEn	Internal configuration lock enable. Note: This field is invalid and can be ignored.
[7:2]	RO	reserved	Reserved.
[1:0]	RW	timeEn	Timeout check enable. Note: This field is invalid and can be ignored.

VOIE_CFG

VOIE_CFG is a first linked list address register.

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Offset Address	Register Name	Total Reset Value
0x0028	VOIE_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AddrOfFirstLLI																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	AddrOfFirstLLI	Address for the first linked list for storing the current audio frame. Note: The address must be configured before encoding and must be 128-bit-aligned.

VOIE_LLICFG0

VOIE_LLICFG0 is a linked list member register (SrcPhyAddr).

Offset Address	Register Name	Total Reset Value
0x0030	VOIE_LLICFG0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SrcPhyAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	SrcPhyAddr	Start physical address for storing the voice frame data to be encoded in the DDR. The address must be 128-bit-aligned. The address is written to the corresponding linked list DDR addresses by the software before encoding and is loaded by the AXI bus after encoding starts. Note: This register is provided only for readback during debugging.

VOIE_LLICFG1

VOIE_LLICFG1 is a linked list member register (DstPhyAddr).

Offset Address	Register Name	Total Reset Value
0x0034	VOIE_LLICFG1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DstPhyAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Access	Name	Description
[31:0]	RO	DstPhyAddr	The physical address of streams output to the DDR after encoding. The 128-bit address must be aligned. The address is written to the corresponding linked list DDR addresses by the software before encoding and is loaded by the AXI bus after encoding starts. Note: This register is provided only for readback during debugging.

VOIE_LLICFG2

VOIE_LLICFG2 is a linked list member register (StatePhyAddr).

Offset Address	Register Name	Total Reset Value
0x0038	VOIE_LLICFG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	StatePhyAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	StatePhyAddr	The physical address for storing the voice frame data to be encoded in the DDR. The address must be 128-bit aligned. This address must be configured during the G726 encoding and ADPCM encoding. As channel variables are not used during the G711 encoding, this register can be ignored. The address is written to the corresponding linked list DDR addresses by the software before encoding and is loaded by the AXI bus. Note: This register is provided only for readback during debugging.

VOIE_LLICFG3

VOIE_LLICFG3 is a linked list member register (NextLLiAddr).

Offset Address	Register Name	Total Reset Value
0x003C	VOIE_LLICFG3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NextLLiAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Access	Name	Description
[31:0]	RO	NextLLiAddr	Memory address of the next channel linked list. The address must be 128-bit aligned. If the current channel is the last channel of this frame, set the next linked list address to 0x000000; otherwise, the next linked list address cannot be set to 0. The address is written to the corresponding linked list DDR addresses by the software before encoding and is loaded by the AXI bus after encoding starts. Note: This register is provided only for readback during debugging.

VOIE_LLICFG4

VOIE_LLICFG4 is a linked list member register (StCtrl, encoding control).

Offset Address	Register Name	Total Reset Value
0x0040	VOIE_LLICFG4	0x0000_0081

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	SamplesPerFrame				Codec		hisi_head	reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 1

Bits	Access	Name	Description
[31:16]	RO	SamplesPerFrame	Number of audio sampling points in the current voice frame. The values range is 80–2880 and the value must an integral multiple of 80. The address is written to the corresponding linked list DDR addresses by the software before encoding and is loaded by the AXI bus after encoding starts. Note: This register is provided only for readback during debugging.

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[15:8]	RO	Codec	Encoding type configuration. 0x01: G711 Alaw 0x02: G711 Ulaw 0x03: ADPCM_DIV4 0x04: G726_16 kbps 0x05: G726_24 kbps 0x06: G726_32 kbps 0x07: G726_40 kbps 0x24: MEDIA_G726_16 kbps 0x25: MEDIA_G726_24 kbps 0x26: MEDIA_G726_32 kbps 0x27: MEDIA_G726_40 kbps 0x43: ADPCM_ORG_DIV4 Other values: invalid configuration. If the VOIE receives other configurations, an configuration error interrupt is reported. The address is written to the corresponding linked list DDR addresses by the software before encoding and is loaded by the AXI bus after encoding starts. Note: This register is provided only for readback during debugging.
[7]	RW	hisi_head	Output stream HiSilicon frame header enable. 0: exclude HiSilicon frame header 1: include HiSilicon frame header This bit is set to 0x1 by default. The address is written to the corresponding linked list DDR addresses by the software before encoding and is loaded by the AXI bus after encoding starts. Note: This register is provided only for readback during debugging.
[6:0]	RO	reserved	Reserved.

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VOIE_LLISTATE0

VOIE_LLISTATE0 is G726 encoding channel variable register 0.

Offset Address	Register Name	Total Reset Value
0x0050	VOIE_LLISTATE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	A1																A2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	A1	G726 encoding channel variable. Two-tap pole predictor coefficient 1.
[15:0]	RO	A2	G726 encoding channel variable. Two-tap pole predictor coefficient 2.

VOIE_LLISTATE1

VOIE_LLISTATE1 is G726 encoding channel variable register 1.

Offset Address	Register Name	Total Reset Value
0x0054	VOIE_LLISTATE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AP												reserved				PK1	PK2	reserved													TD
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	AP	G726 encoding channel variable. Delay speed control.
[21:16]	RO	reserved	Reserved.
[15]	RO	PK1	G726 encoding channel variable. DQ+SEZ signed bit when the delay is 1.
[14]	RO	PK2	G726 encoding channel variable. DQ+SEZ signed bit when the delay is 2.
[13:1]	RO	reserved	Reserved.
[0]	RO	TD	G726 encoding channel variable. Single audio detection signal.

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VOIE_LLISTATE2

VOIE_LLISTATE2 is G726 encoding channel variable register 2.

Offset Address	Register Name	Total Reset Value
0x0058	VOIE_LLISTATE2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	B1																B2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	B1	G726 encoding channel variable. Six-tap pole predictor coefficient 1.
[15:0]	RO	B2	G726 encoding channel variable. Six-tap pole predictor coefficient 2.

VOIE_LLISTATE3

VOIE_LLISTATE3 is G726 encoding channel variable register 3.

Offset Address	Register Name	Total Reset Value
0x005C	VOIE_LLISTATE3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	B3																B4															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	B3	G726 encoding channel variable. Six-tap pole predictor coefficient 3.
[15:0]	RO	B4	G726 encoding channel variable. Six-tap pole predictor coefficient 4.

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VOIE_LLISTATE4

VOIE_LLISTATE4 is G726 encoding channel variable register 4.

Offset Address	Register Name	Total Reset Value
0x0060	VOIE_LLISTATE4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	B5																B6															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	B5	G726 encoding channel variable. Six-tap pole predictor coefficient 5.
[15:0]	RO	B6	G726 encoding channel variable. Six-tap pole predictor coefficient 6.

VOIE_LLISTATE5

VOIE_LLISTATE5 is G726 encoding channel variable register 5.

Offset Address	Register Name	Total Reset Value
0x0064	VOIE_LLISTATE5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DML															reserved	DMS												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	DML	G726 encoding channel variable. F (I) long-term average value of the delay.
[17:16]	RO	reserved	Reserved.
[15:4]	RO	DMS	G726 encoding channel variable. F (I) short-term average value of the delay.
[3:0]	RO	reserved	Reserved.

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VOIE_LLISTATE6

VOIE_LLISTATE6 is G726 encoding channel variable register 6.

Offset Address	Register Name	Total Reset Value
0x0068	VOIE_LLISTATE6	0x0400_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQ1												reserved				DQ2												reserved			
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	DQ1	G726 encoding channel variable. Quantization difference signal when the delay is 1.
[20:16]	RO	reserved	Reserved.
[15:5]	RO	DQ2	G726 encoding channel variable. Quantization difference signal when the delay is 2.
[4:0]	RO	reserved	Reserved.

VOIE_LLISTATE7

VOIE_LLISTATE7 is G726 encoding channel variable register 7.

Offset Address	Register Name	Total Reset Value
0x006C	VOIE_LLISTATE7	0x0400_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQ3												reserved				DQ4												reserved			
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	DQ3	G726 encoding channel variable. Quantization difference signal when the delay is 3.
[20:16]	RO	reserved	Reserved.
[15:5]	RO	DQ4	G726 encoding channel variable. Quantization difference signal when the delay is 4.
[4:0]	RO	reserved	Reserved.

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VOIE_LLISTATE8

VOIE_LLISTATE8 is G726 encoding channel variable register 8.

Offset Address	Register Name	Total Reset Value
0x0070	VOIE_LLISTATE8	0x0400_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQ5												reserved				DQ6												reserved			
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	DQ5	G726 encoding channel variable. Quantization difference signal when the delay is 5.
[20:16]	RO	reserved	Reserved.
[15:5]	RO	DQ6	G726 encoding channel variable. Quantization difference signal when the delay is 6.
[4:0]	RO	reserved	Reserved.

VOIE_LLISTATE9

VOIE_LLISTATE9 is G726 encoding channel variable register 9.

Offset Address	Register Name	Total Reset Value
0x0074	VOIE_LLISTATE9	0x0400_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SR1												reserved				SR2												reserved			
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	SR1	G726 encoding channel variable. Reconstruction signal when the delay is 1.
[20:16]	RO	reserved	Reserved.
[15:5]	RO	SR2	G726 encoding channel variable. Reconstruction signal when the delay is 2.
[4:0]	RO	reserved	Reserved.

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VOIE_LLISTATE10

VOIE_LLISTATE10 is G726 encoding channel variable register 10.

Offset Address	Register Name	Total Reset Value
0x0078	VOIE_LLISTATE10	0x1100_0220

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	YL																				YU											
Reset	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	YL	G726 encoding channel variable. Low-speed quantization scaling factor.
[12:0]	RO	YU	G726 encoding channel variable. High-speed quantization scaling factor.

VOIE_STATE_CHK0

VOIE_STATE_CHK0 is a G726 channel variable check register.

Offset Address	Register Name	Total Reset Value
0x007C	VOIE_STATE_CHK0	0x2100_1220

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	g726_check																															
Reset	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	g726_check	G726 channel variable check result.

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VOIE_LLISTATE11

VOIE_LLISTATE11 is ADPCM encoding channel variable register 11.

Offset Address	Register Name	Total Reset Value
0x0080	VOIE_LLISTATE11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	valprev																reserved								index							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	valprev	ADPCM encoding channel variable, indicating the reconstruction value of the previous audio point.
[15:8]	RO	reserved	Reserved.
[7:0]	RO	index	ADPCM encoding channel variable, indicating the index value of the quantization table.

VOIE_STATE_CHK1

VOIE_STATE_CHK1 is an ADPCM channel variable check register.

Offset Address	Register Name	Total Reset Value
0x0084	VOIE_STATE_CHK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	adpcm_check																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	adpcm_check	ADPCM channel variable check result.

12.7 Linked List Structure

Figure 12-2 shows the structure and arrangement mode of the linked list in the DDR. The linked list must be written to the DDR, and the first linked list address must be written to the VOIE_CFG register whose base address is 0x2064_0028.

The structure of the linked list is as follows:

```
typedef struct hiVOICE_ENGINE_LLI_STATE
{
    HI_U32          u32SrcPhyAddr;
    HI_U32          u32DstPhyAddr;
```


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```
    HI_U32          u32StatePhyAddr;
    HI_U32          u32NextLLiAddr;
    VOICE_ENGINE_Ctrl stCtrl;
    HI_U32          u32Reserved0;
    HI_U32          u32Reserved1;
    HI_U32          u32Reserved2;
} VOICE_ENGINE_LLI_STATE;
```

Figure 12-2 Structure of the corresponding linked list

Address increment

Number of Bits	Storage Content	Description
32	SrcPhyAddr	Physical address of the memory for storing the encoding input data. The address must be 128-bit aligned.
32	DstPhyAddr	Physical address of the memory for storing the encoding output data. The address must be 128-bit aligned.
32	StatePhyAddr	Physical address of the memory for storing the encoding channel variables . The address must be 128-bit aligned.
32	NextLLiAddr	Address of the next encoding linked list. The address must be 128-bit aligned.
32	StCtrl	Encoding control architecture
32	Reserved0	Reserved for expansion
32	Reserved1	Reserved for expansion
32	Reserved2	Reserved for expansion

Figure 12-3 Storage structure of the StCrtl

Content	Reserved	hisi_head	Codec	Samples per frame
Bit Allocation	6:0	7	15:8	31:16

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Figure 12-4 Channel variable structure of the G726

Reserved to 0

Number of Bits	Storage Content	Description
32	A1[15:0] A2[15:0]	[31:16] [15:0]
32	AP[9:0] PK1 PK2 TD	[31:22] [15] [14] [0]
32	B1[15:0] B2[15:0]	[31:16] [15:0]
32	B3[15:0] B4[15:0]	[31:16] [15:0]
32	B5[15:0] B6[15:0]	[31:16] [15:0]
32	DML[13:0] DMS[11:0]	[31:18] [15:4]
32	DQ1[10:0] DQ2[10:0]	[31:21] [15:5]
32	DQ3[10:0] DQ4[10:0]	[31:21] [15:5]
32	DQ5[10:0] DQ6[10:0]	[31:21] [15:5]
32	SR1[10:0] SR2[10:0]	[31:21] [15:5]
32	YL[18:0] YU[12:0]	[31:13] [12:0]
32	G726_check	[31:0]

Address increment

Figure 12-5 Channel variable structure of the ADPCM

Reserved to 0

Number of Bit	Storage Content	Description
32	valprev[15:0] index[7:0]	[31:16] [7:0]
32	adpcm_check	[31:0]

Address decrement

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Contents

13 Audio Interfaces 13-1
13.1 Overview 13-1
13.2 Features 13-1
13.3 Function Description 13-2
13.4 Operating Mode 13-7
13.5 Register Summary 13-9
13.6 Register Description 13-11

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Figures

Figure 13-1 Connection diagram of the I^2S interface in master mode 13-2
Figure 13-2 Connections diagram of the I^2S interface in slave mode 13-3
Figure 13-3 Connections of the I^2S/PCM interface used for audio recording in master mode 13-3
Figure 13-4 Connections of the I^2S/PCM interface used for audio recording in slave mode 13-4
Figure 13-5 Connection between SIO5 and HDMI 13-4
Figure 13-6 Timing of the I^2S interface 13-5
Figure 13-7 Timing of the PCM interface in standard mode 13-5
Figure 13-8 Timing of the PCM interface in user-defined mode 13-5
Figure 13-9 Receiving 2-/4-/8-/16-channel data through the I^2S interface 13-6
Figure 13-10 Receiving 2-/4-/8-/16-channel data through the PCM interface 13-6

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Tables

Table 13-1 Summary of SIO registers 13-10

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13 Audio Interfaces

13.1 Overview

The sonic input/output (SIO) interfaces are used to connect to the external audio codec to play and record music clips (voices). The Hi3521 provides four SIO interfaces: SIO0, SIO1, SIO2, and SIO3. SIO0 and SIO1 support 8- or16-channel audio inputs. SIO2 supports the input and output of voice talkback. SIO3 is connected to the HDMI in inner-IC sound (I^2S) mode.

13.2 Features

The SIO interfaces support pulse code modulation (PCM) mode and I^2S mode. PCM interfaces are mainly used for voice channels, such as the VoIP phone, whereas I^2S interfaces are used to work with the audio codec to implement talkback and record audio clips. The SIO interfaces also support directory memory access (DMA) operations.

PCM Interfaces

The PCM interfaces have the following features:

- Support the master/slave mode.
- Transmit/receive the single-channel 8-/16-bit linear PCM code.
- Receive 2-/4-/8-/16-channel 8-/16-bit data.
- Support the bit stream clocks and frame sync signals generated internally and external clocks and sync signals.
- Support only short pulse sync signals in frame sync signals (the duration of those sync signals is one clock cycle). The PCM interfaces can work in both standard mode and user-defined mode.
- Support the function of enabling the TX channel and the RX channel independently.
- Provide independent FIFOs for the RX channel and TX channel. Each of them is 16-location deep.

I^2S Interfaces

The I^2S interfaces have the following features:

- Support the master/slave mode.

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- Transmit or receive the left-/right-channel 16-/18-/20-/24-/32-bit data.
- Receive 2-/4-/8-/16-channel 8-/16-bit data.
- Support the sampling rate ranging from 8 kHz to 192 kHz.
- Each I^2S TX channel or I^2S RX channel has its independent FIFO. The left channel and the right channel also have their independent FIFOs. The FIFO is 16-location deep and the FIFO threshold can be adjusted.
- Support the function of enabling the TX channel and the RX channel independently.
- In 16-bit transfer mode, the data received by the left and right channels can be combined into 32-bit data and then stored in the receive FIFO, and the data transmitted by the left and right channels can be combined into 32-bit data and then written to the transmit FIFO. This improves the buffer performance of FIFOs. The combination function is not supported when 2-/4-/8-/16-channel 8-/16-bit data is received.

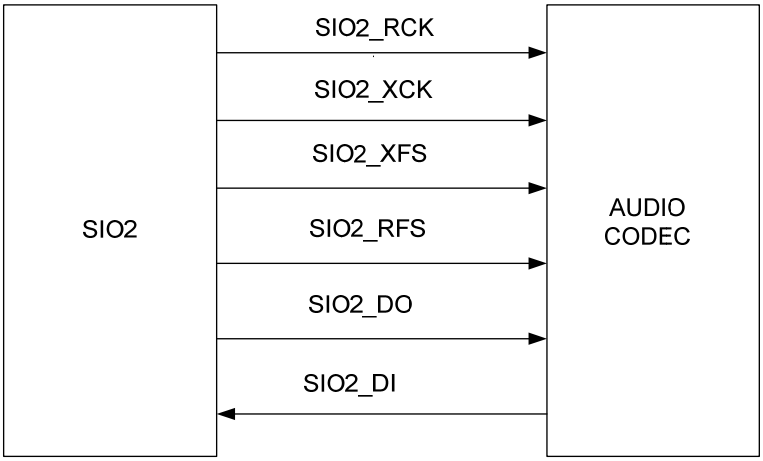
13.3 Function Description

Typical Application

SIO2 is used to input or output audios to implement talkback. The following describes the typical connections of the I^2S interface.

Figure 13-1 shows the typical connections of the I^2S interface in master mode.

Figure 13-1 Connection diagram of the I^2S interface in master mode



In master mode, the bit stream clock and audio channel select signal are sent to the audio codec by the SIO module. In slave mode, the bit stream clock and audio channel select signal are sent to the SIO module by the audio codec.

Figure 13-2 shows the typical connections of the I^2S interface in slave mode.

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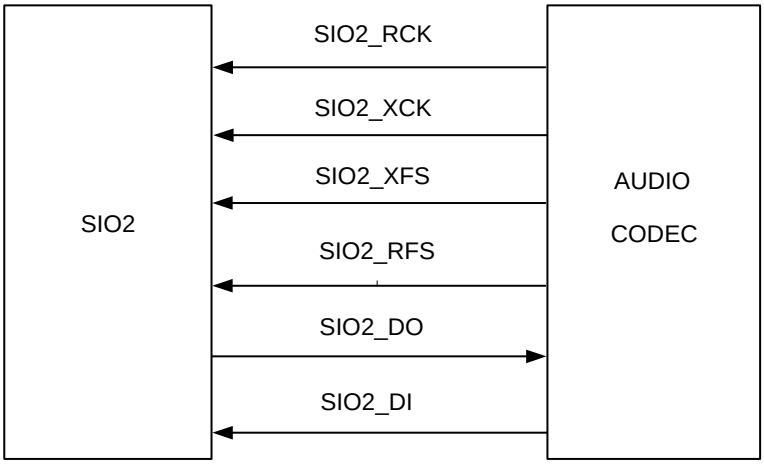
Figure 13-2 Connections diagram of the I²S interface in slave mode



The main working clock of the audio codec is the external crystal oscillator in slave mode.

Figure 13-1 shows the connections of the PCM interface when the audio codec provides the clock and sync signal in master mode. The PCM interface is connected in the same manner as the I²S interface.

Figure 13-2 shows the connections of the PCM interface when the SIO module provides the clock and sync signal in slave mode. The PCM interface is connected in the same manner as the I²S interface.

The main working clock of the audio codec is originated from the external crystal oscillator when the audio codec provides the clock and sync signal.

SIO0 and SIO1 are used to record 8-/16-channel 16-bit audio data. The following is an example using SIO0. Figure 13-3 shows the connections of the I²S/PCM interface used for audio recording in master mode. Figure 13-4 shows the connections of the I²S/PCM interface used for audio recording in slave mode.

Figure 13-3 Connections of the I²S/PCM interface used for audio recording in master mode

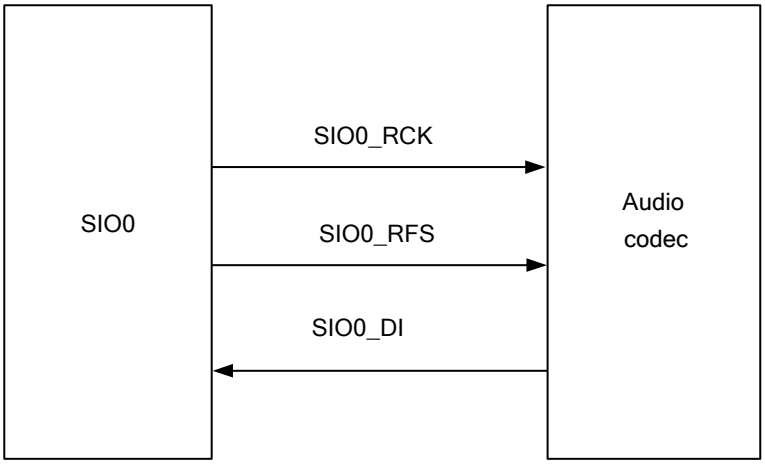


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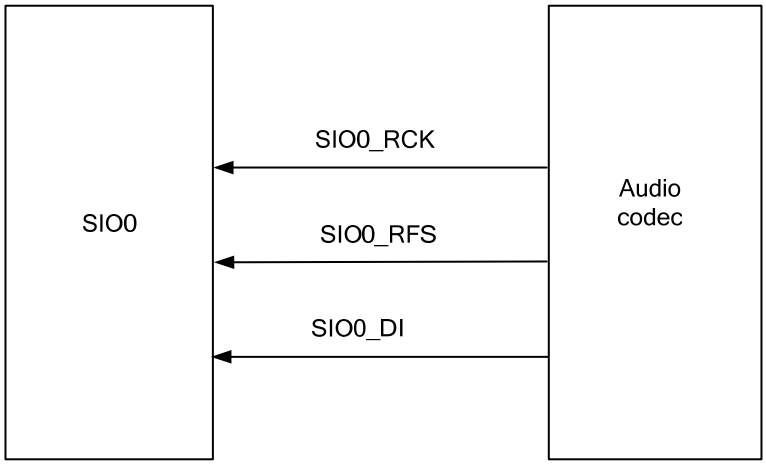
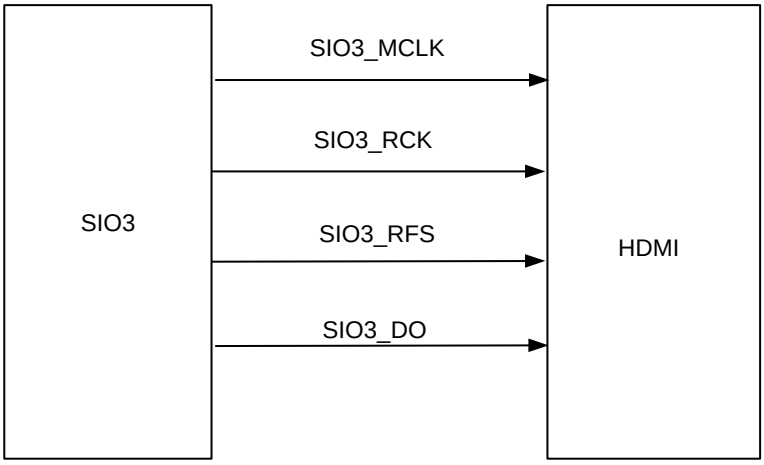
Figure 13-4 Connections of the I²S/PCM interface used for audio recording in slave mode



During audio recording, the function of receiving multi-channel audio clips is supported. That is, 2-/4-/8-/16-channel 8-/16-bit data can be received. The connection of SIO1 is the same as the preceding descriptions.

SIO3 is internally connected to the HDMI, and only the I²S master connection mode is supported.

Figure 13-5 Connection between SIO5 and HDMI



Function Principle

An SIO interface receives the audio data transmitted over the internal bus, and transmits the audio data to the interconnected audio codec over the I²S or PCM interface at a specified sampling rate. After that, the audio codec performs digital-to-analog (DA) conversion on the audio data and plays the audio. At the same time, the SIO interface receives the audio data after analog-to-digital (AD) conversion performed by the audio codec through the I²S and PCM interface, and stores the data into the internal FIFO. Then, the CPU fetches the data and stores it. In this way, the audio recording function is complete.

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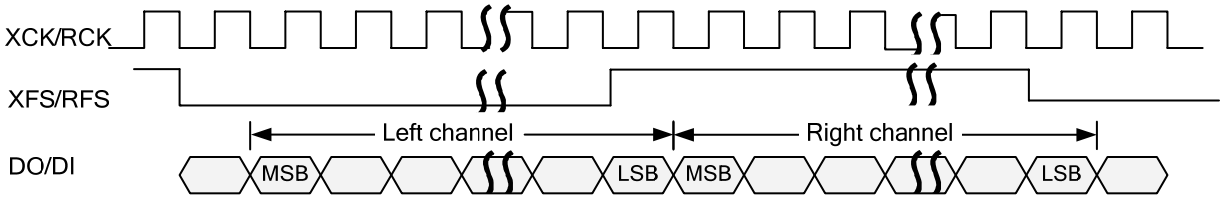
The data transferred through the I²S interface consists of the right-channel data and the left-channel data, which are distinguished from the levels of the XFS (RFS) signal. See Figure 13-5. Data is sampled on the rising edge of the XCK/RCK clock according to the protocol. The MSB is valid in next clock cycle of XFS/RFS. The MSB and LSB are transferred in sequence.

Figure 13-6 shows the timing of the I²S interface.

Figure 13-6 Timing of the I²S interface



The data through the PCM interface is the single-channel data. XFS identifies the start of the data. The MSB is transmitted or received first and data is sampled on the falling edge. In standard timing mode, the MSB is valid in the next cycle after the high-level pulse of XFS; in user-defined timing mode, the MSB is aligned with the high-level pulse of XFS.

Figure 13-7 shows the timing of the PCM interface in standard mode.

Figure 13-7 Timing of the PCM interface in standard mode

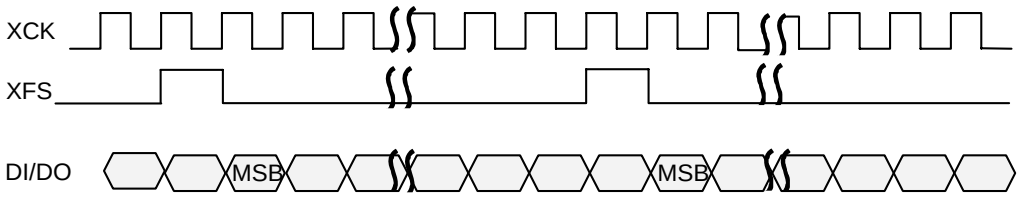
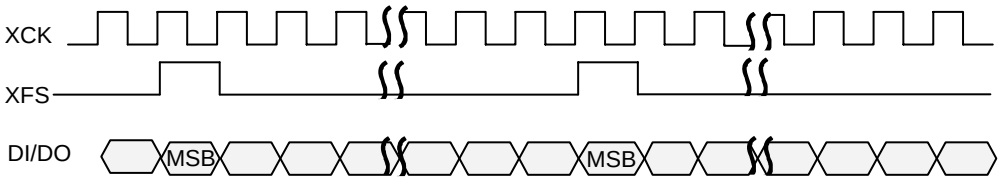


Figure 13-8 shows the timing of the PCM interface in user-defined mode.

Figure 13-8 Timing of the PCM interface in user-defined mode



When receiving 2-/4-/8-/16-channel 8-/16 bit data, the I²S interface stores the data into the left and right channels respectively. See Figure 13-9.

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Figure 13-9 Receiving 2-/4-/8-/16-channel data through the I²S interface

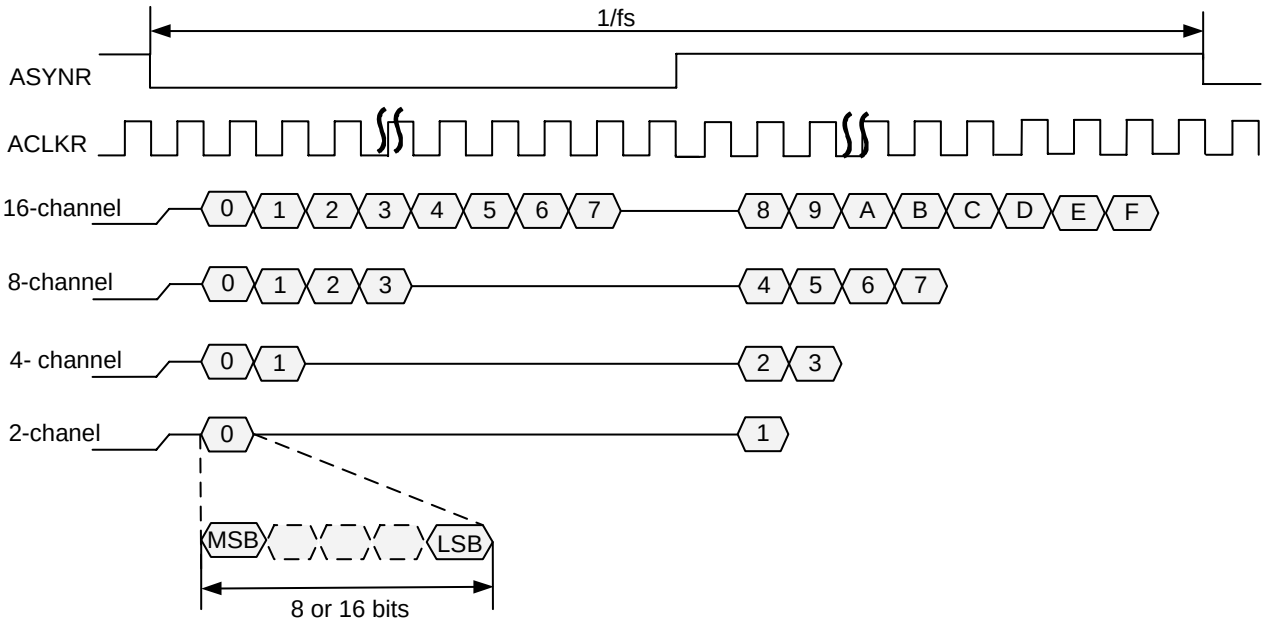
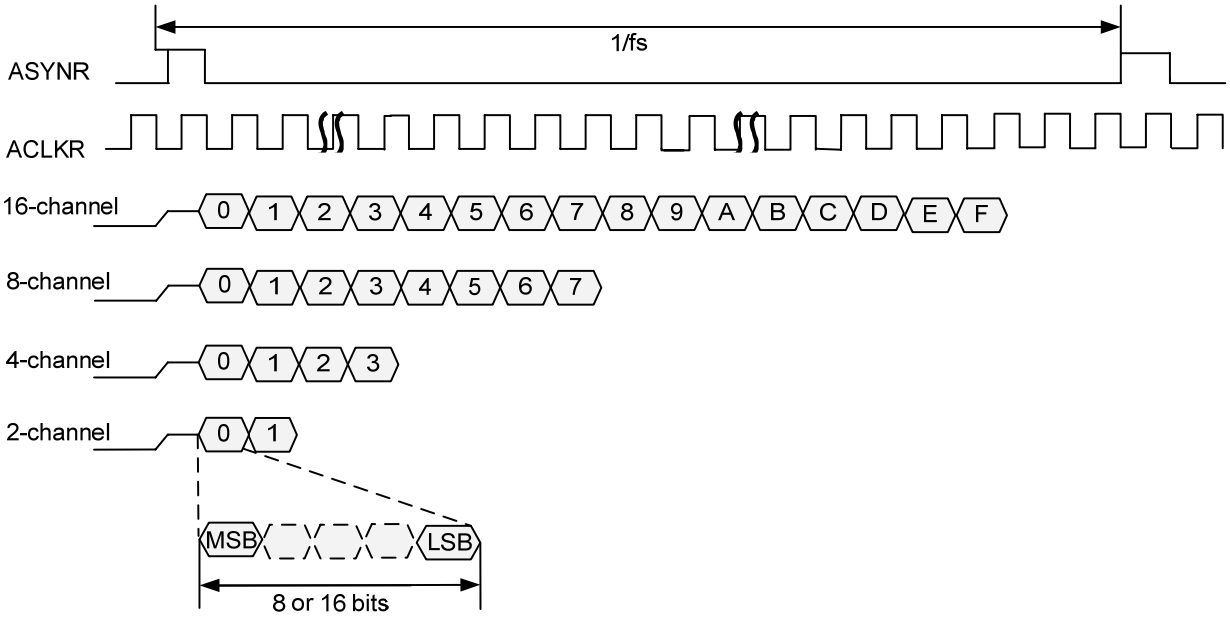


Figure 13-10 shows how data from multiple channels is received in PCM mode. Both the standard and user-defined PCM modes are supported. The difference from the single channel is that the SIO interface can receive data on the rising edge or falling edging optionally. Figure 13-10 shows how the SIO interface receives data on the rising edge in PCM mode.

Figure 13-10 Receiving 2-/4-/8-/16-channel data through the PCM interface



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13.4 Operating Mode

Clock Gating

When no audio is being recorded or played, you can configure PERI_CRG35, PERI_CRG36, PERI_CRG37, and PERI_CRG38 to disable the SIO clocks after SIO_CT_SET [rx_enable] and SIO_CT_SET [tx_enable] are set to 0. The details are as follows:

- Write 0 to PERI_CRG35 [sio0_cken] to disable the SIO0 clock.
- Write 0 to PERI_CRG36 [sio1_cken] to disable the SIO1 clock.
- Write 0 to PERI_CRG37 [sio2_cken] to disable the SIO2 clock.
- Write 0 to PERI_CRG38 [sio3_cken] to disable the SIO3 clock.

You can enable the SIO clocks by setting the related registers to 1. The details are as follows:

- Write 1 to PERI_CRG35 [sio0_cken] to enable the SIO0 clock.
- Write 1 to PERI_CRG36 [sio1_cken] to enable the SIO1 clock.
- Write 1 to PERI_CRG37 [sio2_cken] to enable the SIO2 clock.
- Write 1 to PERI_CRG38 [sio3_cken] to enable the SIO3 clock.

Clock Configuration

The four SIO interfaces work independently, but their clocks are configured in the same way. SIO0–SIO2 can work in master mode or slave mode.

SIO3 works only in master mode.

To enable an SIO interface such as SIO0 to work in master mode, set PERI_CRG35 [sio0_bclk_sel] to 1. If PERI_CRG35 [sio0_bclk_sel] is set to 0, the slave mode is selected. You also need to select the frequency dividers of the bit clock and sync clock by configuring PERI_CRG35 [sio0_bclk_div] and PERI_CRG35 [sio0_fsclk_div] respectively.

Soft Reset

The four SIO interfaces work independently, but their clocks are configured in the same way.

This section takes SIO0 as an example. SIO0 can be separately soft-reset by setting PERI_CRG35 [sio0_srst_req] to 1. After reset, each configuration register is restored its default value. Therefore, these registers must be reinitialized.

Audio Playing and Recording in Interrupt mode or Query Mode

Initialization

The initialization is implemented as follows:

Step 1 Set SIO_CT_SET/SIO_CT_CLR[rx_enable] and SIO_CT_SET/SIO_CT_CLR[tx_enable] to 0 to disable the SIO.

Step 2 Select the I^2S or PCM mode by setting SIO_MODE[sio_mode]. If you select the PCM mode, you need to select the timing type by setting SIO_MODE[pcm_mode]. If multi-channel audio recording is required, you need to set SIO_MODE[ext_rec_en], SIO_MODE[chn_num], and SIO_MODE[clk_edge].

Step 3 Configure the clock frequency in master mode and skip this step in slave mode.

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Step 4 Set the bit width by configuring SIO_DATA_WIDTH_SET and SIO_SIGNED_EXT.

Step 5 Set the thresholds of the RX FIFO and TX FIFO by configuring SIO_CT_SET[rx_fifo_threshold] and SIO_CT_SET [tx_fifo_threshold] respectively.

Step 6 In I^2S mode, configure SIO_I^2S_POS_MERGE_EN and SIO_I^2S_START_POS based on the mode of reading and writing the. In addition, configure SIO_CT_SET[tx_data_merge_en] and SIO_CT_SET[rx_data_merge_en]. For multi-channel audio recording, skip this step.

Step 7 Set the SIO interrupt mask register SIO_INTMASK and SIO_CT_SET[intr_en] as required.

Step 8 Configure the external audio codecs.

---End

Audio Playing

To play audio clips, do as follows:

Step 1 Set SIO_CT_SET [tx_fifo_disable] to 1 and then to 0 to clear the remaining data in the TX FIFO.

Step 2 Write the data to be transmitted to the TX FIFO, and write 1 to SIO_CT_SET[tx_enable] to start data transmission.

Step 3 In query mode, check the status of TX FIFO by reading SIO_TX_STA; in interrupt mode, report an interrupt according to the interrupt status indicated by SIO_INTSTATUS[tx_intr]. When the data depth of the TX FIFO is below the threshold, write data to the TX FIFO. When data is transmitted completely, go to step 4. Ensure that data underflow does not occur in the TX FIFO before data is transmitted completely. Otherwise, the sound may be discontinuous.

Step 4 Set SIO_CT_SET [tx_enable] to 0.

---End

Audio Recording

To record audio clips, do as follows:

Step 1 Set SIO_CT_SET[rx_fifo_disable] to 1 and then to 0 to clear the remaining data in the RX_FIFO.

Step 2 Set SIO_CT_SET[rx_enable] to 1 to start data reception.

Step 3 In query mode, check the status of the RX FIFO by reading SIO_RX_STA; in interrupt mode, check the status of the RX FIFO by reading the related interrupt status bit. When the data depth of the RX FIFO is above the threshold, read data from the RX FIFO. When data is received completely, go to step 4. Ensure that data overflow does not occur in the RX FIFO before data is received completely. Otherwise, data loss occurs.

Step 4 Set SIO_CT_SET[rx_enable] to 0 to read all the remaining data in the RX FIFO.

---End

Audio Playing and Recording in DMA Mode

Initialization

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The audio playing and recording in DMA mode is performed in the same way as that in interrupt mode or query mode.

Audio Playing

To play audio clips, perform the following steps:

Step 1 Set SIO_INTMASK[tx_intr] to 1 to mask transmit interrupts.

Step 2 Configure the DMA data channel, including the data transfer source address, destination address, amount of data to be transferred, and transfer type. For details, see the configuration description of DMA.

Step 3 Set SIO_CT_SET [tx_fifo_disable] to 1 and then to 0 to clear the remaining data in the TX FIFO.

Step 4 Write the initial data to the TX FIFO to ensure that the data depth is above the FIFO threshold. You can write the all-0s data, which indicates mute. If no initial data is written to the FIFO, the SIO reports FIFO underflow because the DMA does not write data to the FIFO when audio playing is started. If the initial data is written to the FIFO, the FIFO underflow upon the start of the audio playing can be prevented.

Step 5 Set SIO_CT_SET[tx_enable] to 1 to start audio playing.

Step 6 Check whether the data is transmitted completely according to the DMA interrupt. If the data is transmitted completely, set SIO_CT_SET[tx_enable] to 0.

---End

Audio Recording

To record audio clips, perform the following steps:

Step 1 Configure the DMA data channel, including the data transfer source, destination address, amount of data to be transferred, and transfer type. For details, see the configuration description of DMA.

Step 2 Set SIO_CT_SET[rx_fifo_disable] to 1 and then to 0 to clear the remaining data in the RX FIFO.

Step 3 Set SIO_CT_SET[rx_enable] to 1 to start data reception.

Step 4 If you want to stop audio recording, set SIO_CT_SET[rx_enable] to 0.

---End

13.5 Register Summary

The base addresses of the Hi3521 are as follows:

- SIO0: 0x1003_0000
- SIO1: 0x1004_0000
- SIO2: 0x1005_0000
- SIO3: 0x1006_0000

Table 13-1 describes the SIO registers.

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Table 13-1 Summary of SIO registers

Offset address	Register	Description	Page
0x03C	SIO_VERSION	SIO version register	13-11
0x040	SIO_MODE	SIO mode register	13-11
0x044	SIO_INTSTATUS	SIO interrupt status register	13-13
0x048	SIO_INTCLR	SIO interrupt clear register	13-15
0x04C	SIO_I^{2}S_LEFT_XD	I^{2}S left channel data transmit register	13-16
0x050	SIO_I^{2}S_RIGHT_XD	I^{2}S right channel data transmit register	13-16
0x050	SIO_PCM_XD	PCM data transmit register	13-16
0x054	SIO_I^{2}S_LEFT_RD	I^{2}S left channel data receive register	13-17
0x058	SIO_I^{2}S_RIGHT_RD	I^{2}S right channel data receive register	13-17
0x058	SIO_PCM_RD	PCM data receive register	13-18
0x05C	SIO_CT_SET	I^{2}S/PCM control set register	13-18
0x060	SIO_CT_CLR	I^{2}S/PCM control clear register	13-20
0x064	RESERVED	Reserved	-
0x068	SIO_RX_STA	SIO receive status register	13-22
0x06C	SIO_TX_STA	SIO transmit status register	13-23
0x070–0x074	RESERVED	Reserved	-
0x078	SIO_DATA_WIDTH_SET	I^{2}S/PCM data width configuration register	13-24
0x07C	SIO_I^{2}S_START_POS	Data access start position control register of I^{2}S left and right channels	13-25
0x080	I^{2}S_POS_FLAG	Current position status register of I^{2}S left and right channels	13-25
0x084	SIO_SIGNED_EXT	Upper-bit sign extend enable register	13-26
0x088	SIO_I^{2}S_POS_MERGE_EN	Access position merging enable of I^{2}S left and right channels	13-27
0x08C	SIO_INTMASK	SIO interrupt mask register	13-27
0x090–0x09C	RESERVED	Reserved	-

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Offset address	Register	Description	Page
0x0A0	SIO_I^{2}S_DUAL_RX_CHN	Data receive register after enabling of I^{2}S left and right channel data access position merging	13-28
0x0C0	SIO_I^{2}S_DUAL_TX_CHN	Data transmit register after enabling of I^{2}S left and right channel data access position merging	13-29

13.6 Register Description

SIO_VERSION

SIO_VERSION is an SIO version register. It is used to record the SIO version number and perform the SIO self-test.

offset Address	Register Name	Total Reset Value
0x03C	SIO_VERSION	0x0000_0013

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							sio_loop	version							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved.
[8]	RW	sio_loop	SIO loop or normal mode select. 0: normal mode 1: Data transmit and receive loop mode. It is used for the self-test of the SIO. In the mode, the SIO receive serial data line is directly connected to the SIO transmit serial data line at the external interface of the SIO.
[7:0]	RO	version	Version number of the SIO.

SIO_MODE

SIO_MODE is an SIO mode register. It is used to select the basic operating mode of the SIO as follows:

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- In master mode, the clock reset generator (CRG) transmits clocks and sync signals to the codec and SIO.
- In slave mode, the external codec transmits clocks and sync signals to the SIO.

For details about the master/slave mode selection of the I^2S or PCM, see "Clock Configuration" in section 13.1.4 "Operating Mode."

offset Address	Register Name	Total Reset Value
0x040	SIO_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									clk_edge	chn_num		ext_rec_en	reserved	pcm_mode	sio_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	-	reserved	Reserved.
[6]	RW	clk_edge	Clock edge on which data is sampled during multi-channel data reception in PCM mode. 0: falling edge 1: rising edge
[5:4]	RW	chn_num	Number of channels during multi-channel data receive. 00: 2 channels 01: 4 channels 10: 8 channels 11: 16 channels
[3]	RW	ext_rec_en	In standard data receive mode, the I^2S interface receives both the left-channel and right-channel data. The PCM interface, however, receives the right-channel data or left-channel data. For the I^2S/PCM interface in multi-channel data receive mode, the number of channels is configurable. Additionally, the bit width of the channels must be 8 bits or 16 bits. 0: standard data receive mode of the I^2S/PCM interface 1: extended multi-channel data receive mode of the I^2S/PCM interface
[2]	-	reserved	Reserved. This bit must be set to 0.
[1]	RW	pcm_mode	PCM timing mode. 0: standard mode 1: user-defined mode
[0]	RW	sio_mode	PCM/I^2S mode select. 0: I^2S mode 1: PCM mode

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SIO_INTSTATUS

SIO_INTSTATUS is an SIO interrupt status register.

Take the receive interrupt as an example. When the data depth of the RX FIFO is above the threshold, the high level is always latched to the interrupt status register and the interrupts are generated continuously. That is, even if the CPU clears the interrupt, the interrupt status register is set to 1 in the next clock cycle. Therefore, the following processing mode of the CPU is recommended:

Step 1 Write 1 to SIO_CT_CLR[intr_en] to disable the global interrupt enable bit.

Step 2 Read the interrupt status register SIO_INTSTATUS.

Step 3 Perform related operations according to the interrupt source.

Step 4 Write 1 to the related bit of SIO_INTCLR to clear the interrupt.

Step 5 Write 1 to SIO_CT_SET[intr_en] to enable the global interrupt enable bit.

---End

The transmit interrupt and receive interrupt are generated in the same way. Therefore, it is recommended that the transmit interrupt is processed in the similar way.

This register is a raw interrupt status register. If the related interrupt bit is masked and the interrupt condition is met, the related interrupt status bit is set to 1 and no interrupt is triggered.

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Offset Address	Register Name	Total Reset Value
0x044	SIO_INTSTATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										tx_left_fifo_under	tx_right_fifo_under	rx_left_fifo_over	rx_right_fifo_over	tx_intr	rx_intr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	-	reserved	Reserved.
[5]	RO	tx_left_fifo_under	In I^2S mode, this bit indicates the left channel TX FIFO underflow interrupt status. In PCM mode, this bit is invalid. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	tx_right_fifo_under	In I^2S mode, this bit indicates the right channel TX FIFO underflow interrupt status. In PCM mode, this bit indicates the PCM TX_FIFO underflow flag. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	rx_left_fifo_over	In I^2S mode, this bit indicates the left channel RX FIFO overflow interrupt status. In PCM mode, this bit is invalid. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	rx_right_fifo_over	In I^2S mode, this bit indicates the right channel RX FIFO overflow interrupt status. In PCM mode, this bit indicates the PCM RX_FIFO overflow flag. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	tx_intr	Interrupt status when the TX FIFO is below the threshold. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	rx_intr	Interrupt status when the RX FIFO is above the threshold. 0: No interrupt is generated. 1: An interrupt is generated.

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SIO_INTCLR

SIO_INTCLR is an SIO interrupt clear register. It can be cleared by bits.

Offset Address	Register Name	Total Reset Value
0x048	SIO_INTCLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										tx_left_fifo_under	tx_right_fifo_under	rx_left_fifo_over	rx_right_fifo_over	tx_intr	rx_intr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	-	reserved	Reserved.
[5]	WO	tx_left_fifo_under	In I^2S mode, this bit indicates left channel TX FIFO underflow interrupt clear. In PCM mode, this bit is invalid. 0: not cleared 1: cleared
[4]	WO	tx_right_fifo_under	In I^2S mode, this bit indicates right channel TX FIFO underflow interrupt clear. In PCM mode, this bit indicates PCM TX FIFO underflow interrupt clear. 0: not cleared 1: cleared
[3]	WO	rx_left_fifo_over	In I^2S mode, it indicates left channel RX FIFO overflow interrupt clear. In PCM mode, this bit is invalid. 0: not cleared 1: cleared
[2]	WO	rx_right_fifo_over	In I^2S mode, this bit indicates right channel RX FIFO overflow interrupt clear. In PCM mode, this bit indicates the PCM RX_FIFO overflow interrupt clear. 0: not cleared 1: cleared
[1]	WO	tx_intr	Interrupt clear when the TX FIFO is below the threshold. 0: not cleared 1: cleared
[0]	WO	rx_intr	Interrupt clear when the RX FIFO is above the threshold. 0: not cleared 1: cleared

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SIO_I²S_LEFT_XD

SIO_I²S_LEFT_XD is an I²S left channel data transmit register.

The SIO module places the valid data in the lower-bit area when writing data to the register. For example, when the data width is 8 bits, bit[7:0] are valid and bit[31:8] are invalid; when the data width is 16 bits, bit[15:0] are valid and bit[31:16] are invalid. The bits beyond the valid data width are automatically set to 0 by the SIO module.

offset Address	Register Name	Total Reset Value
0x04C	SIO_I²S_LEFT_XD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_left_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	tx_left_data	Left channel transmit data.

SIO_I²S_RIGHT_XD

SIO_I²S_LEFT_XD is an I²S right channel data transmit register, which is multiplexed with the PCM data transmit register SIO_PCM_XD.

The SIO module places the valid data in the lower-bit area when writing data to the register. For example, when the data width is 8 bits, bit[7:0] are valid and bit[31:8] are invalid; when the data width is 16 bits, bit[15:0] are valid and bit[31:16] are invalid. The bits beyond the valid data width are automatically set to 0 by the SIO module.

Offset Address	Register Name	Total Reset Value
0x050	SIO_I²S_RIGHT_XD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_right_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	tx_right_data	Right channel transmit data.

SIO_PCM_XD

SIO_PCM_XD is a PCM data transmit register, which is multiplexed with SIO_I²S_RIGHT_XD.

The SIO module places the valid data in the lower bit area when writing the valid data to the register. For example, when the data width is 8 bits, bit[7:0] are valid and bit[31:8] are invalid.

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When the data width is 16 bits, bit[15:0] are valid and bit[31:16] are invalid. The bits beyond the valid data width are automatically set to 0 by the SIO module.

Offset Address	Register Name	Total Reset Value
0x050	SIO_PCM_XD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx__data															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	WO	tx_data	PCM transmit data.

SIO_I²S_LEFT_RD

SIO_I^{2}S_LEFT_RD is an I^{2}S left channel data receive register.

The SIO module places the received valid data in the low-bit area of the register. For example, when the data width is 8 bits, bit[7:0] are valid and bit[31:8] are invalid; when the data width is 16 bits, bit[15:0] are valid and bit[31:16] are invalid. The bits beyond the valid data width are automatically set to 0 by the SIO module.

Offset Address	Register Name	Total Reset Value
0x054	SIO_I^{2}S_LEFT_RD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_left_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rx_left_data	I^{2}S left channel receive data.

NOTE

When data reception is disabled in I^{2}S mode, the right-channel data may not be written to the FIFO. In this case, the left-channel FIFO has one data segment more than the right-channel FIFO. Therefore, the data in the left-channel and right-channel FIFOs must be cleared before the CPU starts the next data reception.

SIO_I²S_RIGHT_RD

SIO_I^{2}S_RIGHT_RD is an I^{2}S right channel data receive register, which is multiplexed with the PCM data receive register SIO_PCM_RD.

The SIO module places the received valid data in the low-bit area of the register. For example, when the data width is 8 bits, bit[7:0] are valid and bit[31:8] are invalid; when the data width

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is 16 bits, bit[15:0] are valid and bit[31:16] are invalid. The bits beyond the valid data width are automatically set to 0 by the SIO module.

Offset Address	Register Name	Total Reset Value
0x058	SIO_I2S_RIGHT_RD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_right_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rx_right_data	I2S right channel receive data.

NOTE

When data reception is disabled in I2S mode, the right-channel data may not be written to the FIFO. In this case, the left-channel FIFO has one data segment more than the right-channel FIFO. Therefore, the data in the left-channel and right-channel FIFOs must be cleared before the CPU starts the next data reception.

SIO_PCM_RD

SIO_PCM_RD is a PCM data receive register, which is multiplexed with SIO_I2S_RIGHT_RD.

The SIO module places the received valid data in the low-bit area of the register. For example, when the data width is 8 bits, bit[7:0] are valid and bit[31:8] are invalid; when the data width is 16 bits, bit[15:0] are valid and bit[31:16] are invalid. The bits beyond the valid data width are automatically set to 0 by the SIO module.

Offset Address	Register Name	Total Reset Value
0x058	SIO_PCM_RD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rx__data															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RO	rx_data	PCM receive data.

SIO_CT_SET

To operate the SIO control register by bits, the SIO_CT_SET register with the address 0x05C is provided. When 1 is written to the related bit of the register, the bit is set to 1. Writing 0 has no effect. This is a read/write register.

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Offset Address	Register Name	Total Reset Value
0x05C/0x060	SIO_CT_SET	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rst_n	intr_en	rx_enable	tx_enable	rx_fifo_disable	tx_fifo_disable	rx_data_merge_en	tx_data_merge_en	rx_fifo_threshold				tx_fifo_threshold			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15]	RW	rst_n	I^2S/PCM channel reset, active low. This bit is used to reset the transmit and receive modules (including the FIFOs) in I^2S/PCM mode. Therefore, the RX FIFO and TX FIFO status registers are changed to 0. This bit does not reset the CPU interface register module.
[14]	RW	intr_en	Global interrupt enable. 0: disabled 1: enabled
[13]	RW	rx_enable	RX channel enable. 0: disabled 1: enabled
[12]	RW	tx_enable	TX channel enable. 0: disabled 1: enabled
[11]	RW	rx_fifo_disable	RX FIFO disable. 0: enabled 1: disabled
[10]	RW	tx_fifo_disable	TX FIFO disable. 0: enabled 1: disabled

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[9]	RW	rx_data_merge_en	Data receive merging enable. This bit is valid only when the data width is 16 bits in I^2S mode. 0: disabled 1: enabled If this bit is 1, the left-channel and right-channel data is merged into a 32-bit data and then is stored in the FIFO. The left-channel 16 bits occupy the 16 MSBs, and the right-channel 16 bits occupy the 16 LSBs. Therefore, the usage and buffer capacity of the FIFO is improved. The CPU reads data from the RX_FIFO in the following order. That is, reads the 32-bit data (formed by merging the16-bit left-channel data and 16-bit right-channel data) from the left-channel FIFO, and then reads the 32-bit data from the right-channel FIFO. The CPU reads data in this manner repeatedly.
[8]	RW	tx_data_merge_en	Data transmit merging enable. It is valid only when the data bit width is 16 bits in I^2S mode. 0: disabled 1: enabled If this bit is 1, the left-channel and right-channel data is merged into a 32-bit data and then is stored in the FIFO. The left-channel 16 bits occupy the 16 MSBs, and the right-channel 16 bits occupy the 16 LSBs. Therefore, the usage and buffer capacity of the FIFO is improved. The CPU writes data into the TX_FIFO in the following order. That is, writes the 32-bit data (formed by merging the16-bit left-channel data and 16-bit right-channel data) to the left-channel FIFO, and then writes the 32-bit data to the right-channel FIFO. The CPU writes data in this manner repeatedly.
[7:4]	RW	rx_fifo_threshold	RX_FIFO threshold. When rx_right_depth ≥ (rx_fifo_threshold + 1), the receive interrupt and DMA request are reported.
[3:0]	RW	tx_fifo_threshold	TX_FIFO threshold. When the tx_right_depth < (tx_fifo_threshold + 1), the transmit interrupt and DMA request are reported.

SIO_CT_CLR

To facilitate the bit operation on the SIO control register, the SIO_CT_CLR register with the address of 0x06 is provided. When 1 is written to the related bit of the register, the bit is set to 1. Writing 0 has no effect. This is a write-only register.

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Offset Address	Register Name	Total Reset Value
0x05C/0x060	SIO_CT_SET	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rst_n	intr_en	rx_enable	tx_enable	rx_fifo_disable	tx_fifo_disable	rx_data_merge_en	tx_data_merge_en	rx_fifo_threshold				tx_fifo_threshold			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15]	RW	rst_n	I^2S/PCM channel reset, active low. This bit is used to reset the transmit and receive modules (including the FIFOs) in I^2S/PCM mode. Therefore, the RX_FIFO and TX_FIFO status registers are changed to 0. This bit does not reset the CPU interface register module.
[14]	RW	intr_en	Global interrupt enable. 0: disabled 1: enabled
[13]	RW	rx_enable	RX channel enable. 0: disabled 1: enabled
[12]	RW	tx_enable	TX channel enable. 0: disabled 1: enabled
[11]	RW	rx_fifo_disable	RX FIFO enable. 0: enabled 1: disabled
[10]	RW	tx_fifo_disable	TX FIFO disable. 0: enabled 1: disabled

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[9]	RW	rx_data_merge_en	Data receive merging enable. This bit is valid only when the data width is 16 bits in I^2S mode. 0: disabled 1: enabled If this bit is 1, the left-channel and right-channel data is merged into a 32-bit data and then is stored in the FIFO. The left-channel 16 bits occupy the upper 16 bits, and the right-channel 16 bits occupy the lower16 bits. Therefore, the usage and buffer capacity of the FIFO is improved. The CPU reads data from the RX FIFO in the following sequence. That is, the 32-bit data (formed by merging the16-bit left-channel data and 16-bit right-channel data) from the left-channel FIFO and the 32-bit data from the right-channel FIFO are read in sequence. The CPU reads data in this manner repeatedly.
[8]	RW	tx_data_merge_en	Data transmit merging enable. It is valid only when the data bit width is 16 bits in I^2S mode. 0: disabled 1: enabled If this bit is 1, the left-channel and right-channel data is merged into a 32-bit data and then is stored in the FIFO. The left-channel 16 bits occupy the upper 16 bits, and the right-channel 16 bits occupy the lower 16 bits. Therefore, the usage and buffer capacity of the FIFO is improved. The CPU writes data into the TX_FIFO in the following sequence. That is, the 32-bit data (formed by merging the16-bit left-channel data and 16-bit right-channel data) is written to the left-channel FIFO, and then the 32-bit data is written to the right-channel FIFO. The CPU writes data in this manner repeatedly.
[7:4]	RW	rx_fifo_threshold	RX FIFO threshold. When the following condition is met, the receive interrupt and DMA request are reported: rx_right_depth ≥ (rx_fifo_threshold + 1)
[3:0]	RW	tx_fifo_threshold	TX FIFO threshold. When the following condition is met, the transmit interrupt and DMA request are reported: tx_right_depth < (tx_fifo_threshold + 1)

SIO_RX_STA

SIO_RX_STA is an SIO receive status register.

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Offset Address	Register Name	Total Reset Value
0x068	SIO_RX_STA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						rx_left_depth					rx_right_depth					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	-	reserved	Reserved.
[9:5]	RO	rx_left_depth	Left channel RX FIFO depth indicator. These bits are valid only in I^2S mode.
[4:0]	RO	rx_right_depth	In I^2S mode, it indicates the right channel RX FIFO depth indicator. In PCM mode, it indicates the PCM RX FIFO depth indicator.

SIO_TX_STA

SIO_TX_STA is an SIO transmit status register.

Offset Address	Register Name	Total Reset Value
0x06C	SIO_TX_STA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						tx_left_depth					tx_right_depth					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9:5]	RO	tx_left_depth	Left channel TX FIFO depth indicator. These bits are valid only in I^2S mode.
[4:0]	RO	tx_right_depth	In I^2S mode, it indicates the right channel TX FIFO depth indicator. In PCM mode, it indicates the PCM TX FIFO depth indicator

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SIO_DATA_WIDTH_SET

SIO_DATA_WIDTH_SET is an I²S/PCM data width configuration register.

Offset Address	Register Name	Total Reset Value
0x078	SIO_DATA_WIDTH_SET	0x0000_0009

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								reserved		rx_mode			tx_mode		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bits	Access	Name	Description
[31:6]	-	reserved	Reserved.
[5:3]	RW	rx_mode	Length of the data to be received. 000: 8 bits 001: 16 bits 010: 18 bits 011: 20 bits 100: 24 bits. 101: 32 bits. 110–111: reserved The data length of 16 bits, 18 bits, 20 bits, 24 bits, or 32 bits is supported in I²S mode. The data length of 8 bits or 16 bits is supported in PCM mode. For multi-channel data reception, only the data length of 8 bits or 16 bits is supported in I²S or PCM mode.
[2:0]	RW	tx_mode	Length of the data to be transmitted. For the I²S mode: 000: reserved 001: 16 bits 010: 18 bits 011: 20 bits 100: 24 bits. 101: 32 bits. 110–111: reserved For the PCM mode 000: 8 bits 001: 16 bits 010: 32 bits 011: 64 bits 100: 128 bits 101–111: reserved

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SIO_I²S_START_POS

SIO_I²S_START_POS is a start operation position control register of I²S left and right channels.

This register controls whether the initial access starts from the left channel or right channel after the left-channel and right-channel data access address merging is enabled.

Offset Address	Register Name	Total Reset Value
0x07C	SIO_I²S_START_POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														start_pos_write	start_pos_read
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved.
[1]	RW	start_pos_write	When writing data to the TX FIFO: 0: Start the access from the left channel. 1: Start the access from the right channel.
[0]	RW	start_pos_read	When reading data from the RX FIFO: 0: Start the access from the left channel. 1: Start the access from the right channel.

I²S_POS_FLAG

I²S_POS_FLAG is a current operation position status register of I²S left and right channels.

This register controls whether the subsequent access starts from the left channel or the right channel after the left-channel and right-channel data access address merging is enabled.

Offset Address	Register Name	Total Reset Value
0x080	I²S_POS_FLAG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														start_pos_write	start_pos_read
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Access	Name	Description
[31:2]	-	reserved	Reserved.
[1]	RO	start_pos_write	When writing data into the TX FIFO: 0: Start the subsequent access from the left channel. 1: Start the subsequent access from the right channel.
[0]	RO	start_pos_read	When reading data from the RX FIFO: 0: Start the subsequent access from the left channel. 1: Start the subsequent access from the right channel.

SIO_SIGNED_EXT

SIO_SIGNED_EXT is an upper-bit sign extend enable register. This upper-bit sign extend enable bit is valid only for the received data rather than the transmitted data. The sign extension function is supported by the received data in PCM and I^{2}S modes.

Assume that the received valid data width is 8 bits, 16 bits, 18 bits, 20 bits, or 24 bits and the upper-bit sign extend enable bit is enabled. When the receive data is converted into 32-bit data, the invalid upper bit of the 32 bits are set to the value corresponding to the MSB of the received data and then written to the RX FIFO.

The following example is based on the data width of 16 bits:

```
if (data_rx[15] == 1)
data_rx[31:16] = 0xffff;
else
data_rx[31:16] = 0x0000;
```

Offset Address	Register Name	Total Reset Value
0x084	SIO_SIGNED_EXT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															signed_ext_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	signed_ext_en	Upper-bit sign extend enable. 0: disabled 1: enabled

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SIO_I²S_POS_MERGE_EN

SIO_I²S_POS_MERGE_EN is a data access position merging enable register of the I²S left and right channels.

When you read/write the FIFO data of the SIO in DMA mode over the I²S interface, the CPU needs to continuously configure the DMA operation addresses due to the different data addresses of the left and right channels. To improve the CPU efficiency, the access position merging bit of the left-channel and right-channel is used.

When the access position merging bit is enabled, both the right-channel and left-channel data is read through SIO_I²S_DUAL_RX_CHN register and written through the SIO_I²S_DUAL_TX_CHN register.

Offset Address	Register Name	Total Reset Value
0x088	SIO_I2S_POS_MERGE_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															merge_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	merge_en	Data access position merging enable of the I²S left and right channels. 0: disabled 1: enabled

SIO_INTMASK

SIO_INTMASK is an SIO Interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x08C	SIO_INTMASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										tx_left_fifo_under	tx_right_fifo_under	rx_left_fifo_over	rx_right_fifo_over	tx_intr	rx_intr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

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Bits	Access	Name	Description
[31:6]	-	reserved	Reserved.
[5]	RW	tx_left_fifo_under	In I^{2}S mode, this bit indicates left channel TX FIFO underflow interrupt mask. In PCM mode, this bit is invalid. 0: not masked 1: masked
[4]	RW	tx_right_fifo_under	In I^{2}S mode, this bit indicates right channel TX FIFO underflow interrupt mask. In PCM mode, this bit indicates PCM TX FIFO underflow interrupt mask. 0: not masked 1: masked
[3]	RW	rx_left_fifo_over	In I^{2}S mode, this bit indicates left channel RX FIFO overflow interrupt mask. In PCM mode, this bit is invalid. 0: not masked 1: masked
[2]	RW	rx_right_fifo_over	In I^{2}S mode, this bit indicates right channel RX FIFO overflow interrupt mask. In PCM mode, this bit indicates PCM RX FIFO overflow interrupt mask. 0: not masked 1: masked
[1]	RW	tx_intr	Interrupt mask when the TX_FIFO is below the threshold. 0: not masked 1: masked
[0]	RW	rx_intr	Interrupt mask when the RX_FIFO is above the threshold. 0: not masked 1: masked

SIO_I²S_DUAL_RX_CHN

SIO_I2S_DUAL_RX_CHN is a data receive register after enabling of I^{2}S left and right channel data access position merging.

Offset Address	Register Name	Total Reset Value
0x0A0	SIO_I2S_DUAL_RX_CHN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rx_data	Received data.

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SIO_I²S_DUAL_TX_CHN

SIO_I^{2}S_DUAL_TX_CHN is a data transmit register after enabling of I^{2}S left and right channel data access position merging.

Offset Address	Register Name	Total Reset Value
0x0C0	SIO_I^{2}S_DUAL_TX_CHN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	tx_data	Transmitted data.

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Contents

14 Peripherals 14-1
14.1 I²C Controller 14-1
14.1.1 Overview 14-1
14.1.2 Function Description 14-1
14.1.3 Operating Mode 14-1
14.1.4 Register Summary 14-3
14.1.5 Register Description 14-4
14.2 SPI 14-11
14.2.1 Overview 14-11
14.2.2 Features 14-12
14.2.3 Function Description 14-12
14.2.4 Peripheral Bus Timings 14-14
14.2.5 Operating Mode 14-20
14.2.6 Register Summary 14-23
14.2.7 Register Description 14-24
14.3 UART 14-33
14.3.1 Overview 14-33
14.3.2 Features 14-33
14.3.3 Function Description 14-34
14.3.4 Operating Mode 14-35
14.3.5 Register Summary 14-38
14.3.6 Register Description 14-38
14.4 IR Interface 14-52
14.4.1 Overview 14-52
14.4.2 Features 14-52
14.4.3 Function Description 14-52
14.4.4 Operating Mode 14-60
14.4.5 Register Summary 14-62
14.4.6 Register Description 14-63
14.5 GPIO 14-80
14.5.1 Overview 14-80
14.5.2 Features 14-80

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14.5.3 Function Description 14-81
14.5.4 Operating Mode 14-81
14.5.5 Register Summary 14-82
14.5.6 Register Description 14-83
14.6 USB 2.0 Host 14-88
14.6.1 Overview 14-88
14.6.2 Function Description 14-89
14.6.3 Operating Mode 14-91
14.6.4 Register Summary 14-93
14.6.5 Register Description 14-93
14.7 MMC/SD/SDIO Controller 14-97
14.7.1 Function Description 14-97
14.7.2 Timing and Parameters 14-103
14.7.3 Application Notes 14-104
14.7.4 Register Summary 14-118
14.7.5 Register Description 14-119
14.8 SATA 14-143
14.8.1 Overview 14-143
14.8.2 Features 14-143
14.8.3 Signal Description 14-143
14.8.4 Function Description 14-144
14.8.5 Operating Mode 14-146
14.8.6 Register Summary 14-149
14.8.7 Register Description 14-151
14.8.8 Appendix A Format of the SATA Command Linked List 14-186

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Figures

Figure 14-1 Process of transmitting data through the I^{2}C master 14-2
Figure 14-2 Process of receiving data through the I^{2}C master 14-3
Figure 14-3 Application block diagram when the SPI is connected to a single slave device 14-13
Figure 14-4 Application block diagram when the SPI is connected to multiple slave devices 14-13
Figure 14-5 SPI single frame format (SPO = 0, SPH = 0) 14-14
Figure 14-6 SPI continuous frame format (SPO = 0, SPH = 0) 14-14
Figure 14-7 SPI single frame format (SPO = 0, SPH = 1) 14-15
Figure 14-8 SPI continuous frame format (SPO = 0, SPH = 1) 14-15
Figure 14-9 SPI single frame format (SPO = 1, SPH = 0) 14-16
Figure 14-10 SPI continuous frame format (SPO = 1, SPH = 0) 14-16
Figure 14-11 SPI single frame format (SPO = 1, SPH = 1) 14-17
Figure 14-12 SPI continuous frame format (SPO = 1, SPH = 1) 14-17
Figure 14-13 SPI timings 14-18
Figure 14-14 TI synchronous serial single frame format 14-18
Figure 14-15 TI synchronous serial continuous frame format 14-19
Figure 14-16 National semiconductor microwire single frame format 14-19
Figure 14-17 National semiconductor microwire continuous frame format 14-20
Figure 14-18 Typical application block diagram of the UART 14-34
Figure 14-19 Frame format of the UART 14-34
Figure 14-20 Frame format for transmitting a single NEC with simple repeat code 14-55
Figure 14-21 Frame format for transmitting NEC with simple repeat codes by pressing the key continuously 14-55
Figure 14-22 Definitions of bit0 and bit1 of the NEC with simple repeat code 14-55
Figure 14-23 Format for transmitting a single NEC with simple repeat code 14-55
Figure 14-24 Code format for transmitting consecutive NEC with simple repeat codes 14-56
Figure 14-25 Frame format for transmitting a single NEC with full repeat code 14-56
Figure 14-26 Frame format for transmitting NEC with full repeat codes by pressing the key continuously 14-56

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Figure 14-27 Definitions of bit0 and bit1 of the NEC with full repeat code 14-57
Figure 14-28 Format for transmitting a single NEC with full repeat code 14-57
Figure 14-29 Frame format for transmitting a single TC9012 code 14-58
Figure 14-30 Frame format for transmitting TC9012 codes by pressing the key continuously 14-58
Figure 14-31 Definitions of bit0 and bit1 of the TC9012 code 14-58
Figure 14-32 Format for transmitting a single TC9012 code 14-58
Figure 14-33 Format for transmitting consecutive TC9012 codes (C0 = 1) 14-59
Figure 14-34 Format for transmitting consecutiveTC9012 codes (C0 = 0) 14-59
Figure 14-35 Frame format for transmitting a single SONY code 14-59
Figure 14-36 Frame format for continuously transmitting SONY codes by pressing the key 14-60
Figure 14-37 Definitions of bit0 and bit1 of a SONY code 14-60
Figure 14-38 Process of initializing the IR module 14-61
Figure 14-39 Process of reading the decoded data 14-62
Figure 14-40 Logic block diagram of the USB 2.0 host controller 14-89
Figure 14-41 Reference design of the USB 2.0 host controller 14-90
Figure 14-42 Functional block diagram of the MMC controller 14-97
Figure 14-43 Typical application circuit of the MMC controller 14-98
Figure 14-44 Format of an MMC command 14-99
Figure 14-45 Format of the response to an MMC command 14-100
Figure 14-46 Operations by running an MMC non-data transfer command 14-100
Figure 14-47 Single-block and multi-block read operations 14-101
Figure 14-48 Single-block and multi-block write operations 14-102
Figure 14-49 Data transfer format in 1-bit mode 14-103
Figure 14-50 Data transfer format in 4-bit mode 14-103
Figure 14-51 Output timing 14-104
Figure 14-52 Input timing 14-104
Figure 14-53 Structure of the dual-buffer descriptor 14-112
Figure 14-54 Structure of the linked descriptor 14-112
Figure 14-55 Internal structure of 32-bit descriptors 14-112
Figure 14-56 Typical application mode 1 14-144
Figure 14-57 Typical application mode 2 14-145
Figure 14-58 Typical application mode 3 14-145
Figure 14-59 Architecture of the Hi3521 SATA module 14-146

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Figure 14-60 Structure of the linked list 14-186

Figure 14-61 Structures of the command list and data list 14-187

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Tables

Table 14-1 Summary of I²C registers 14-4
Table 14-2 Timing parameters of the SPI 14-18
Table 14-3 Summary of SPI registers (base address of SPI: 0x200C_0000) 14-23
Table 14-4 Summary of UART registers 14-38
Table 14-5 Code formats of the received infrared data (NEC with simple repeat code) 14-53
Table 14-6 Code formats of the received infrared data (NEC with full repeat code) 14-53
Table 14-7 Code formats of the received infrared data (TC9012 code and SONY code) 14-54
Table 14-8 Summary of IR registers (base address: 0x2007_0000) 14-63
Table 14-9 Base addresses of 15 groups of GPIO registers 14-82
Table 14-10 Summary of GPIO registers 14-83
Table 14-11 Summary of USB registers (base address: 0x100B_0000) 14-93
Table 14-12 Load parameters of signal lines 14-99
Table 14-13 Timing parameters of the MMC interface 14-103
Table 14-14 Default values of MMC_CMD when a non-data transfer command is executed 14-107
Table 14-15 Default values of MMC_CMD when a single data block or multiple data blocks are read 14-109
Table 14-16 Default values of MMC_CMD when a single data block or multiple data blocks are written 14-110
Table 14-17 Definition of each bit of DES0 14-113
Table 14-18 Definition of each bit of DES1 14-113
Table 14-19 Definition of each bit of DES2 14-114
Table 14-20 Definition of each bit of DES3 14-114
Table 14-21 Reference configuration of MMC_CMDARG when the resume operation is performed 14-117
Table 14-22 Summary of MMC registers (base address: 0x1002_0000) 14-118
Table 14-23 Signals of the SATA interface 14-143
Table 14-24 Summary of the SATA registers (base address: 0x1008_0000) 14-149
Table 14-25 Summary of the SATA_PORT_CFG registers (base address: 0x1008_0100) 14-150

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14 Peripherals

14.1 I²C Controller

14.1.1 Overview

The inter-integrated circuit (I^2C) module serves as the slave device on the advanced peripheral bus (APB) or the master device on the I^2C bus. The I^2C module is used to read/write data from/to the slave device on the I^2C bus through the CPU. When writing data to and reading data from the slave device, the CPU configures the I^2C configuration register over APB bus and transmits the control information and the data to be used to the I^2C data communication register. After parsing the commands, the I^2C module transmits the data of the data channel register to the slave device over I^2C bus and notifies the CPU of the final status to the CPU by using interrupts after transmitting the data. The CPU reads data from the slave device in the similar way.

14.1.2 Function Description

The I^2C module has the following features:

- Provides the master I^2C interface. The working reference clock of the I^2C module is the APB clock.
- Serves as the slave device on the APB bus or the master device on the I^2C bus, and supports the bus arbitration in the case of multiple master devices.
- Supports clock synchronization and bit and byte waiting.
- Supports interrupts or polling.
- Supports 7-bit standard address and 10-bit extended address.
- Supports standard mode (100 kbit/s) and high-speed mode (400 kbit/s).
- Supports general call and start byte.
- Incompatible with the CBUS component on the I^2C bus.
- Filters the received serial data (SDA) and serial clock (SCL) signals.

14.1.3 Operating Mode

14.1.3.1 Process of Transmitting Data Through the I²C Master

The I^2C master can write data to the slave or receive data from the slave. Figure 14-1 shows how the I^2C master transmits data.

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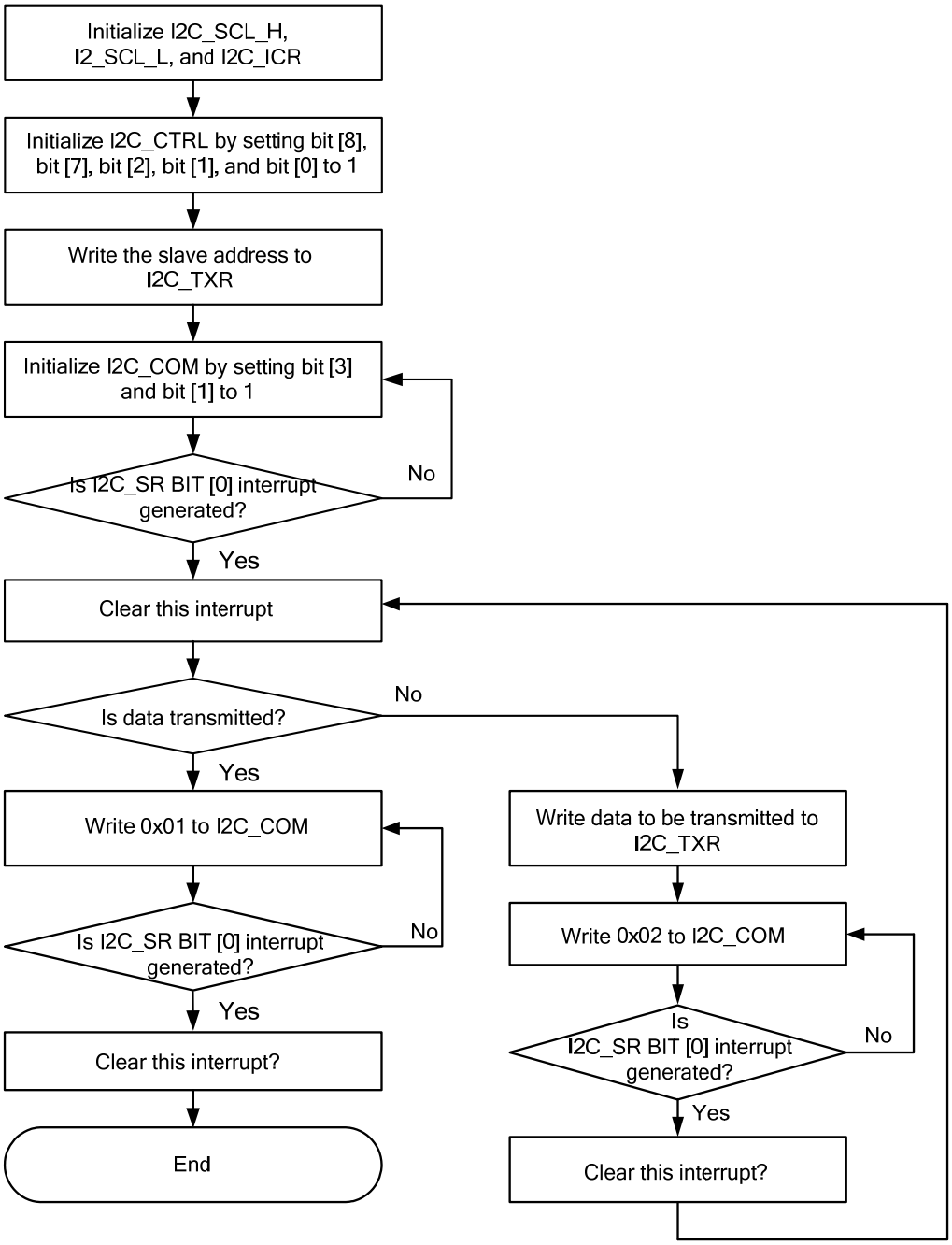
Figure 14-1 Process of transmitting data through the I²C master



14.1.3.2 Process of Receiving Data Through the I²C Master

Figure 14-2 shows how the I²C master receives data.

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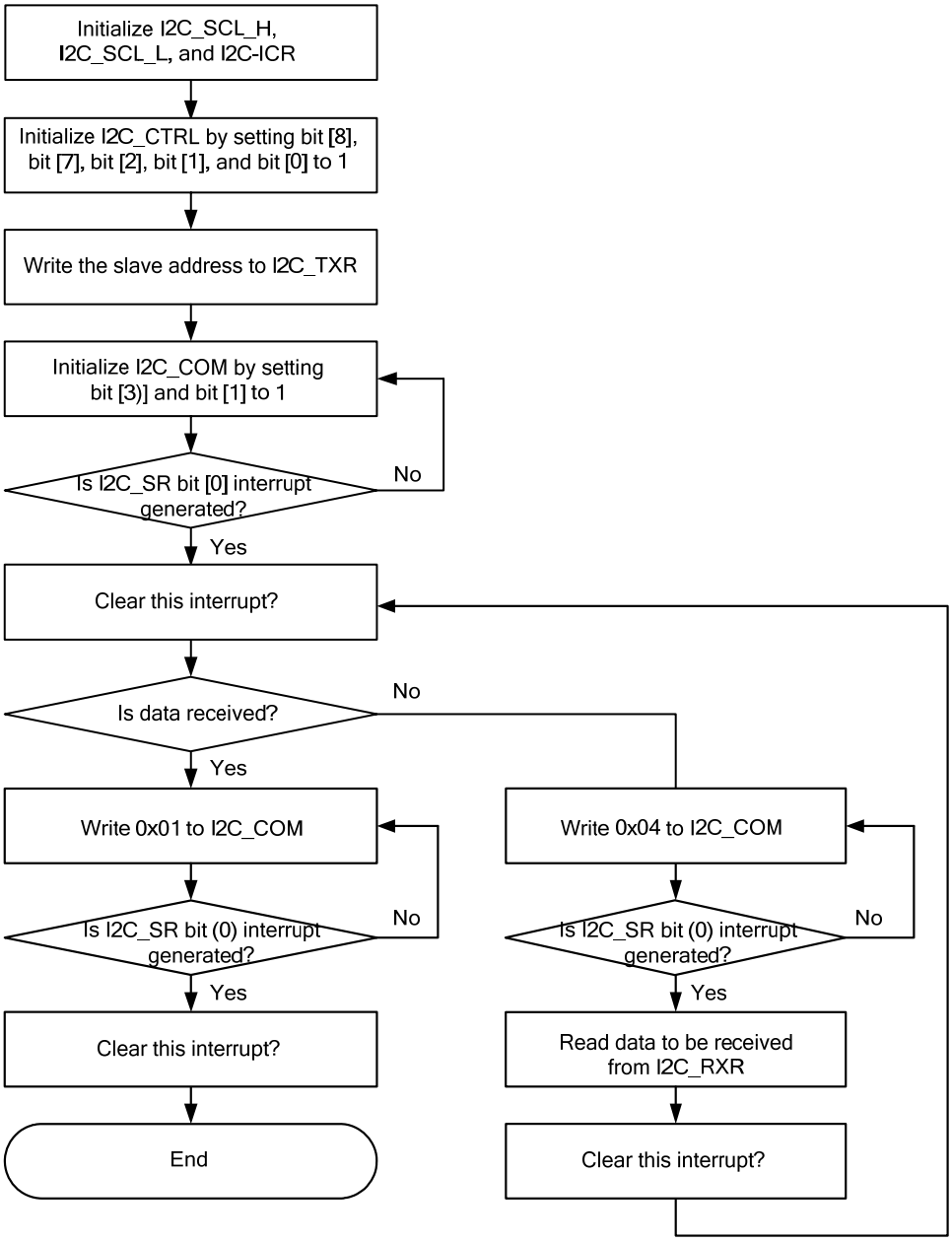
Figure 14-2 Process of receiving data through the I²C master



14.1.4 Register Summary

The Hi3521 contains an I²C module and the base address of I²C registers is 0x200D_0000.

Table 14-1 describes the I²C registers.

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Table 14-1 Summary of I²C registers

Address	Register	Type	Description	Page
0x00	I2C_CTRL	RW	I²C control register	14-4
0x04	I2C_COM	RW	I²C command register	14-5
0x08	I2C_ICR	RW	I²C interrupt clear register	14-6
0x0C	I2C_SR	RO	I²C status register	14-7
0x10	I2C_SCL_H	RW	I²C SCL high-level cycle number register	14-8
0x14	I2C_SCL_L	RW	I²C SCL low-level cycle number register	14-9
0x18	I2C_TXR	RW	I²C transmit data register	14-10
0x1C	I2C_RXR	RO	I²C receive data register	14-11

14.1.5 Register Description

I2C_CTRL

I2C_CTRL is an I²C control register. It is used to enable the I²C module and mask interrupts.

Offset Address	Register Name	Total Reset Value
0x00	I2C_CTRL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9	8	7	6	5	4	3	2	1	0
Name	reserved						i2c_en	int_mask	int_start_mask	int_stop_mask	int_tx_mask	int_rx_mask	int_ack_err_mask	int_arb_loss_mask	int_done_mask
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved.
[8]	RW	i2c_en	I²C enable. 0: disabled 1: enabled
[7]	RW	int_mask	Global I²C interrupt mask. 0: masked 1: not masked.

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[6]	RW	int_start_mask	Master start condition transmit end interrupt mask. 0: masked 1: not masked.
[5]	RW	int_stop_mask	Master stop condition transmit end interrupt mask. 0: masked 1: not masked.
[4]	RW	int_tx_mask	Master transmit interrupt mask. 0: masked 1: not masked.
[3]	RW	int_rx_mask	Master receive interrupt mask. 0: masked 1: not masked.
[2]	RW	int_ack_err_mask	Slave ACK error interrupt mask. 0: masked 1: not masked.
[1]	RW	int_arb_loss_mask	Bus arbitration failure interrupt mask. 0: masked 1: not masked.
[0]	RW	int_done_mask	Bus transfer done interrupt mask. 0: masked 1: not masked.

I2C_COM

I2C_COM is an I^2C command register. It is used to configure the commands for the I^2C module.

CAUTION

During or before the configuration of system initialization, the corresponding interrupts must be cleared. I2C_COM bit[3:0] are automatically cleared after the initialization.

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Offset Address	Register Name	Total Reset Value
0x04	I2C_COM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											op_ack	op_start	op_rd	op_we	op_stop
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	-	reserved	Reserved.
[4]	RW	op_ack	Indicates whether to send an ACK when the master serves as the receiver. 0: yes 1: no
[3]	RW	op_start	Start condition operation. 0: The operation is complete. 1: The operation is valid.
[2]	RW	op_rd	Read operation. 0: The operation is complete. 1: The operation is valid.
[1]	RW	op_we	Write operation. 0: The operation is complete. 1: The operation is valid.
[0]	RW	op_stop	Stop condition operation. 0: The operation is complete. 1: The operation is valid.

I2C_ICR

I2C_ICR is an I^2C interrupt clear register.

CAUTION

When a new interrupt is generated, the I^2C module automatically clears certain bits of I2C_ICR.

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Offset Address	Register Name	Total Reset Value
0x08	I2C_ICR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									clr_int_start	clr_int_stop	clr_int_tx	clr_int_rx	clr_int_ack_err	clr_int_arb_loss	clr_int_done
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	-	reserved	Reserved.
[6]	WC	clr_int_start	Master start condition transmit end interrupt clear. 0: not cleared 1: cleared
[5]	WC	clr_int_stop	Master stop condition transmit end interrupt clear. 0: not cleared 1: cleared
[4]	WC	clr_int_tx	Master transmit interrupt clear. 0: not cleared 1: cleared
[3]	WC	clr_int_rx	Master receive interrupt clear. 0: not cleared 1: cleared
[2]	WC	clr_int_ack_err	Slave ACK error interrupt clear. 0: not cleared 1: cleared
[1]	WC	clr_int_arb_loss	Bus arbitration failure interrupt clear. 0: not cleared 1: cleared
[0]	WC	clr_int_done	Bus transfer done interrupt clear. 0: not cleared 1: cleared

I2C_SR

I2C_SR is an I^2C status register. It is used to read the operating status of the I^2C module.

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CAUTION

I2C_SR bit[1] indicates an I^2C bus arbitration failure. When I2C_SR bit[1] is valid, the current operation fails. Before clearing I2C_SR bit[1], you need to clear other interrupts and clear I2C_COM or write a new command to I2C_COM in sequence.

Offset Address	Register Name	Total Reset Value
0x0C	I2C_SR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								bus_busy	int_start	int_stop	int_tx	int_rx	int_ack_err	int_arb_loss	int_done
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7]	RO	bus_busy	Bus busy. 0: idle 1: busy
[6]	RO	int_start	Master start condition transmit end interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	int_stop	Master stop condition transmit end interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	int_tx	Master transmit interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	int_rx	Master receive interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	int_ack_err	Slave ACK error interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	int_arb_loss	Bus arbitration failure interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

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[0]	RO	int_done	Bus transfer done interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

I2C_SCL_H

I2C_SCL_H is an I^{2}C SCL high-level cycle number register. It is used to configure the number of SCL high-level cycles of the working I^{2}C module.

CAUTION

During or before the configuration of system initialization, you must set I2C_CTRL bit[7] to 0.

Offset Address	Register Name	Total Reset Value
0x10	I2C_SCL_H	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																scl_h															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	scl_h	SCL high-level time.

Assume that the frequency of the reference clock is 108 MHz, I2C_SCL_H is set to *m*, and the SCL high-level period is DelTim. DelTim is calculated as follows:

Deltim = 1/108 x (m + 1) x 2, (in the unit of μs)

If the required SCL high-level period is 5 μs, the value m of I2C_SCL_H is:

m = (5 x 108)/2 – 1 = 269

If the frequency of the reference clock is 108 MHz, the maximum SCL high-level period is 606 μs.

I2C_SCL_L

I2C_SCL_L is an I^{2}C SCL low-level cycle number register. It is used to configure the number of SCL low-level cycles when the I^{2}C module works.

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CAUTION

During or before the configuration of system initialization, you must set I2C_CTRL bit[7] to 0.

Offset Address	Register Name	Total Reset Value
0x14	I2C_SCL_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																scl_l															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	scl_l	SCL low-level time.

Assume that the frequency of the reference clock is 108 MHz, I2C_SCL_L is set to m, and the SCL low-level period is DelTim. DelTim is calculated as follows:

Deltim = 1/108 x (m + 1) x 2, (in the unit of μs)

If the required SCL low-level period is 5 μs, the value m of I2C_SCL_L is:

m = (5 x 108)/2 – 1 = 269

If the frequency of the reference clock is 108 MHz and the maximum SCL low-level period is 606 μs.

I2C_TXR

I2C_TXR is an I^2C transmit data register. It is used to enable the I^2C module to transmit data.

CAUTION

When data is transmitted completely, the I^2C module does not modify I2C_TXR.

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Offset Address	Register Name	Total Reset Value
0x18	I2C_TXR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								i2c_txr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	RW	i2c_txr	Data is transmitted by the master

I2C_RXR

I2C_RXR is an I^2C receive data register. It is used to enable the master to receive the data from the slave.

CAUTION

When I2C_SR bit[3] is 1, the I2C_RXR data is valid. The data is remained until the next start operation starts.

Offset Address	Register Name	Total Reset Value
0x1C	I2C_RXR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								i2c_rxr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	RO	i2c_rxr	Data is received by the master.

14.2 SPI

14.2.1 Overview

The serial peripheral interface (SPI) controller implements serial-to-parallel conversion and parallel-to-serial conversion, and serves as a master to communicate with peripherals in

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synchronous and serial modes. The SPI controller supports three types of peripheral interfaces including the SPI, TI synchronous serial interface, and MicroWire interface.

14.2.2 Features

CAUTION

The Hi3521has one serial peripheral interface (SPI) that supports eight chip selects (CSs).

The Hi3521 SPI is a master interface by default and CS0 can be set to the slave interface. The working reference clock is the APB bus clock. SPI_CLK output by the SPI supports the maximum working frequency of 40 MHz.

The SPI controller has the following features:

- Supports programmable frequency of the interface clock.
- Supports two separate FIFOs. One acts as a receive FIFO and the other one acts as a transmit FIFO. Each of them is 16-bit wide and 256-location deep.
- Supports programmable serial data frame length: 4 bits to 16 bits.
- Provides internal loopback test mode.
- Supports the direct memory access (DMA) operation.
- Supports three types of peripheral interfaces including the SPI, MicroWire interface, and TI synchronous serial interface.
- Supports SPI in full-duplex mode and configurable clock polarity and phase.
- Supports MicroWire in half-duplex mode.
- Supports TI synchronous serial interface in full-duplex mode.

14.2.3 Function Description

14.2.3.1 Typical Application

Figure 14-3 shows the application block diagram when the SPI is connected to a single slave device. The default chip select pin SPI_CSN0 is used.

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Figure 14-3 Application block diagram when the SPI is connected to a single slave device

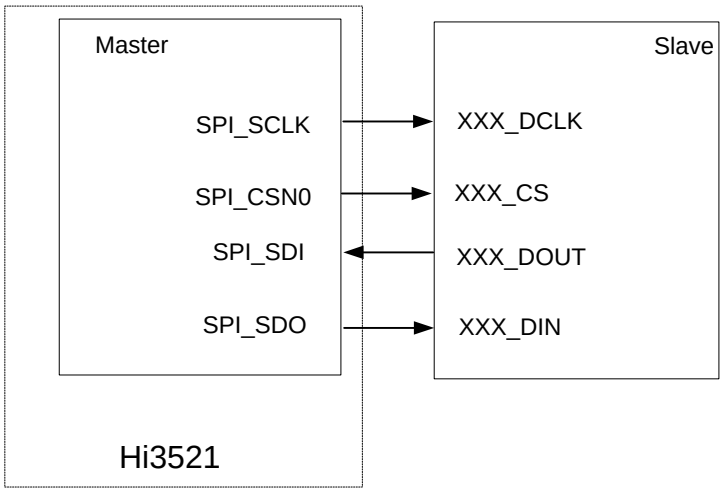
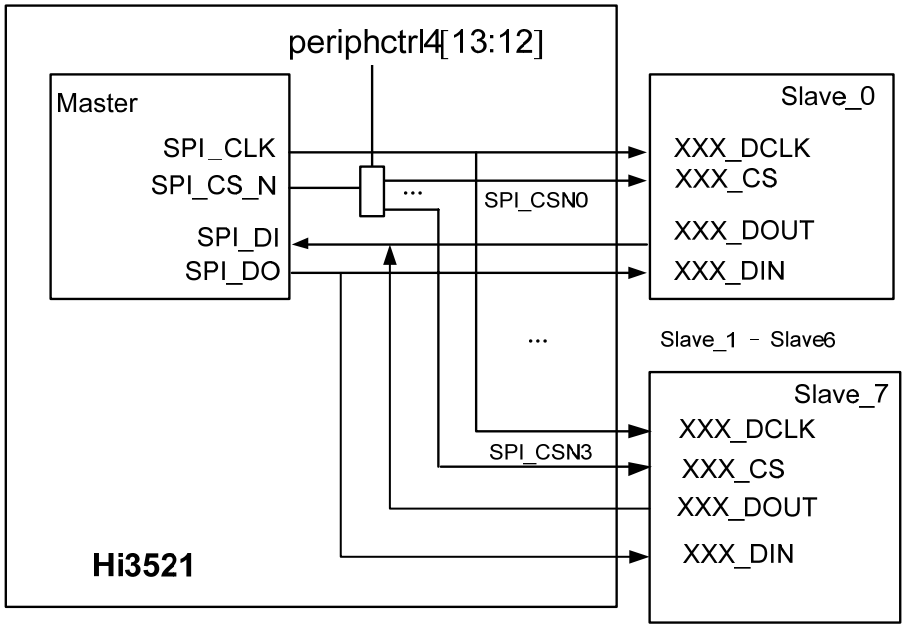


Figure 14-4 shows the application block diagram when the SPI is connected to multiple slave devices.

Figure 14-4 Application block diagram when the SPI is connected to multiple slave devices



For details about how to select SPI CS, see periphctrl4 bit[13:12] register in section 3.4 "System Controller."

The daisy chain mode is supported when the SPI acts as a configuration interface. For details, see the *Hi3521 H.264 Codec Processor Data Sheet*

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14.2.3.2 Peripheral Bus Timings

The meanings of the abbreviations and acronyms in Figure 14-5 to Figure 14-12 are as follows:

- MSB: most significant bit
- LSB: least significant bit
- Q: Q is an undefined signal

14.2.3.3 SPI

NOTE

SPO indicates the polarity of SPICLKOUT and SPH indicates the phase of SPICLKOUT. They correspond to SPICR0 bit[7:6].

(1) SPO = 0, SPH = 0

Figure 14-5 shows the SPI single frame format.

Figure 14-5 SPI single frame format (SPO = 0, SPH = 0)

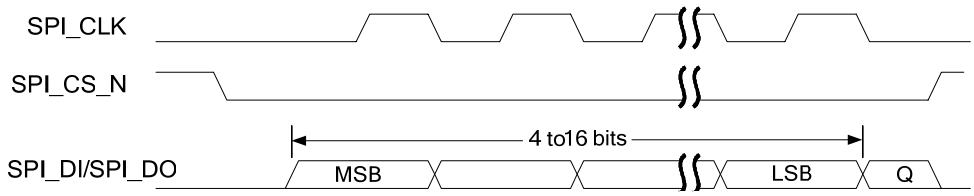
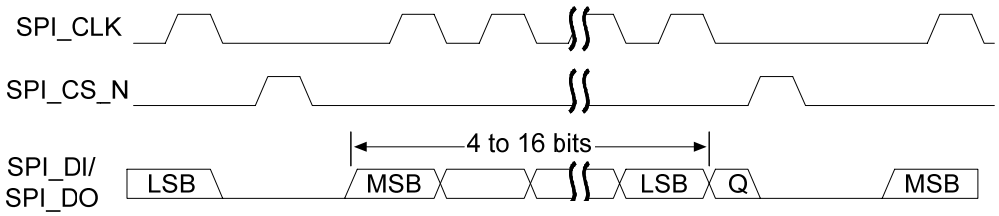


Figure 14-6 shows the SPI continuous frame format.SPI continuous frame format (SPO = 0, SPH = 0)



When the SPI is idle in this mode:

- The SPI_CLK signal is set to low.
- The SPI_CS_N signal is set to high.
- The transmit data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the transmit FIFO, data transfer starts if the SPI_CS_N signal is set to low. The data from the slave device is transferred to the receive data line SIP_DI of the master device immediately. Half SPI_CLK clock cycle later, the valid master data is transmitted to SPI_DO. At this time, both the master and slave data become valid. The SPI_CLK pin changes to high level in the next half SPI_CLK clock cycle. Then, data is captured on the rising edge and is transmitted on the falling edge of the SPI_CLK clock.

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If a single word is transferred, SPI_CS_N is restored to high level one SPI_CLK clock later after the last bit is captured.

For continuous transfer, the SPI_CS_N signal must pull up the SPI_CLK clock by one clock cycle between the transfers of two words. When SPH is 0, the slave select pin fixes the data of the internal serial device register. Therefore, the master device must pull up the SPI_CS_N signal between the transfers of two words in continuous transfer. When the continuous transfer ends, SPI_CS_N is restored to high level one SPI_CLK clock cycle later after the last bit is captured.

(2) SPO = 0, SPH = 1

Figure 14-7 shows the SPI single frame format.

Figure 14-7 SPI single frame format (SPO = 0, SPH = 1)

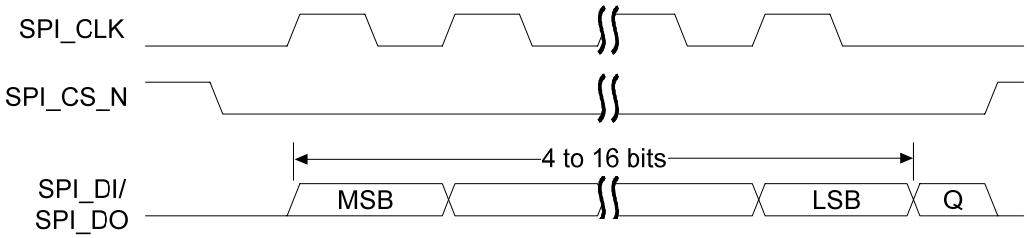
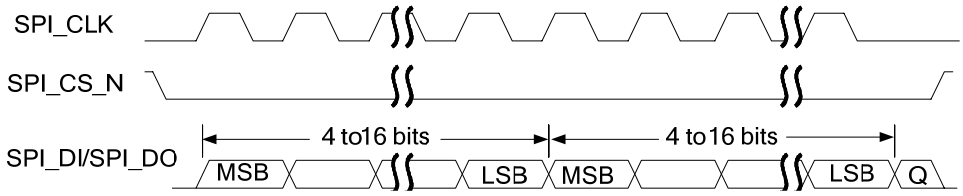


Figure 14-8 shows the SPI continuous frame format.

Figure 14-8 SPI continuous frame format (SPO = 0, SPH = 1)



When the SPI is idle in this mode:

- The SPI_CLK signal is set to low.
- The SPI_CS_N signal is set to high.
- The transmit data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the transmit FIFO, data transfer start if the SPI_CS_N signal is set to low. The master and slave data become valid on their respective transfer line half SPI_CLK clock cycle later. Meanwhile, SPI_CLK becomes valid from the first rising edge. Then, data is captured on the falling edge and is transmitted on the rising edge of the SPI_CLK clock.

If a single word is transferred, SPI_CS_N is restored to high level one SPI_CLK clock later after the last bit is captured.

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For a continuous transfer, SPI_CS_N remains low between the transfers of two words. When the continuous transfer ends, SPI_CS_N is restored to high level one SPI_CLK clock cycle later after the last bit is captured.

(3) SPO = 1, SPH = 0

Figure 14-9 shows the SPI single frame format.

Figure 14-9 SPI single frame format (SPO = 1, SPH = 0)

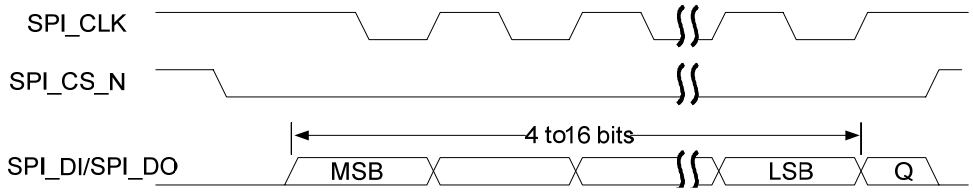
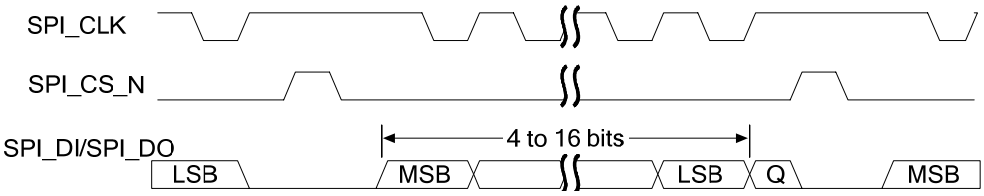


Figure 14-10 shows the SPI continuous frame format.

Figure 14-10 SPI continuous frame format (SPO = 1, SPH = 0)



When the SPI is idle in this mode:

- The SPI_CLK signal is set to high.
- The SPI_CS_N signal is set to high.
- The transmit data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the transmit FIFO, data transfer starts if the SPI_CS_N signal is set to low. The data from the slave device is transferred to the receive data line SPI_DI of the master device immediately. Half SPI_CLK clock cycle later, the valid master data is transmitted to SPI_DO. After another half SPI_CLK clock cycle, the SPI_CLK master pin is set to low. Then, data is captured on the falling edge and is transmitted on the rising edge of the SPI_CLK clock.

If a single word is transferred, SPI_CS_N is restored to high level after one SPI_CLK clock since the data of the last bit is captured.

For a continuous transfer, the SPI_CS_N signal must be pulled up between the transfers of two words. This is because that when SPH is 0, the slave select pin fixes the data of the internal serial device register. SPI_CS_N is restored to high level one SPI_CLK clock later after the last bit is captured.

(4) SPO = 1, SPH = 1

Figure 14-11 shows the SPI single frame format.

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Figure 14-11 SPI single frame format (SPO = 1, SPH = 1)

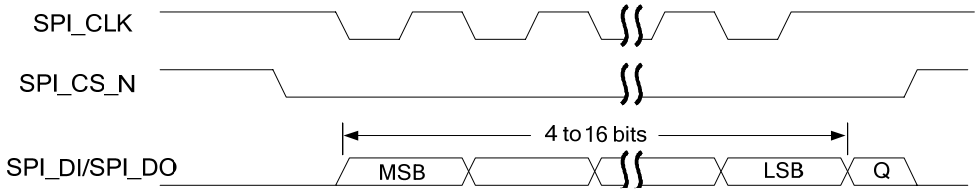
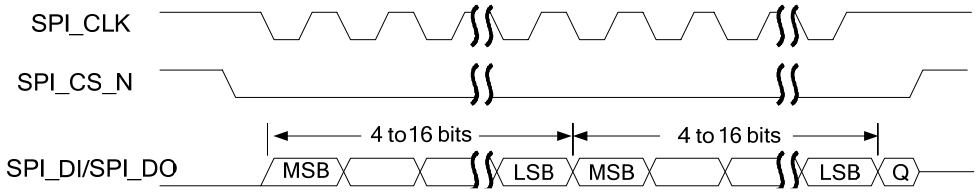


Figure 14-12 shows the SPI continuous frame format.

Figure 14-12 SPI continuous frame format (SPO = 1, SPH = 1)



When the SPI is idle in this mode:

- The SPI_CLK signal is set to high.
- The SPI_CS_N signal is set to high.
- The transmit data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the transmit FIFO, data transfer starts if the SPI_CS_N signal is set to low. Half SPI_CLK clock cycle later, the master data and slave data are valid on respective transfer line. Meanwhile, SPI_CLK becomes valid from a falling edge of SPI_CLK. Then, data is captured on the rising edge and is transmitted on the falling edge of the SPI_CLK clock. If a single word is being transmitted, SPI_CS_N is restored to high level one SPI_CLK clock cycle later after the last bit is captured.

For a continuous transfer, the SPI_CS_N signal remains low. SPI_CS_N is restored to high level one SPI_CLK clock cycle after the last bit is captured. For a continuous transfer, SPI_CS_N remains low during transfer. The method of ending data transfer is the same as that in single transfer mode.

(5) Interface timings

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Figure 14-13 SPI timings

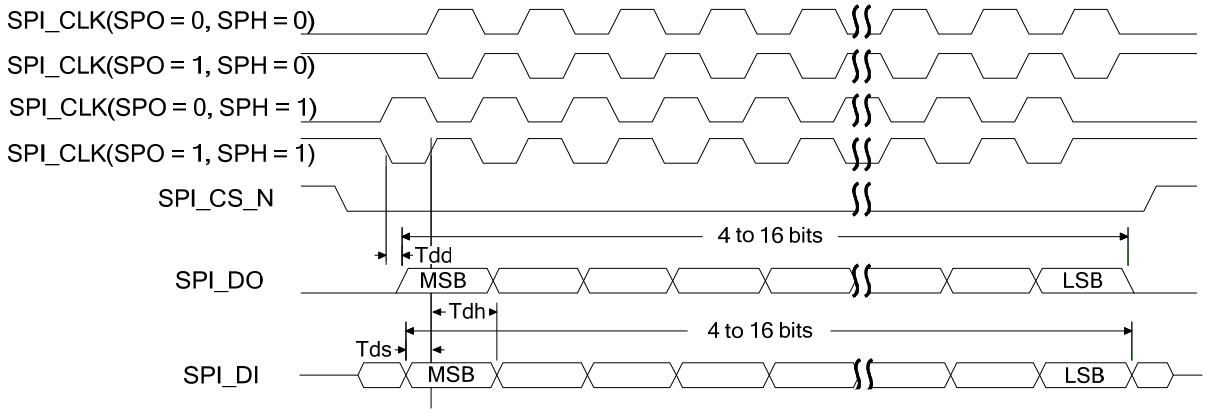

Table 14-2 Timing parameters of the SPI

Parameter	Description	Min	Max	Unit
Tdd	Output data delay	－3.5	5	ns
Tds	Input control signal setup time	23	None	ns
Tdh	Input control signal hold time	0	None	ns

TI Synchronous Serial Interface

Figure 14-14 shows the TI synchronous serial single frame format.

Figure 14-14 TI synchronous serial single frame format

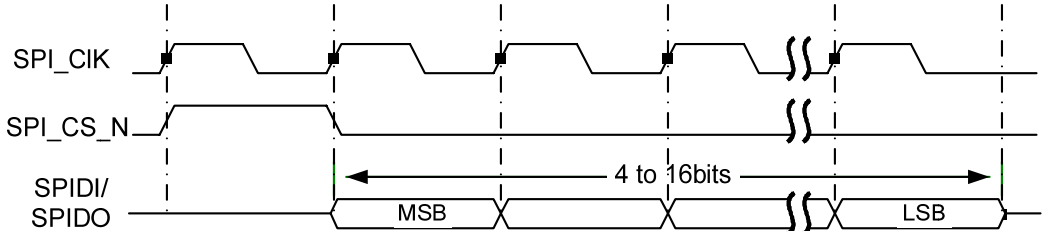

Figure 14-15 shows the TI synchronous serial continuous frame format.

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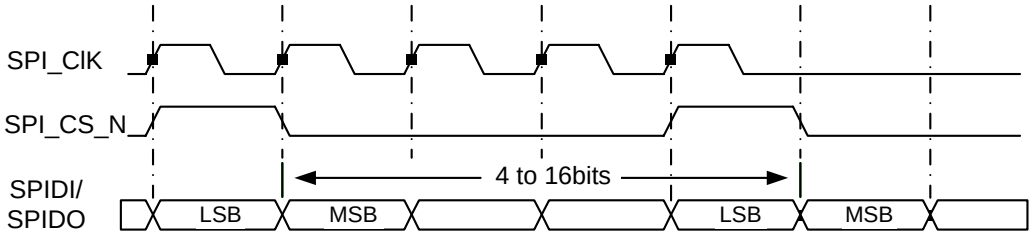
Figure 14-15 TI synchronous serial continuous frame format



When the SPI is idle in this mode:

- The SPI_CK signal is set to low.
- The SPI_CS_N signal is set to low.
- The transfer data line SPI_DO retains high impedance.

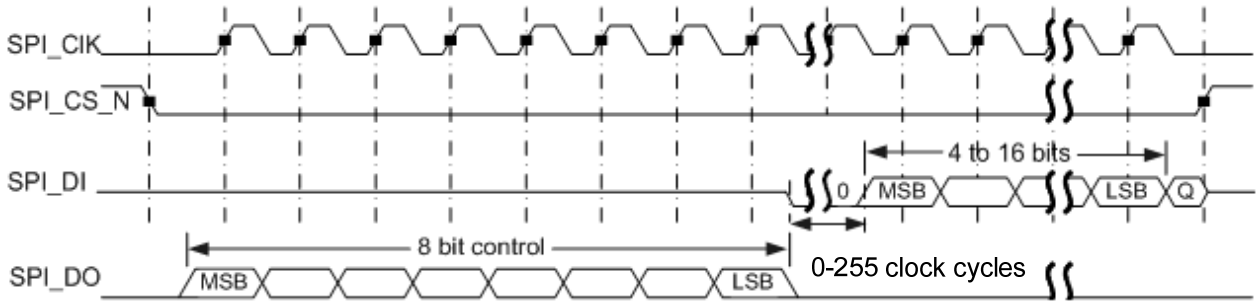
If there is data in the transmit FIFO, SPI_CS_N generates a high-level pulse in one SPI_CK clock cycle. Then, the data to be transmitted is transferred from the transmit FIFO to the transmit logic serial shift register. In addition, the MSBs of the data frames with the length of 4–16 bits are shifted and output from SPI_DO on the next rising edge of the SPI_CK clock. Similarly, the MSB of the data received from the external serial slave device is shifted and input from the SPI_DI pin.

The SPI and off-chip serial device stores the data in the serial shift register on the falling edge of the SPI_CK clock. The receive serial register transmits the data to the receive FIFO on the rising edge of the first SPI_CK clock after receiving the LSB.

National Semiconductor Microwire Interface

Figure 14-16 shows the national semiconductor microwire single frame format.

Figure 14-16 National semiconductor microwire single frame format



0 to 255 clock cycles can be delayed between the end of SPI_DO LSB and the start of SPI_DI MSB.

Figure 14-17 shows the national semiconductor microwire continuous frame format.

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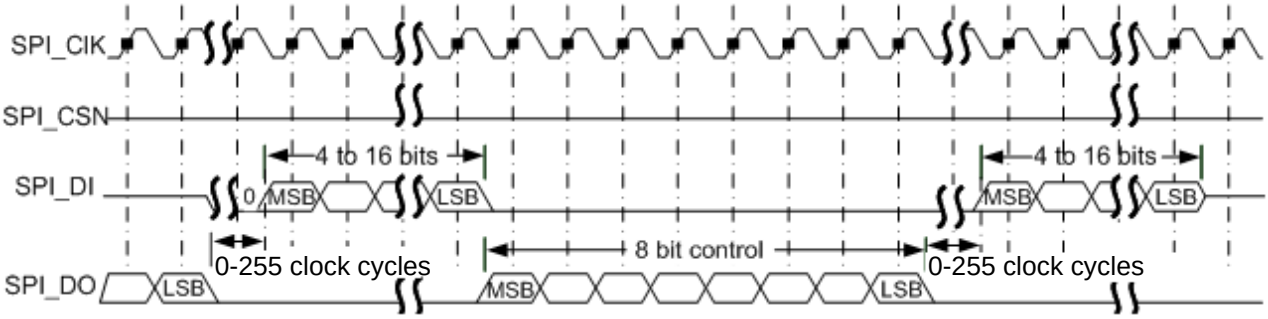
Figure 14-17 National semiconductor microwire continuous frame format



0 to 255 clock cycles can be delayed between the end of SPI_DO LSB and the start of SPI_DI MSB.

The microwire format is similar to the SPI format because both of them use the technology of transferring master-slave information. The only difference is that the SPI works in full-duplex mode and the microwire interface works in half-duplex mode. Before the SPI transmits serial data to the external chip, an 8-bit control word needs to be added. In this process, the SPI does not receive any data. After data transfer is complete, the external chip decodes the received data. One clock cycle later after 8-bit control information is transmitted, the slave device starts to respond to the required data. The returned data length is 4 bits to 16 bits, and the length of the entire frame is 13 bits to 25 bits.

When the SPI is idle in this mode:

- The SPI_CLK signal is set to low.
- The SPI_CS_N signal is set to high level.
- The transmit data signal SPI_DO is forced to low level.

Writing one control byte to the transmit FIFO starts a data transfer. The data transfer is triggered on a falling edge of SPI_CS_N. The data of the transmit FIFO is sent to the serial shift register. The MSB of the 8-bit control frame is transmitted to the SPI_DO pin. During frame transfer, SPI_CS_N remains low. Whereas SPI_DI retains high impedance.

The off-chip serial slave device latches the data to the serial shift register on each rising edge of the SPI_CLK clock. After the slave device latches the data of the last bit, the slave device starts to decode the received data in the next clock cycle. Then, the slave device provides the data required by the SPI. Each bit is written to SPI_DI on the falling edge of the SPI_CK clock. For a single data transfer, SPI_CS_N is pulled up at the end of the frame one clock cycle after the last bit is written to the receive serial register. In this way, the received data is transmitted to the receive FIFO.

The start and end for a continuous data transfer are the same as those for a signal data transfer. During the continuous data transfer, SPI_CS_N retains low and the data transferred is continuous. The control word of the next frame is adjacent to the LSB of the previous frame. When the LSB of the frame is latched to the SPI, each received value is originated from the receive shift register on the falling edge of the SPI_CLK clock.

14.2.4 Operating Mode

Working Modes

The SPI working modes include the data transmission in the interrupt or query mode and the data transmission in the DMA mode.

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Clock and Reset

The frequency of the output SPI clock is calculated as follows:

Fsspclkout = Fsspclk/[CPSDVR x (1 + SCR)]

Fsspclk is the working reference clock of the SPI and its value is 1/2 of the bus clock.

For details about CPSDVR and SCR, query the corresponding registers.

The SPI of the Hi3521 supports separate soft reset, which is controlled by using the PERI_CRG57 bit[12] register. Writing 0 to the corresponding bit stops soft reset and writing 1 to the corresponding bit starts soft reset. The default value is 0 after power on.

Interrupts

The SPI has five interrupts. Four of them have separate interrupts sources and maskable and active high.

- SPIRXINTR

  Receive FIFO interrupt request. When there are four or more valid data segments in the receive FIFO, the interrupt is set to 1.
- SPITXINTR

  Transmit FIFO interrupt request. When there are four or less valid data segments in the transmit FIFO, the interrupt is set to 1.
- SPIRORINTR

  Receive overrun interrupt request. When the FIFO is full and new data is written to the FIFO, the FIFO is overrun and the interrupt is set to 1. In this case, the data is written to the receive shift register rather than the FIFO.
- SPIRTINTR

  Receive timeout interrupt request. When the receive FIFO is not empty and the SPI is idle for more than a fixed 32-bit cycle, the interrupt is set to 1.

  It indicates that data in the receive FIFO needs to be transmitted. When the receive FIFO is empty or new data is transmitted to SPIRXD, the interrupt is cleared. The interrupt can also be cleared by writing to the SPIICR[RTIC] register.
- SPIINTR

  Combined interrupt. This interrupt is obtained by performing an OR operation on the preceding four interrupts. If any of the preceding four interrupts is set to 1 and enabled, SPIINTR is set to 1.

For details about how to connect the SPIINTR of SPI, see "Interrupts" in this section.

Initialization

The initialization is implemented as follows:

Step 1 Write 0 to SPICR1[sse] to disable the SPI.

Step 2 Write to SPICR0 to set the parameters such as the frame format and transfer data bit width.

Step 3 Configure SPICPSR to set the required clock divider.

Step 4 In the interrupt mode, configure SPIIMSC to enable the corresponding interrupts or disable the generation of corresponding interrupts in query or DMA mode.

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Step 5 Configure SPITXFIFOCR and SPIRXFIFOCR in interrupt or DMA mode.

Step 6 Configure SPIDMACR to enable the DMA function of the SPI in DMA mode.

---End

Data Transfer in Query Mode

The full status of the transmit or receive FIFO is not considered, because the depth of the transmit FIFO or receive FIFO is 512.

Perform the following steps:

Step 1 If multiple CSs are used, select the current CS by configuring the system control register periphctrl4 [14:12].

Step 2 Write 1 to SPICR1[sse] to enable the SPI.

Step 3 Write the data to be transmitted to SPIDR continuously.

Step 4 Poll SPISR until SPISR[BSY] is 0, SPISR[TFE] is 1, and SPISR[RNE] is 1. If SPISR[BSY] is 0, the bus is busy; if SPISR[TFE] is 1, the transmit FIFO is empty; if SPISR[RNE] is 1, the receive FIFO is not empty.

Step 5 Read data until the receive FIFO is empty. You can check whether the receive FIFO is empty by querying SPISR[RNE]

CAUTION

The SPI/Microwire has full-duplex features. That is, a data segment is received after a data segment is transmitted. Even if only data is transmitted, the receive FIFO must be cleared.

Step 6 Write 0 to SPICR1[sse] to disable the SPI.

---End

Data Transfer in Interrupt Mode

Perform the following steps:

Step 1 If multiple CSs are used, select the current CS to configure the system control register periphctrl4 [14:12].

Step 2 Write 1 to SPICR1 [sse] to disable the SPI.

Step 3 Write the data to be transmitted to SPIDR continuously.

Step 4 Wait for the interrupt SPIRXINTR and read data in cyclic mode until all data is read.

Note that the full-duplex features of the SPI/Microwire. That is, a data segment is received after a data segment is transmitted. Even if only data is transmitted, the receive FIFO must be cleared.

Step 5 Write 0 to SPICR1 [sse] to disable the SPI.

---End

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Data Transfer in DMA Mode

Perform the following steps:

Step 1 Obtain a DMAC channel.

Step 2 If two CSs are used, select the current CS to configure the system control register PERIPHCTRL4 [14:12].

Step 3 Write 1 to SPICR1 [sse] to disable the SPI.

Step 4 Transmit data.

1. Configure the parameters of the configuration register and control register related to the DMAC channel.
2. Start the DMAC and respond to the DMA request of the SPI transmit FIFO for the data transfer.
3. Check whether all data is transmitted by viewing the DMA interrupt. If all data is transmitted, disable the DMA transmit function of the SPI.

Step 5 Receive data

1. Configure the parameters of the configuration register and control register related to the DMAC channel.
2. Start the DMAC and respond to the DMA request of the SSP receive FIFO for the data transfer.
3. Check whether all data is received by viewing the DMA interrupt. If all data is received, disable the DMA receive function of the SPI.

Step 6 Write 0 to SPICR1 [sse] to disable the SPI.

---End

14.2.5 Register Summary

Table 14-3 describes the registers.

Table 14-3 Summary of SPI registers (base address of SPI: 0x200C_0000)

Offset Address	Register	Description	Page
0x000	SPICR0	Control register 0	14-24
0x004	SPICR1	Control register 1	14-25
0x008	SPIDR	Data register	14-26
0x00C	SPISR	Status register	14-26
0x010	SPICPSR	Clock divider register	14-27
0x014	SPIIMSC	Interrupt mask register	14-28
0x018	SPIRIS	Raw interrupt status register	14-29
0x01C	SPIMIS	Masked interrupt status register	14-29

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Offset Address	Register	Description	Page
0x020	SPIICR	Interrupt clear register	14-30
0x024	SPIDMACR	DMA control register	14-30
0x028	SPITXFIFOCR	Transmit FIFO control register	14-31
0x02C	SPIRXFIFOCR	Receive FIFO control register	14-32

14.2.6 Register Description

SPICR0

SPICR0 is SPI control register 0.

Offset Address	Register Name	Total Reset Value
0x000	SPICR0	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCR								SPH	SPO	FRF		DSS			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RW	SCR	Serial clock rate, ranging from 0 to 255. The value of the SCR is used to generate the transmit and receive bit rates of the SPI. The formula is as follows: FSPICLK/(CPSDVSR/(1 + SCR). CPSDVSR is an even ranging from 2 to 254, and it is configured by SPICPSR.
[7]	RW	SPH	SPICLKOUT phase. For details, see the "SPI frame format of Peripheral Bus Timings" in section 14.2.4.
[6]	RW	SPO	SPICLKOUT polarity. For details, see the "SPI Frame Format of Peripheral Bus Timings" in section 14.2.4.
[5:4]	RW	FRF	Frame format select. 00: Motorola SPI frame format 01: TI synchronous serial frame format 10: National microwire frame format 11: reserved

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[3:0]	RW	DSS	Data width. 0011: 4 bits 1000: 9 bits 1101: 14 bits 0100: 5 bits 1001: 10 bits 1110: 15 bits 0101: 6 bits 1010: 11 bits 1111: 16 bits 0110: 7 bits 1011: 12 bits 0111: 8 bits 1100: 13 bits Other values: reserved

SPICR1

SPICR1 is SPI control register 1.

Offset Address	Register Name	Total Reset Value
0x004	SPICR1	0x7F00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WaitEn	WaitVal							reserved			BigEnd	reserved	MS	SSE	LBM
Reset	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	WaitEn	Wait enable. This bit is valid when the SPICR0[FRF] is set to the national microwire frame format. 0: disabled 1: enabled
[14:8]	RW	WaitVal	Number of waiting beats between read and write when in the national microwire frame format. When WaitEn is 1 and the frame format is national microwire, WaitVal is valid.
[7:5]	RW	reserved	Reserved.

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[4]	RW	BigEnd	Data endian mode. 0: little endian 1: big endian
[3]	RW	reserved	Reserved.
[2]	RW	MS	Master or slave mode. This bit can be changed only when the SPI is disabled. 0: master mode (default value) 1: slave mode
[1]	RW	SSE	SPI enable. 0: disabled 1: enabled
[0]	RW	LBM	Loopback mode. 0: A normal serial port operation is enabled. 1: The output of the transmit serial shift register is connected to the input of the receive serial shift register.

SPIDR

SPIDR is a data register.

Offset Address	Register Name	Total Reset Value
0x008	SPIDR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	DATA	transmit or receive FIFO. Read: receive FIFO Write: transmit FIFO If the data is less than 16 bits, the data must be aligned to the right. The transmit logic ignores the unused upper bits, and the receive logic automatically aligns the data to the right.

SPISR

SPISR is a status register.

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Offset Address	Register Name	Total Reset Value
0x00C	SPISR	0x0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											BSY	RFF	RNE	TNF	TFE
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[15:5]	RW	reserved	Reserved.
[4]	RW	BSY	SPI busy flag. 0: idle 1: busy
[3]	RW	RFF	Whether the receive FIFO is full. 0: not full 1: full.
[2]	RW	RNE	Whether the receive FIFO is not empty. 0: empty 1: not empty
[1]	RW	TNF	Whether the transmit FIFO is not full. 0: full 1: not full
[0]	RW	TFE	Whether the transmit FIFO is empty. 0: not empty 1: empty

SPICPSR

SPICPSR is a clock divider register.

Offset Address	Register Name	Total Reset Value
0x010	SPICPSR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								CPSDVSR							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RW	reserved	Reserved.

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[7:0]	RW	CPSDVSR	Clock divider. The value must be an even ranging from 2 to 254. It depends on the frequency of the input clock SPICLK. The LSB is read as 0.

SPIIMSC

SCIIMSC is an interrupt mask register. The value 0 indicates an interrupt is masked and the value1 indicates an interrupt is not masked.

Offset Address	Register Name	Total Reset Value
0x014	SPIIMSC	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXIM	RXIM	RTIM	RORIM
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:4]	RW	reserved	Reserved.
[3]	RW	TXIM	Transmit FIFO interrupt mask. 0: The interrupt masked when only half of or less data is left in the transmit FIFO. 1: The interrupt not masked when only half of or less data is left the transmit FIFO.
[2]	RW	RXIM	Receive FIFO interrupt mask. 0: The interrupt is masked when only half of or less data is left in the receive FIFO. 1: The interrupt is not masked when only half of or less data is left in the receive FIFO.
[1]	RW	RTIM	Receive timeout interrupt mask. 0: masked 1: not masked
[0]	RW	RORIM	Receive overflow interrupt mask. 0: masked 1: not masked When the value is 1, the hardware stream control function is enabled. That is, when the receive FIFO is full, the SPI stops transmitting data.

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SPIRIS

SPIRIS is a raw interrupt status register. The value 0 indicates no interrupts are generated, and the value 1 indicates interrupts are generated.

Offset Address	Register Name	Total Reset Value
0x018	SPIRIS	0x0008

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXRIS	RXRIS	RTRIS	RORRIS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved.
[3]	RO	TXRIS	Raw transmit FIFO interrupt status.
[2]	RO	RXRIS	Raw receive FIFO interrupt status.
[1]	RO	RTRIS	Raw receive timeout interrupt status.
[0]	RO	RORRIS	Raw receive overflow interrupt status.

SPIMIS

SPIMIS is a masked interrupt status register. The value 0 indicates no interrupts are generated, and the value 1 indicates interrupts are generated.

Offset Address	Register Name	Total Reset Value
0x01C	SPIMIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXMIS	RXMIS	RTMIS	RORMIS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved.
[3]	RO	TXMIS	Status of the masked transmit FIFO interrupt.
[2]	RO	RXMIS	Status of the masked transmit FIFO interrupt.
[1]	RO	RTMIS	Status of the masked receive timeout interrupt.

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[0]	RO	RORMIS	Status of the masked receive overflow interrupt.

SPIICR

SCIICR is an interrupt clear register. Writing 1 clears an interrupt, and writing 0 has no effect.

Offset Address	Register Name	Total Reset Value
0x020	SPIICR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														RTIC	RORIC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:2]	RO	reserved	Reserved.
[1]	RO	RTIC	Receive timeout interrupt clear.
[0]	RO	RORIC	Receive overflow interrupt clear.

SPIDMACR

SCIDMACR is a DMA control register.

Offset Address	Register Name	Total Reset Value
0x024	SPIDMACR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														TXDMAE	RXDMAE
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:2]	WO	reserved	Reserved.
[1]	WO	TXDMAE	DMA transmit FIFO enable. 0: disabled 1: enabled

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[0]	WO	RXDMAE	DMA receive FIFO enable. 0: disabled 1: enabled

SPITXFIFOCR

SPITXFIFOCR is a transmit FIFO control register.

Offset Address	Register Name	Total Reset Value
0x028	SPITXFIFOCR	0x0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										TXINTSize			DMATXBRSize		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[15:6]	RW	reserved	Reserved.
[5:3]	RW	TXINTSize	Threshold for generating the transmit FIFO request interrupt. That is, when the number of data segments in the transmit FIFO is less than or equal to the value of TXINTSize, TXRIS is valid. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 64 111: 64

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[2:0]	RW	DMATXBRSize	Threshold for generating the transmit FIFO request DMA transfer burst. That is, when the number of data segments in the transmit FIFO is less than or equal to the configured value (256 – DMATXBRSize), DMATXBREQ is valid. The width of the transmit FIFO is 16 bits. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 128 111: 128

SPIRXFIFOCR

SPIRXFIFOCR is a receive FIFO control register.

Offset Address	Register Name	Total Reset Value
0x02C	SPIRXFIFOCR	0x0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										RXINTSize			DMARXBRSize		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[15:6]	RW	reserved	Reserved.
[5:3]	RW	RXINTSize	Threshold for generating the receive FIFO request interrupt. That is, when the number of data segments in the transmit FIFO is less than or equal to the configured value (256 – RXINTSize), RXRIS is valid. The width of the receive FIFO is 16 bits. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64

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			110: 64 111: 64
[2:0]	RW	DMARXBRSize	Burst transfer threshold. When this threshold is reached, the receive FIFO asks the DMA to perform a burst transfer. That is, when number of data segments in the transmit FIFO is less than or equal to the value of DMARXBRSize, DMARXBREQ is valid. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 128 111: 224

14.3 UART

14.3.1 Overview

The universal asynchronous receiver transmitter (UART) interface is an asynchronous serial communication interface. It performs serial-to-parallel conversion on the data received from peripherals and transmits the converted data to the internal bus. It also performs parallel-to-serial conversion on the data that is transmitted to peripherals. The UART is mainly used to interconnect the Hi3521 with the UART of an external chip so that the two chips can communicate with each other.

The Hi3521 provides four UART units.

- UART0: a two-wire UART for debugging
- UART1: a four-wire UART for connecting to an external modem
- UART2/3: a two-wire UART for connecting to a universal UART device.

14.3.2 Features

The UART unit has the following features:

- Supports16x8-bit transmit first-in, first-out (FIFO) and 16x12-bit receive FIFO.
- Supports programmable widths for the data bit and stop bit. The width of the data bit can be set to 5 bits, 6 bits, 7 bits, or 8 bits and width of the stop bit can be set to 1 bit or 2 bits by programming.
- Supports parity check or no check.
- Supports the programmable transfer rate.
- Supports receive FIFO interrupts, transmit FIFO interrupts, receive timeout interrupts, and error interrupts.

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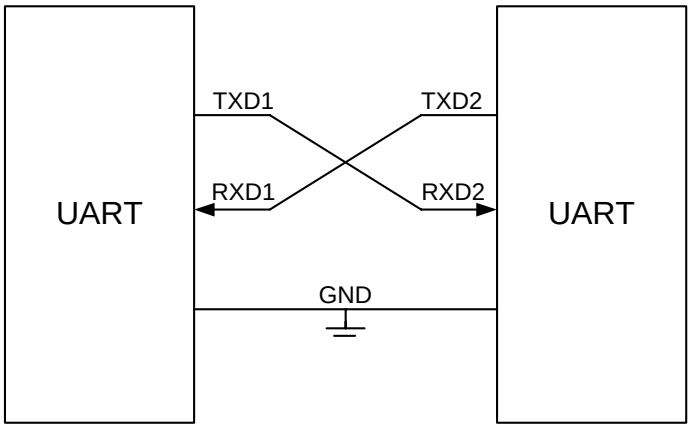
- Supports the query of the raw interrupt status and the masked interrupt status.
- Allows the UART or the transmit/receive function of the UART to be disabled by programming to reduce power consumption.
- Allows the UART clock to be disabled to reduce power consumption.
- Supports DMA.

14.3.3 Function Description

Application Block Diagram

Figure 14-18 shows the typical application of the UART.

Figure 14-18 Typical application block diagram of the UART



The UART serves as an asynchronous bidirectional serial bus. Through the UARTs connected by two data lines, a simplified and effective data transfer mode is implemented.

Function Principle

A frame transfer of the UART involves the start signal, data signal, parity bit, and stop signal, as shown in Figure 14-19. The data frame is output from the TXD end of one UART and then is input to the RXD end of the other UART.

Figure 14-19 Frame format of the UART

The definitions of the start signal, data signal, parity bit, and stop signal are as follows:

- Start signal (start bit)

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It is the start flag of a data frame. According to the UART protocol, the low level of the TXD signal indicates the start of a data frame. When the UART does not transmit data, the level must remain high.

- Data signal (data bit)

  The data bit width can be set to 5 bits, 6 bits, 7 bits, or 8 bits according to the requirements in different applications.

- Parity bit

  It is a 1-bit error correction signal. The UART parity bit can be an odd parity bit, even parity bit, or stick parity bit. The UART can enable and disable the parity bit. For details, see the description of the UART_LCR_H register.

- Stop signal (stop bit)

  It is the stop bit of a data frame. The stop bit width can be set to 1 bit or 2 bits. The high level of TXD indicates the end of the data frame.

14.3.4 Operating Mode

14.3.4.1 Baud Rate Configuration

The operating baud rate of the UART can be set by configuring the registers UART_IBRD and UART_FBRD. The baud rate is calculated as follows:

Current baud rate = Frequency of the UART reference clock (1/2 bus clock frequency)/(16 x Frequency divider)

The clock frequency divider consists of the integral part and the fractional part that correspond to UART_IBRD and UART_FBRD respectively.

For example, assume that the frequency of the UART reference clock is 60 MHz. If UART_IBRD is set to 0x1E and UART_FBRD is set to 0x00, the current baud rate is calculated as follows: 60/(16 x 30) = 0.125 Mbit/s

The typical UART baud rates are 9600 bit/s, 14,400 bit/s, 19,200 bit/s, 38,400 bit/s, 57,600 bit/s, 76,800 bit/s, 115,200 bit/s, 230,400 bit/s, and 460,800 bit/s.

The following examples show how to calculate the clock divider and how to configure the clock divider register:

If the required baud rate is 230,400 bit/s and the frequency of the UART reference clock is 100 MHz, the clock divider is calculated as follows: $(100x10^6)/(16 \times 230,400) = 27.1267$. The integral part IBRD is 27 and the fractional part FBRD is 0.1267.

To calculate the value of the 6-bit UART_FBRD register, do as follows: calculate the value of *m* by using the following formula: $m = \text{integer}(FBRD \times 2^n + 0.5) = (0.1267 \times 2^6 + 0.5) = 8$(n = the width of UART_FBRD). Then set UART_IBRD to 0x001B and set UART_FBRD to 0x08.

If the fractional part of the frequency divider is set to 8, the actual divisor of the baud rate is 27 + 8/64 = 27.125, the baud rate is (100 x 16)/(16 x 27.125) = 230,414.75, and the error rate is (230,414.75 – 230,400)/230,400 x 100 = 0.006%.

The maximum error rate is 1/64 x 100 = 1.56% when the 6-bit UART_FBRD is used. If the value of *m* is 1, the total error rate is greater than 64 clock cycles.

14.3.4.2 Soft Reset

The UART controller can be separately reset by configuring the CRG registers.

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- The UART0 controller can be separately reset by setting PERI_CRG57[uart0_srst_req] to 1.
- The UART1 controller can be separately reset by setting PPERI_CRG57[uart1_srst_req] to 1.
- The UART2 controller can be separately reset by setting PERI_CRG57[uart2_srst_req] to 1.
- The UART3 controller can be separately reset by setting PERI_CRG57[uart3_srst_req] to 1.

After reset, the configuration registers are restored to default values. Therefore, these registers must be initialized again.

14.3.4.3 Data Transfer in Interrupt or Query Mode

Initialization

The initialization is implemented as follows:

Step 1 Write 0 to UART_CR bit[0] to disable the UART.

Step 2 Write to UART_IBRD and UART_FBRD to configure the transfer rate.

Step 3 Configure UART_CR and UART_LCR_H to set the UART operating mode.

Step 4 Configure UART_IFLS to set the thresholds of transmit and receive FIFOs.

Step 5 If the driver runs in interrupt mode, set UART_IMSC to enable the corresponding interrupt; if the driver runs in query mode, disable the generation of corresponding interrupts.

Step 6 Write 1 to UART_CR bit[0] to enable the UART.

---End

Data Transmission

To transmit data, perform the following steps:

Step 1 Write the data to be transmitted to UART_DR and start data transmission.

Step 2 In query mode, check the TX_FIFO status by reading UART_FR bit[5] during the continuous data transmission. According to the TX_FIFO status, determine whether to transmit data to TX_FIFO. In interrupt mode, check the TX_FIFO status by reading the corresponding interrupt status bits and then determine whether to transmit data to TX_FIFO.

Step 3 Check whether the UART transmits all data by reading UART_FR bit[7]. If UART_FR bit[7] is 1, the UART transmits all data.

---End

Data Reception

To receive data, perform the following steps:

- In query mode, detect the RX_FIFO status by reading UART_FR[rxfe] during data reception and then determine whether to read data from the RX_FIFO according to the RX_FIFO status.

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- In interrupt mode, determine whether to read data from RX_FIFO according to corresponding interrupt status bits.

14.3.4.4 Data Transfer in DMA Mode

Initialization

The initialization is implemented as follows:

Step 1 Write 0 to UART_CR[uarten] to disable the UART.

Step 2 Write to UART_IBRD and UART_FBRD to configure the transfer rate.

Step 3 Configure UART_CR and UART_LCR_H to set the UART operating mode.

Step 4 Configure UART_IFLS to set the thresholds of transmit and receive FIFOs.

Step 5 If the driver runs in interrupt mode, set UART_IMSC to enable the corresponding interrupts; if the driver runs in query mode, disable the generation of corresponding interrupts.

Step 6 Write 1 to UART_CR[uarten] to enable the UART.

---End

Data Transmission

The following is an example using the DMA mode. To transmit data, perform the following steps:

Step 1 Configure the DMA data channel, including the data transmission source, destination address, number of data segments to be transmitted, and transmission type. For details, see the description in section 3.5 "DMAC."

Step 2 Set UART_DMACR to 0x2 to enable the DMA transmit function of the UART.

Step 3 Check whether the data is transmitted completely based on the interrupt report status of the DMA. If all data is transmitted, disable the DMA transmit function of the UART.

---End

Data Reception

The following is an example using the DMA mode. To receive data, perform the following steps:

Step 1 Configure the DMA data channel, including data transfer source and destination addresses, data receive area address, number of data segments to be transmitted, and transfer type.

Step 2 Set UART_DMACR to 0x1 to enable the DMA receive function of the UART.

Step 3 Check whether the data is received completely by querying the DMA status. If all data is received, disable the DMA receive function of the UART.

---End

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14.3.5 Register Summary

The Hi3521 provides four UART units: UART0, UART1, UART2, and UART3. Their base addresses are as follows:

- The base address of UART0 registers is 0x2008_0000.
- The base address of UART1 registers is 0x2009_0000.
- The base address of UART2 registers is 0x200A_0000.
- The base address of UART3 registers is0x200B_0000.

Table 14-4 describes the UART registers.

Table 14-4 Summary of UART registers

Offset Address	Register	Description	Page
0x000	UART_DR	Data register	14-38
0x004	UART_RSR	Receive status register or error clear register	14-39
0x008 – 0x014	RESERVED	Reserved	-
0x018	UART_FR	Flag register	14-40
0x01C – 0x020	RESERVED	Reserved	-
0x024	UART_IBRD	Integral baud rate register	14-42
0x028	UART_FBRD	Fractional baud rate register	14-42
0x02C	UART_LCR_H	Transfer mode control register	14-43
0x030	UART_CR	Control register	14-44
0x034	UART_IFLS	Interrupt FIFO threshold select register	14-46
0x038	UART_IMSC	Interrupt mask register	14-47
0x03C	UART_RIS	Raw interrupt status register	14-48
0x040	UART_MIS	Masked interrupt status register	14-49
0x044	UART_ICR	Interrupt clear register	14-50
0x048	UART_DMACR	DMA control register	14-51

14.3.6 Register Description

UART_DR

UART_DR is a UART data register that stores the received data and the data to be transmitted. The receive status can be queried by reading this register.

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Offset Address	Register Name	Total Reset Value
0x000	UART_DR	0x00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				oe	be	pe	fe	data							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:12]	-	reserved	Reserved.
[11]	RO	oe	Overflow error. 0: No overflow error occurs. 1: An overflow error occurs. That is, a data segment is received when the receive FIFO is full.
[10]	RO	be	Break error. 0: No break error occurs. 1: A break error occurs. That is, the time of receive data input signal keeping low is longer than a full word transfer. A full word consists of a start bit, a data bit, a parity bit, and a stop bit.
[9]	RO	pe	Parity error. 0: No parity error occurs. 1: A parity error occurs.
[8]	RO	fe	Frame error. 0: No frame error occurs. 1: A frame error (namely, stop bit error) occurs.
[7:0]	RW	data	Data received and to be transmitted.

UART_RSR

UART_RSR is a receive status register or error clear register.

- It acts as the receive status register when being read.
- It acts as the error clear register when being written.

You can query the receive status by reading UART_DR. The status information about the break, frame, and parity read from UART_DR has priority over that read from UART_RSR. That is, the status read from UART_DR changes faster than that read from UART_RSR.

UART_RSR is reset when any value is written to it.

Offset Address	Register Name	Total Reset Value
0x004	UART_RSR	0x00

Bit	7	6	5	4	3	2	1	0

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Name	reserved				oe	be	pe	fe
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:4]	-	reserved	Reserved.
[3]	RW	oe	Overflow error. 0: No overflow error occurs. 1: An overflow error occurs. When the FIFO is full, the next data segment cannot be written to the FIFO and an overflow occurs in the shift register. Therefore, the contents in the FIFO are valid. In this case, the CPU must read the data immediately to spare the FIFO.
[2]	RW	be	Break error. 0: No break error occurs. 1: A break error occurs. A break error occurs when the time of the receive data signal keeping low is longer than a full word transfer. A full word consists of a start bit, a data bit, a parity bit, and a stop bit.
[1]	RW	pe	Parity error. 0: No parity error occurs. 1: A parity error occurs when the received data is checked. In FIFO mode, the error is associated with the data at the top of the FIFO.
[0]	RW	fe	Frame error. 0: No frame error occurs. 1: The stop bit of the received data is incorrect. The valid stop bit is 1.

UART_FR

UART_FR is a UART flag register.

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Offset Address	Register Name	Total Reset Value
0x018	UART_FR	0x0012

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								txfe	rxff	txff	rxfe	busy	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[15:8]	-	reserved	Reserved.
[7]	RO	txfe	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the transmit holding register is empty. If UART_LCR_H [fen] is 1, the bit is set to 1 when the transmit FIFO is empty.
[6]	RO	rxff	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the receive holding register is full. If UART_LCR_H [fen] is 1, this bit is set to 1 when the receive FIFO is full.
[5]	RO	txff	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the transmit holding register is full. If UART_LCR_H [fen] is 1, the bit is set to 1 when the transmit FIFO is full.
[4]	RO	rxfe	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the receive holding register is empty. If UART_LCR_H [fen] is 1, this bit is set to 1 when the receive FIFO is empty.
[3]	RO	busy	UART busy/idle status. 0: The UART is idle or data transmission is complete. 1: The UART is busy in transmitting data. If the bit is set to 1, the status is kept until the entire byte (including all stop bits) is transmitted from the shift register. Regardless of whether the UART is enabled, this bit is set to 1 when the transmit FIFO is not empty.
[2:0]	-	reserved	Reserved.

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UART_IBRD

UART_IBRD is an integral baud rate register.

Offset Address	Register Name	Total Reset Value
0x024	UART_IBRD	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	baud divint															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	baud divint	Clock frequency divider corresponding to the integral part of the baud rate. All bits are cleared after reset.

UART_FBRD

UART_FBRD is a fractional baud rate register.

CAUTION

- The values of UART_IBRD and UART_FBRD can be updated only after the current data is transmitted and received completely.
- The minimum clock frequency divider is 1 and the maximum divider is 65,535 (2^{16} – 1). That is, UART_IBRD cannot be 0 and UART_FBRD is ignored if UART_IBRD is 0. Similarly, if UART_IBRD is equal to 65,535 (0xFFFF), UART_IBRD must be 0. If UART_FBRD is greater than 0, the data fails to be transmitted or received.
- Assume that UART_FBRD is set to 0x1E and UART_IBRD is set to 0x01. This indicates that the integral part of the clock frequency divider is 30 and the fractional part of the clock frequency divider is 0.015625. Therefore, the clock frequency divider is 30.015625.
- Baud rate of the UART = Internal bus frequency/(16 x clock divider) = Internal bus frequency/(16 x 30.015625).

Offset Address	Register Name	Total Reset Value
0x028	UART_FBRD	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		baud divfrac					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	-	reserved	Reserved.

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[5:0]	RW	band divfrac	Clock frequency divider corresponding to the fractional part of the baud rate. All bits are cleared after reset.

UART_LCR_H

UART_LCR_H is a transfer mode control register. The registers UART_LCR_H, UART_IBRD, and UART_FBRD are combined to form a 30-bit register. If UART_IBRD and UART_FBRD are updated, UART_LCR_H must be updated at the same time.

Offset Address	Register Name	Total Reset Value
0x02C	UART_LCR_H	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								sps	wlen		fen	stp2	eps	pen	brk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	-	reserved	Reserved.
[7]	RW	sps	Parity select. When bit 1, bit 2, and bit 7 of this register are set to 1, the parity bit is 0 during transmission and detection. When bit 1 and bit 7 of this register are set to 1 and bit 2 is set to 0, the parity bit is 1 during transmission and detection. When bit 1, bit 2, and bit 7 are cleared, the stick parity bit is disabled.
[6:5]	RW	wlen	Count of bits in a transmitted or received frame. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits
[4]	RW	fen	Transmit/receive FIFO enable. 0: disabled 1: enabled
[3]	RW	stp2	2-bit stop bit at the end of a transmitted frame. 0: There is no 2-bit stop bit at the end of the transmitted frame. 1: There is a 2-bit stop bit at the end of the transmitted frame. The receive logic does not check for the 2-bit stop bit during data reception.

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[2]	RW	eps	Parity select during data transmission and reception. 0: The odd parity is generated or checked during data transmission and reception. 1: The even parity is generated or checked during data transmission and reception. When UART_LCR_H [fen] is 0, this bit becomes invalid.
[1]	RW	pen	Parity enable. 0: The parity is disabled. 1: The parity is generated on the transmit side and checked on the receive side.
[0]	RW	brk	Break transmit. 0: invalid 1: After the current data transmission is complete, UTXD outputs low level continuously. Note: This bit must retain 1 during the period of at least two full frames to ensure the break command is executed properly. In general, the bit must be set to 0.

UART_CR

UART_CR is a UART control register.

To configure UART_CR, perform the following steps:Write 0 to UART_CR[uarten] to disable the UART.

Step 2 Wait until the current data transmission or reception is complete.

Step 3 Clear UART_LCR_H [fen].

Step 4 Configure UART_CR.

Step 5 Write 1 to UART_CR[uarten] to enable the UART.

---End

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Offset Address	Register Name	Total Reset Value
0x030	UART_CR	0x0300

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ctsen	rtsen	reserved		rts	dtr	rxe	txe	lbe	reserved						uarten
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	ctsen	CTS hardware flow control enable. 0: disabled 1: enabled. Data is transmitted only when the nUARTCTS signal is valid.
[14]	RW	rtsen	RTS hardware flow control enable. 0: disabled 1: enabled. The data reception request is raised only when the receive FIFO has available space.
[13:12]	-	reserved	Reserved.
[11]	RW	rts	Request transmit. This bit is the inversion of the status output signal nUARTRTS of the UART modem. 0: The output signal retains. 1: When this bit is set to 1, the output signal is 0.
[10]	RW	dtr	Data transmit ready. This bit is the inversion of the status output signal nUARTDTR of the UART modem. 0: The output signal retains. 1: When this bit is set to 1, the output signal is 0.
[9]	RW	rxe	UART receive enable. 0: disabled 1: enabled If the UART is disabled during data reception, the current data reception is stopped abnormally.
[8]	RW	txe	UART transmit enable. 0: disabled 1: enabled If the UART is disabled during data transmission, the current data transmission is stopped abnormally.

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[7]	RW	lbe	Loopback enable. 0: disabled 1: UARTTXD is looped back to UARTRXD.
[6:1]	-	reserved	Reserved.
[0]	RW	uarten	UART enable. 0: disabled 1: enabled If the UART is disabled during data reception and transmission, the data transfer is stopped abnormally.

UART_IFLS

UART_IFLS is an interrupt FIFO threshold select register. It is used to set a threshold for triggering a FIFO interrupt (UART_TXINTR or UART_RXINTR).

Offset Address	Register Name	Total Reset Value
0x034	UART_IFLS	0x0012

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										rxiflsel			txiflsel		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[15:6]	-	reserved	Reserved.
[5:3]	RW	rxiflsel	Receive interrupt FIFO threshold select. A receive interrupt is triggered when any of the following conditions is met: 000: receive FIFO ≥ 1/8 full 001: receive FIFO ≥ 1/4 full 010: receive FIFO ≥ 1/2 full 011: receive FIFO ≥ 3/4 full 100: receive FIFO ≥ 7/8 full 101 – 111: reserved

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[2:0]	RW	txiflsel	Transmit interrupt FIFO threshold select. A transmit interrupt is triggered when any of the following conditions is met: 000: transmit FIFO ≤ 1/8 full 001: transmit FIFO ≤ 1/4 full 011: transmit FIFO ≤ 3/4 full 010: transmit FIFO ≤ 1/2 full 100: transmit FIFO ≤ 7/8 full 101 – 111: reserved

UART_IMSC

UART_IMSC is an interrupt mask register. It is used to mask interrupts.

Offset Address	Register Name	Total Reset Value
0x038	UART_IMSC	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeim	beim	peim	feim	rtim	txim	rxim	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	-	reserved	Reserved.
[10]	RW	oeim	Mask status of the overflow error interrupt. 0: masked 1: not masked
[9]	RW	beim	Mask status of the break error interrupt. 0: masked 1: not masked
[8]	RW	peim	Mask status of the parity interrupt. 0: masked 1: not masked
[7]	RW	feim	Mask status of the frame error interrupt. 0: masked 1: not masked
[6]	RW	rtim	Mask status of the receive timeout interrupt. 0: masked 1: not masked

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[5]	RW	txim	Mask status of the transmit interrupt. 0: masked 1: not masked
[4]	RW	rxim	Mask status of the receive interrupt. 0: masked 1: not masked
[3:0]	-	reserved	Reserved.

UART_RIS

UART_RIS is a raw interrupt status register. The contents of this register are not affected by the UART_IMSC register.

Offset Address	Register Name	Total Reset Value
0x03C	UART_RIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeris	beris	peris	feris	rtris	txris	rxris	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	-	reserved	Reserved.
[10]	RO	oeris	Status of the raw overflow error interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	beris	Status of the raw break error interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	peris	Status of the raw parity interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	feris	Status of the raw error interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	rtris	Status of the raw receive timeout interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

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[5]	RO	txris	Status of the raw transmit interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	rxris	Status of the raw receive interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3:0]	-	reserved	Reserved.

UART_MIS

UART_MIS is a masked interrupt status register. The contents of this register are the results obtained after the raw interrupt status is ANDed with the interrupt mask status.

Offset Address	Register Name	Total Reset Value
0x040	UART_MIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oemis	bemis	pemis	femis	rtmis	txmis	rxmis	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	-	reserved	Reserved.
[10]	RO	oemis	Status of the masked overflow error interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	bemis	Status of the masked break error interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	pemis	Status of the masked parity interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	femis	Status of the masked error interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	rtmis	Status of the masked receive timeout interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

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[5]	RO	txmis	Status of the masked transmit interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	rxmis	Status of the masked receive interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3:0]	-	reserved	Reserved.

UART_ICR

UART_ICR is an interrupt clear register. When 1 is written to it, the corresponding interrupt is cleared. Writing 0 has no effect.

Offset Address	Register Name	Total Reset Value
0x044	UART_ICR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeic	beic	peic	feic	rtic	txic	rxic	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	-	reserved	Reserved.
[10]	WO	oeic	Overflow error interrupt clear. 0: invalid 1: cleared
[9]	WO	beic	Break error interrupt clear. 0: invalid 1: cleared
[8]	WO	peic	Parity interrupt clear. 0: invalid 1: cleared
[7]	WO	feic	Error interrupt clear. 0: invalid 1: cleared
[6]	WO	rtic	Receive timeout interrupt clear. 0: invalid 1: cleared

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[5]	WO	txic	Transmit interrupt clear. 0: invalid 1: cleared
[4]	WO	rxic	Receive interrupt clear. 0: invalid 1: cleared
[3:0]	-	reserved	Reserved.

UART_DMACR

UART_DMACR is a DMA control register. It is used to control whether to enable the DMA operation of the transmit and receive FIFOs.

Offset Address	Register Name	Total Reset Value
0x048	UART_DMACR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													dmaonerr	txdmae	rxdmae
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:3]	-	reserved	Reserved.
[2]	RW	dmaonerr	Receive channel DMA enable when the UART error interrupt (UARTEINTR) occurs. 0: When UARTEINTR is valid, the DMA output request (UARTRXDMASREQ or UARRTXDMABREQ) of the receive channel is valid. 1: When UARTEINTR is valid, the DMA output request (UARTRXDMASREQ or UARRTXDMABREQ) of the receive channel is invalid.
[1]	RW	txdmae	Transmit FIFO DMA enable. 0: disabled 1: enabled
[0]	RW	rxdmae	Receive FIFO DMA enable. 0: disabled 1: enabled

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14.4 IR Interface

14.4.1 Overview

The infrared (IR) module receives data over the IR interface.

14.4.2 Features

The IR module has the following features:

- Allows to disable the IR receive module by using software.
- Supports two operating modes:
  - Mode 0: supports decoding in four formats (including NEC with simple repeat code, NEC with full repeat code, SONY, and TC9012), error detection on received data, and IR wakeup.
  - Mode 1: supports the symbol level width detection in any data format.
- In mode 0, supports the receive data overflow interrupt, receive data frame format error interrupt, receive data frame interrupt, key release interrupt, and combined interrupt.
- In mode 1, supports the receive symbol overflow interrupt, receive symbol interrupt, symbol timeout interrupt, and combined interrupt.
- Supports the query of the raw interrupt status and the masked interrupt status.
- Supports interrupt clear and mask (write to clear).
- Supports IR wakeup.
- Supports the reference clock frequency ranging from 1 MHz to 128 MHz and controls the clock frequency divider by software programming, enabling the frequency of the working clock to be prescaled to 1 MHz.

14.4.3 Function Description

The IR module receives infrared signals transmitted by the infrared remote control, decodes the signals, and then transmits the decoded signals to the ARM system. The ARM system performs corresponding operations according to the received codes, which implements expected functions. The IR module connects to the APB of the ARM subsystem. When the chip is in the low-power state (the CPU is in low freguency), the IR module generates an interrupt after receiving a complete frame, and transmits the interrupt to the CPU. In this way, the IR wake function is implemented.

The analysis of the signals transmitted by various infrared remote controls shows that the lead codes in the infrared commands vary according to remote controls. In addition, the subsequent control commands and the bits of command codes are also different. This is because infrared remote controls are not designed based on a unified infrared remote control standard. The basic encoding principles, however, are the same. That is, the pulses with different periods and duty ratios are used to represent 0 and 1. The duty ratios and pulse cycles may vary according to remote controls. Based on preceding differences, the code formats of the infrared data are classified into NEC with simple repeat code, NEC with full repeat code, TC9012 code, and SONY code.

Table 14-5 to Table 14-7 describe the code formats of the received infrared data.

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Table 14-5 Code formats of the received infrared data (NEC with simple repeat code)

Data Format		**NEC with Simple Repeat Code**			
		uPD6121G	**D6121/BU5777/D1913**	**LC7461M-C13**	**AEHA**
Lead code (10 μs)	LEAD_S	900	900	900	337.6
	LEAD_E	450	450	450	168.8
Bit0 (10 μs)	B0_L	56	56	56	42.2
	B0_H	56	56	56	42.2
Bit1 (10 μs)	B1_L	56	56	56	42.2
	B1_H	169	169	169	126.6
Simple repeat code (10 μs)	SLEAD_S	900	900	900	337.6
	SLEAD_E	225	225	225	337.6
Burst (10 μs)		55	55	55	42.2
Frame length (10 μs)		108,00	10,800	10,800	8,777.6 – 12,828.8
Valid data bit		32	32	42	48

Table 14-6 Code formats of the received infrared data (NEC with full repeat code)

Data Format		**NEC with Full Repeat cCode**						
		uPD6121G	**LC7461M-C13**	**MN6024-C5D6**	**MN6014-C6D6**	**MATNEW**	**MN6030**	**PANASONIC**
Lead code (10 μs)	LEAD_S	900	900	337.6	349.2	348.8	349	352
	LEAD_E	450	450	337.6	349.2	374.4	349	352
Bit 0 (10 μs)	B0_L	56	56	84.4	87.3	43.6	87.3	88
	B0_H	56	56	84.4	87.3	43.6	87.3	88
Bit 1 (10 μs)	B1_L	56	56	84.4	87.3	43.6	87.3	88
	B1_H	169	169	253.2	174.6	130.8	261.9	264
Simple repeat code (10 μs)	SLEAD_S	None	None	None	None	None	None	None
	SLEAD_E							
Burst (10 μs)		55	55	84.4	87.3	43.6	87.3	88
Frame length (10 μs)		10,800	10,800	10,130	10,470	12,413.6 – 16,594.4	10,500	10,400

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Data Format	NEC with Full Repeat cCode						
	uPD6121G	LC7461 M-C13	MN602 4-C5D6	MN6014 -C6D6	MATNEW	MN6030	PANA SONIC
Valid data bit	32	42	22	24	48	22	22

Table 14-7 Code formats of the received infrared data (TC9012 code and SONY code)

Data Format		TC9012	SONY			
		TC9012F/9243	SONY-D7C5	SONY-D7C6	SONY-D7C8	SONY-D7C13
Lead code (10 µs)	LEAD_S	450	240	240	240	240
	LEAD_E	450	60	60	60	60
Bit0 (10 µs)	B0_L	56	60	60	60	60
	B0_H	56	60	60	60	60
Bit1 (10 µs)	B1_L	56	120	120	120	120
	B1_H	169	60	60	60	60
Simple repeat code (10 µs)	SLEAD_S	None	None	None	None	None
	SLEAD_E					
Burst (10 µs)		56	None	None	None	None
Frame length (10 µs)		10,800	4500	4500	4500	4500
Valid data bit		32	12	13	15	20

14.4.3.1 NEC with Simple Repeat Code

Frame Format

The NEC with simple repeat code consists of the following:

- Start code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit depend on specific code format. During data code reception, its LSB is received first.
- Burst signal: It is used to receive the last data bit.

Figure 14-20 shows the frame format of transmitting a single NEC with simple repeat code.

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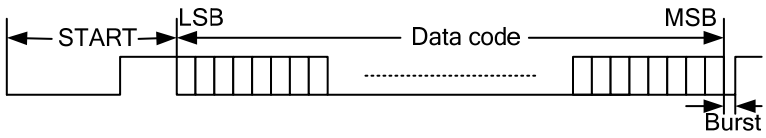
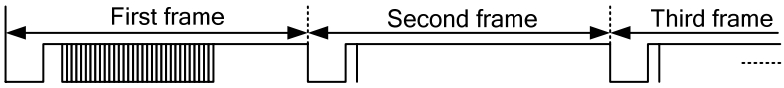
Figure 14-20 Frame format for transmitting a single NEC with simple repeat code



If a complete data frame is received after the key is held down for more than one frame length, the subsequently received data frame consists only of a simple lead code and a burst signal. The lead code also consists of a start code (low level) and an end code (high level). Figure 14-21 shows the frame format for transmitting NEC with simple repeat codes by pressing the key continuously.

Figure 14-21 Frame format for transmitting NEC with simple repeat codes by pressing the key continuously



Code Format

Figure 14-22 shows the definitions of bit0 and bit1 of the NEC with simple repeat code.

Figure 14-22 Definitions of bit0 and bit1 of the NEC with simple repeat code

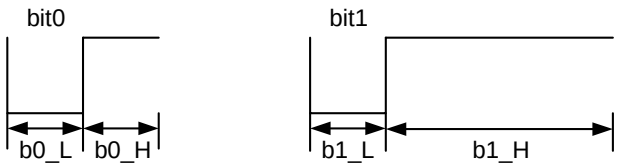


Figure 14-23 shows the format for transmitting a single NEC with simple repeat code. Figure 14-24 shows the format for transmitting consecutive NEC with simple repeat codes.

Figure 14-23 Format for transmitting a single NEC with simple repeat code

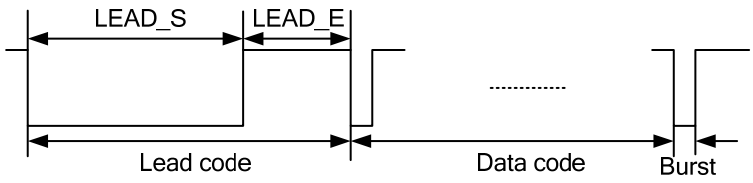


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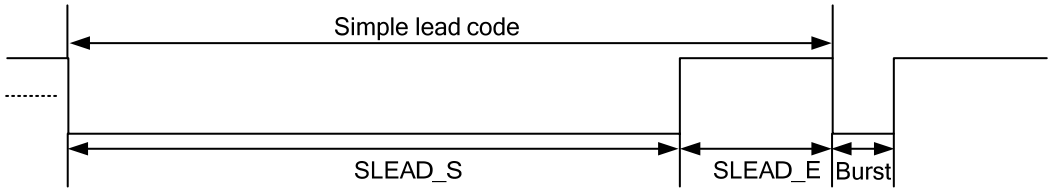
Figure 14-24 Code format for transmitting consecutive NEC with simple repeat codes



NOTE

The pulse width of the high and low levels and the frame length depend on specific code formats. See Table 14-5 to Table 14-7.

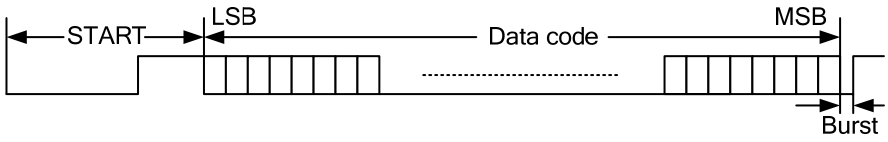
The frame length must be less than or equal to 160 ms. Otherwise, the simple lead code cannot be identified.

14.4.3.2 NEC with Full Repeat Code

Frame Format

The data format of the NEC with full repeat code consists of the following parts: START (lead code), data code, and burst. START (lead code): Consists of a start code (low level) and an end code (high level). Data code: The valid bits and the definition of each bit are determined by the specific code format. During data code reception, the LSB is received first. Burst signal: It is used to receive the last data bit. Figure 14-25 shows the frame format for transmitting a single NEC with full repeat code.

Figure 14-25 Frame format for transmitting a single NEC with full repeat code



If a complete data frame (first frame) is received after the key is held down for more than one frame length, the subsequently received data frame is still a complete data frame. That is, the first frame is transmitted repeatedly based on the frame length. Figure 14-26 shows the frame format for transmitting NEC with full repeat codes by pressing the key continuously.

Figure 14-26 Frame format for transmitting NEC with full repeat codes by pressing the key continuously

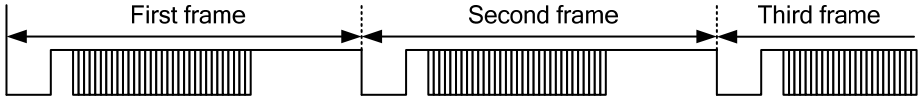


Figure 14-25 and Figure 14-26 show that the only difference between the NEC with simple repeat code and the NEC with full repeat code is the format of the repeat frame. For the NEC with simple repeat code, the simple lead code is transmitted; for the NEC with full repeat code, the complete frame is transmitted. That is, the first frame and the repeat frame are the same.

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Code Format

Figure 14-27 shows the definitions of bit0 and bit1 of the NEC with full repeat code.

Figure 14-27 Definitions of bit0 and bit1 of the NEC with full repeat code

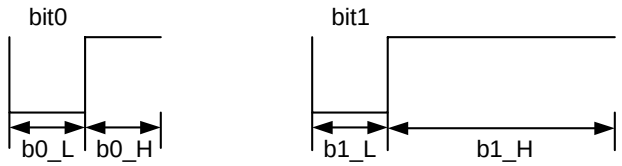
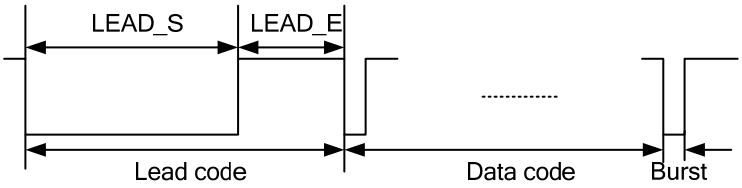


Figure 14-28 shows the format for transmitting a single NEC with full repeat code.

Figure 14-28 Format for transmitting a single NEC with full repeat code



NOTE

The pulse width of the high and low levels and the frame length depend on specific code formats. See Table 14-5 to Table 14-7.

14.4.3.3 TC9012 Code

Frame Format

CAUTION

According to the features of the TC9012 code, the first bit of all key codes must be all 1s or all 0s. Otherwise, unnecessary frames are generated when the key are pressed continuously.

The TC9012 code consists of the following parts:

- START code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit depend on the specific code pattern. During data code reception, its LSB is received first.
- Burst signal: It is used to receive the last data bit.

Figure 14-29 shows the frame format for transmitting a single TC9012 code.

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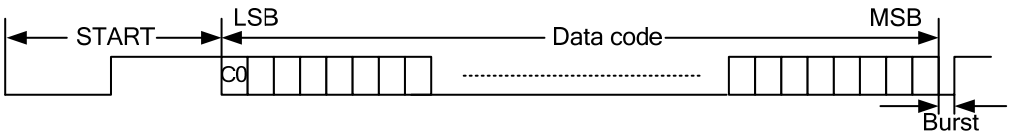
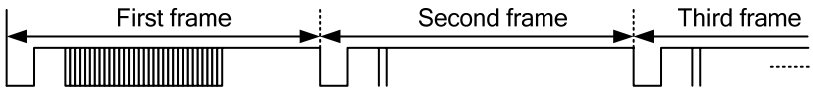
Figure 14-29 Frame format for transmitting a single TC9012 code



When a complete data frame is received after the key is held down for more than one frame length, the subsequently received data frame consists of a lead code, a data bit, and a burst signal. The lead code also consists of a start code (low level) and an end code (high level). The data bit is the complement of the first data bit (C0) received in the previous frame. Figure 14-30 shows the frame format for transmitting TC9012 codes by pressing the key continuously.

Figure 14-30 Frame format for transmitting TC9012 codes by pressing the key continuously



Code Format

Figure 14-31 shows the definitions of bit0 and bit1 of the TC9012 code.

Figure 14-31 Definitions of bit0 and bit1 of the TC9012 code

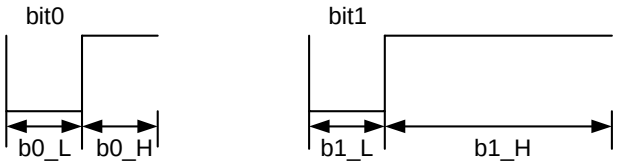


Figure 14-32 shows the format for transmitting a single TC9012 code.

Figure 14-32 Format for transmitting a single TC9012 code

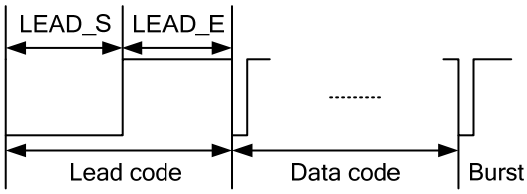


Figure 14-33 shows the format for transmitting consecutive TC9012 codes when C0 is 1.

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Figure 14-33 Format for transmitting consecutive TC9012 codes (C0 = 1)

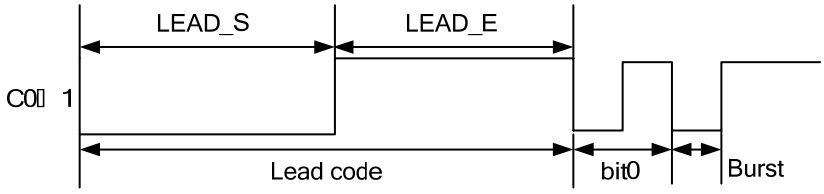
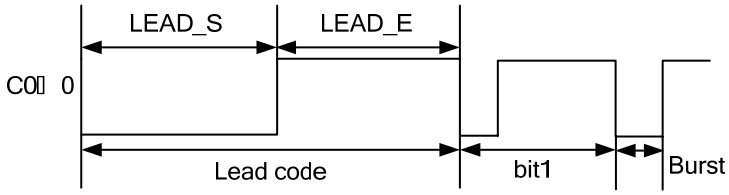


Figure 14-34 shows the format for transmitting consecutive TC9012 codes when C0 is 0.

Figure 14-34 Format for transmitting consecutiveTC9012 codes (C0 = 0)



NOTE

The pulse width of the high level and low level and the frame length depend on specific code patterns. For details, see Table 14-5 to Table 14-7. In addition, the frame length must be less than or equal to 160 ms. Otherwise, the repeat frame cannot be identified.

14.4.3.4 SONY Code

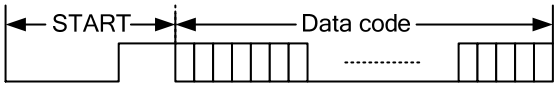
Frame Format

A SONY code consists of the following parts:

- START code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit are determined by the specific code pattern.

During reception, the LSB is received first. Figure 14-35 shows the frame format for transmitting a single SONY code.

Figure 14-35 Frame format for transmitting a single SONY code



When a complete data frame is received after the key is pressed for more than one frame length, the subsequently received data frame is also a complete data frame. Figure 14-36 shows the frame format for continuously transmitting SONY codes by pressing the key.

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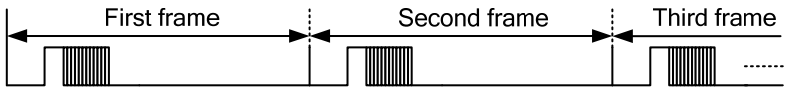
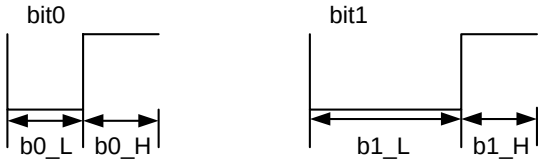
Figure 14-36 Frame format for continuously transmitting SONY codes by pressing the key



Code Format

Figure 14-37 shows the definitions of bit0 and bit1 of a SONY code.

Figure 14-37 Definitions of bit0 and bit1 of a SONY code



NOTE

The pulse width of the high level and low level and the frame length depend on specific code patterns. For details, see Table 14-5 to Table 14-7.

14.4.4 Operating Mode

Soft Reset

When CRG_PERCTRL57[ir_srst_req] is set to 1, the IR module is soft-reset separately. After reset, each configuration register is restored its default value. Therefore, these registers must be reinitialized.

Instances of Configuring Registers

Figure 14-38 shows the process of initializing the IR module.

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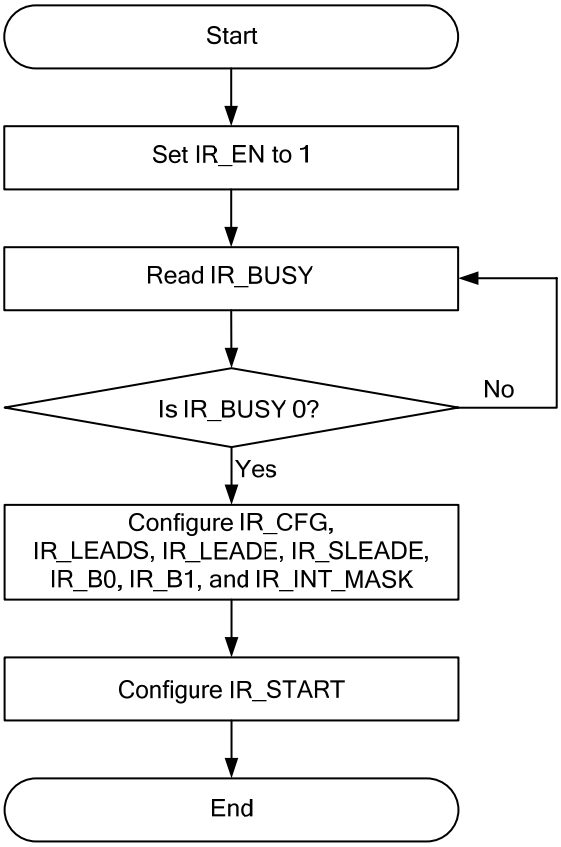
Figure 14-38 Process of initializing the IR module



To initialize the IR module, perform the following steps:

Step 1 Select the address space of the IR module.

Step 2 Set IR_EN bit [0] to 1 to enable the IR receive module.

Step 3 Read IR_BUSY to check the current status of the IR module.

- If the value of IR_BUSY is 1, the IR module is busy. Then continue to read IR_BUSY. Note that configuring other control registers of the IR module by using software has no effect in this case.
- If the value of is 0, the IR module is idle. Then go to 4.

Step 4 Configure IR_CFG, IR_LEADS, IR_LEADE, IR_SLEADE, IR_B0, IR_B1, and IR_INT_MASK.Note: You can update corresponding registers as required. If the registers are not updated, the original values are retained.

Step 5 Configure IR_STARTafter all IR control registers are configured. This is because IR_START is used to generate the start signal. If IR_START is configured, the IR module starts to receive infrared data based on the values of IR control registers.

---End

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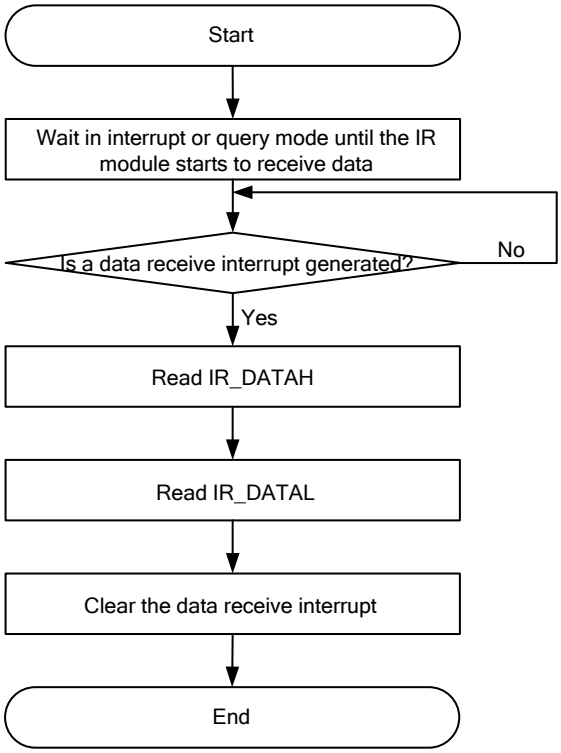
Figure 14-39 Process of reading the decoded data



To read the decoded data, perform the following steps:

Step 1 Select the address space of the IR module.

Step 2 Wait in interrupt or query mode until data frames are received.

- In interrupt mode, when the CPU receives an interrupt request signal from the IR module, read the value of IR_INT_STATUS[intms_rcv].If the value is 1, the IR module receives a data frame. Then, go to 3. If the value is 0, repeat 2 to wait for an interrupt.
- In query mode, continuously read the value of IR_INT_STATUS[intrs_rcv] by using software or read the value at intervals. If the value is 1, the IR module receives a data frame. Then, go to 3. If the value is 0, the IR module does not receive any data frame. Then, repeat 2 to continue the query.

Step 3 Read IR_DATAH. If the number of data bits in one frame is less than or equal to 32, skip this step.

Step 4 Read IR_DATAL.

Step 5 Clear the data receive interrupt.

---End

14.4.5 Register Summary

Table 14-8 describes IR registers.

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Table 14-8 Summary of IR registers (base address: 0x2007_0000)

Offset Address	Register	Description	Page
0x000	IR_EN	IR receive enable control register	14-63
0x004	IR_CFG	IR configuration register	14-64
0x008	IR_LEADS	Lead code start bit margin configuration register (valid when IR_CFG[ir_mode] is 0 only)	14-66
0x00C	IR_LEADE	Lead code end bit margin configuration register (valid when IR_CFG[ir_mode] is 0 only)	14-67
0x010	IR_SLEADE	Simple lead code end bit margin configuration register (valid when IR_CFG[ir_mode] is 0 only)	14-68
0x014	IR_B0	Data 0 level judge margin configuration register (used only when IR_CFG[ir_mode] is 0)	14-69
0x018	IR_B1	Data 1 level judge margin configuration register (used only when IR_CFG[ir_mode] is 0)	14-70
0x01C	IR_BUSY	Configuration busy flag register	14-71
0x020	IR_DATAH	Upper 16-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or symbol count register in the symbol FIFO (IR_CFG[ir_mode] = 1)	14-72
0x024	IR_DATAL	Lower 32-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or IR received symbol width register (IR_CFG[ir_mode] = 1)	14-73
0x028	IR_INT_MASK	IR interrupt mask register	14-74
0x02C	IR_INT_STATUS	IR interrupt status register	14-76
0x030	IR_INT_CLR	IR interrupt clear register	14-78
0x034	IR_START	IR start configuration register	14-79

14.4.6 Register Description

IR_EN

IR_EN is an IR receive enable control register.

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CAUTION

Before configuring other registers, you must set IR_EN[ir_en] to 1 by using software. When IR_EN[ir_en] is 0, other registers are read-only and the read values are their reset values.

Offset Address	Register Name	Total Reset Value
0x000	IR_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ir_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	ir_en	IR receive module enable. 0: disabled 1: enabled.

IR_CFG

IR_CFG is an IR configuration register.

CAUTION

Before configuring this register, you must set IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value is retained after configuration.

The reference clock frequency supported by the IR module ranges from 1 MHz to 128 MHz. The relationship between the frequency and the clock frequency divider ir_freq is as follows:

- When the reference clock frequency is 1 MHz, ir_freq must be set to 0x00.
- If the reference clock frequency is 128 MHz, ir_freq must be set to 0x7F.

When the frequency of the IR reference clock is not an integer ranging from 1 MHz to 128 MHz, the clock frequency divider is rounded off. For example, if the reference clock frequency is 12.1 MHz, the clock frequency divider is 0x0B; if the reference clock frequency is 12.8 MHz, the clock frequency divider is 0x0C.

The relationship between the frequency offset and the count deviation is as follows: If the base frequency is f and the frequency variation is D_f, the frequency offset ratio is D_f/f. If the count deviation of the counter is Dcnt, and the judge level width is s (in μs), the count deviation Dcnt is calculated as follows: Dcnt = |0.1 x s x ratio|Therefore, when the clock has frequency offset, the valid range of the parameter value needs to be changed. If the frequency

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increases, the corresponding margin range is changed to [min + Dcnt, max + Dcnt]. Where, min and max indicate the margins without frequency offset. If the frequency decreases, the offset range is changed to [min – Dcnt, max – Dcnt]. Take the margin of the start bit in the lead code as an example. If the base frequency is 100 MHz, and the frequency increases by 0.1 MHz, then the ratio is 0.001 (0.1/100). Assume that s is 9000 μs. Dcnt is calculated as follows: Dcnt = |0.1 x 9,000 x 0.001| = 1. In this case, the margin range of ir_leads must be changed to [0x033D, 0x3CD].

Offset Address	Register Name	Total Reset Value
0x004	IR_CFG	0x3E80_1F0B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ir_max_level_width																ir_format		ir_bits						ir_mode	ir_freq						
Reset	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	1	0	1	1

Bits	Access	Name	Description
[31:16]	RW	ir_max_level_width	Invalid when IR_CFG[ir_mode] is 0. Indicates the maximum level width (in 10 μs) of a symbol whenIR_CFG[ir_mode] is 1. This width indicates the end of a symbol stream.
[15:14]	RW	ir_format	Indicates the data code format when IR_CFG[ir_mode] is 0. 00: NEC with simple repeat code 01: TC9012 code 10: NEC with full repeat code 11: SONY code For details about the relationship between code types and code formats, see Table 14-5 to Table 14-7. Indicates the symbol format when IR_CFG[ir_mode] is 1. bit[15]: reserved The definitions of bit[14] are as follows: 0: The symbol is from low to high, and the symbol stream ends at the high level. 1: The symbol is from high to low, and the symbol stream ends at the low level.

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[13:8]	RW	ir_bits	Indicates the number of data bits in a frame when IR_CFG[ir_mode] is 0. 0x00 – 0x2F: 1 – 48 data bits in a frame 0x30 – 0x3F: reserved If ir_bits is set to a value ranging from 0x30 to 0x3F by using software, the setting has no effect and the original value is retained. Indicates the symbol receive interrupt threshold when IR_CFG[ir_mode] is 1. bit[13]: reserved bit[12:8]: 0x0 – 0x1F. 0x0 indicates that an interrupt is reported when there is at least one symbol in the FIFO; 0x1F indicates that an interrupt is reported when there are at least 32 symbols in the FIFO, and so on.
[7]	RW	ir_mode	IR operating mode. 0: The decoded complete data frames are output. 1: Only the symbol width is output.
[6:0]	RW	ir_freq	Frequency divider of the working clock. 0x00 – 0x7F: correspond to the working clock divider 1 – 128 respectively.

IR_LEADS

IR_LEADS is a lead code start bit margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

Before setting this register, you must set IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.

The margin must be considered based on the typical value of the specific code type for accurately judging the start bit of the lead code. For details about the typical values of specified code types, see the values of LEAD_S in Table 14-5 to Table 14-7.

- For a pulse width whose typical value is greater than or equal to 400 (10 µs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example. If the typical value of LEAD_S is 900, the values of cnt_leads_min and cnt_leads_max are calculated as follows:

  cnt_leads_min = 900 x 92% = 828 = 0x33C cnt_leads_max = 900 x 108% = 972 = 0x3CC
- For a pulse width whose typical value is less than 400 (10 µs precision), the recommended margin is 20% of the typical value. Take the SONY-D7C5 as an example. If the typical value of LEAD_S is 240, the values of cnt_leads_min and cnt_leads_max are calculated as follows:

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cnt_leads_min = 240 x 80% = 192 = 0xC0 cnt_leads_max = 240 x 120% = 288 = 0x120

The basic configuration principle is as follows: cnt_leads_max is greater than or equal to cnt_leads_min, and cnt_leads_min is greater than cnt0_b_max and cnt1_b_max.

Offset Address	Register Name	Total Reset Value
0x008	IR_LEADS	0x033C_03CC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt_leads_min								reserved								cnt_leads_max							
Reset	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	cnt_leads_min	Minimum pulse width of the start bit of the lead code. 0x000 – 0x007: reserved
[15:10]	-	reserved	Reserved.
[9:0]	RW	cnt_leads_max	Maximum pulse width of the start bit of the lead code. 0x000 – 0x007: reserved

IR_LEADE

IR_LEADE is a lead code end bit margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the NEC with simple repeat code, the margins of cnt_sleade and cnt_leade cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, the simple lead code cannot be identified. As a result, a frame format error occurs.

The margin must be considered based on the typical value of the specific code type for accurately judging the end bit of the lead code. The margin is about 8% of the type value. For details about the typical values of specific code types, see the values of LEAD_E in Table 14-5 to Table 14-7.

- For the pulse width whose typical values is greater than or equal to 400 (10 μs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example. If the typical value of LEAD_E is 450, the values of cnt_leade_min and cnt_leade_max are calculated as follows:

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cnt_leade_min = 450 x 92% = 414 = 0x19E cnt_leade_max = 450 x 108% = 486 = 0x1E6

- For a pulse width whose typical value is less than 400 (10 μs precision), the recommended margin is 20% of the typical value. Take the SONY-D7C5 code as an example. If the typical value of LEAD_E is 60, the values of cnt_leade_min and cnt_leade_max are calculated as follows:

  cnt_leade_min = 60 x 80% = 48 = 0x030 cnt_leade_max = 60 x 120% = 72 = 0x048

The basic configuration principle is as follows: cnt_leade_max is greater than or equal to cnt_leade_min.

Offset Address	Register Name	Total Reset Value
0x00C	IR_LEADE	0x019E_01E6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt_leade_min								reserved								cnt_leade_max							
Reset	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved.
[24:16]	RW	cnt_leade_min	Minimum pulse width of the end bit of the lead code. 0x000 – 0x007: reserved
[15:9]	-	reserved	Reserved.
[8:0]	RW	cnt_leade_max	Maximum pulse width of the end bit of the lead code. 0x000 – 0x007: reserved

IR_SLEADE

IR_SLEADE is a simple lead code end bit margin configuration register (IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the NEC with simple repeat code, the margins of cnt_sleade and cnt_leade cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, the simple lead code cannot be identified. As a result, a frame format error occurs.
- This register must be configured only for the NEC with simple repeat code.

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The margin must be considered based on the typical value of the specific code type for accurately judging the end bit of the simple lead code. For details about the typical values of specific code types, see the values of SLEAD_E in Table 14-5 to Table 14-7.

- For a pulse width whose typical value is greater than or equal to 225 (10 µs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example. If the typical value of SLEAD_E is 225, the values of cnt_sleade_min and cnt_sleade_max are calculated as follows:
  cnt_sleade_min = 225 x 92% = 207 = 0xCF cnt_sleade_max = 225 x 108% = 243 = 0xF3
- For a pulse width whose typical value is less than 225 (10 µs precision), the recommended margin is 20% of the typical value. For example, if the typical value of SLEAD_E of a code type is 60, the values of cnt_sleade_min and cnt_sleade_max are calculated as follows:
  cnt_sleade_min = 60 x 80% = 48 = 0x30 cnt_sleade_max = 60 x 120% = 72 = 0x48

The basic configuration principle is as follows: cnt_sleade_max is greater than or equal to cnt_sleade_min.

Offset Address	Register Name	Total Reset Value
0x010	IR_SLEADE	0x00CF_00F3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt_sleade_min								reserved								cnt_sleade_max							
Reset	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved.
[24:16]	RW	cnt_sleade_min	Minimum pulse width of the end bit of the simple lead code. 0x000 – 0x007: reserved
[15:9]	-	reserved	Reserved.
[8:0]	RW	cnt_sleade_max	Maximum pulse width of the start bit of the simple lead code. 0x000 – 0x007: reserved

IR_B0

IR_B0 is data 0 level judge margin configuration register (valid only when IR_CFG[ir_mode] = 0).

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CAUTION

- Before setting this register, you must set IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the preceding four code types, the margins for judging the levels of bit0 and bit1 cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, bit1 cannot be identified and is regarded as bit0 by mistake.

A margin must be considered based on the typical value of the specific code type to accurately judging bit0. The margin is about 20% of the typical value.

- For details about the typical values of the NEC with full repeat code, NEC with simple repeat code, and TC9012 code, see the values of B0_H in Table 14-5 to Table 14-7. Take the D6121 code as an example. If the typical value of B0_H is 56 (10 μs precision), the values of cnt0_b_min and cnt0_b_max are calculated as follows:

  cnt0_b_min = 56 x 80% = 45 = 0x2D cnt0_b_max = 56 x 120% = 67 = 0x43
- For details about the typical value of the SONY code, see the values of B0_L in Table 14-5 to Table 14-7. Take the SONY-D7C5 code as an example. If the typical value of B0_L is 60 (10 μs precision), the values of cnt0_b_min and cnt0_b_max are calculated as follows:

  cnt0_b_min = 60 x 80% = 48 = 0x30 cnt0_b_max = 60 x 120% = 72 = 0x48

The basic configuration principle is as follows: cnt0_b_max is greater than or equal to cnt0_b_min.

Offset Address	Register Name	Total Reset Value
0x018	IR_B1	0x0087_00CB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt0_b_min								reserved								cnt0_b_max							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	1

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved.
[24:16]	RW	cnt0_b_min	Minimum pulse width of the level for judging bit0. 0x000 – 0x007: reserved
[15:9]	-	reserved	Reserved.
[8:0]	RW	cnt0_b_max	Maximum pulse width of the level for judging bit0. 0x000 – 0x007: reserved

IR_B1

IR_B1 is data 1 judge level margin configuration register (valid only when IR_CFG[ir_mode] = 0).

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CAUTION

- Before setting this register, you must set IR_BUSY bit[0] to 0 and set IR_EN bit[0] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the preceding four code types, the margins for judging the levels of bit0 and bit1 cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, bit1 cannot be identified and is regarded as bit0 by mistake.

A margin must be considered based on the typical value of the specific code type for accurately judging bit1. The margin is about 20% of the typical value.

- For details about the typical values of the NEC with simple repeat code, NEC with simple repeat code, and TC9012 code, see the values of B1_H in Table 14-5 to Table 14-7. Take the D6121 code as an example. If the typical value of B1_H is 169 (10 μs precision), the values of cnt1_b_min and cnt1_b_max are calculated as follows:

  cnt1_b_min = 169 x 80% = 135 = 0x87 cnt1_b_max = 169 x 120% = 203 = 0xCB
- For details about the typical value of the SONY code, see the values of B1_L in Table 14-5 to Table 14-7. Take the SONY-D7C5 code as an example. If the typical value of B1_L is 120 (10 μs precision), the values of cnt1_b_min and cnt1_b_max are calculated as follows:

  cnt1_b_min = 120 x 80% = 96 = 0x60 cnt1_b_max = 120 x 120% = 144 = 0x90

The basic configuration principle is as follows: cnt1_b_max is greater than or equal to cnt1_b_min.

Offset Address	Register Name	Total Reset Value
0x018	IR_B1	0x0087_00CB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt1_b_min								reserved								cnt1_b_max							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	1

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved.
[24:16]	RW	cnt1_b_min	Minimum pulse width of the level for judging bit1. 0x000 – 0x007: reserved
[15:9]	-	reserved	Reserved.
[8:0]	RW	cnt1_b_max	Maximum pulse width of the level for judging bit1. 0x000 – 0x007: reserved

IR_BUSY

IR_BUSY is a configuration busy flag register.

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Offset Address	Register Name	Total Reset Value
0x01C	IR_BUSY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ir_busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	ir_busy	Busy status flag. 0: idle. In this case, software can configure data. 1: Indicates the busy state. In this state, software cannot configure data.

IR_DATAH

IR_DATAH is an upper 16-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or symbol count register in the symbol FIFO (IR_CFG[ir_mode] = 1)

The IR_DATAH register stores the upper 16 bits of the decoded data received by the IR, whereas IR_DATAL stores the lower 32 bits of the decoded data received by the IR. The data bits depend on the valid data bits in a frame and the specific code. For details, see the valid data bits in Table 14-5 to Table 14-7.

Data is stored as follows: The data is stored in IR_DATAH and IR_DATAL in sequence from MSB to LSB. That is, after IR_DATAL is full, the remaining data is stored in IR_DATAH. The unused upper bits are reserved. Data is read as follows: IR_DATAH and IR_DATAL are read in sequence.

The hardware receives all data bits without checking the definition of each data bit. The software is responsible for processing data bits.

Offset Address	Register Name	Total Reset Value
0x020	IR_DATAH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ir_datah															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.

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[15:0]	RO	ir_datah	Indicates the upper 16 bits of the decoded data received by the IR module when IR_CFG[ir_mode] is 0. Indicates the symbol count in the symbol FIFO when IR_CFG[ir_mode] is 1. bit[15:6]: reserved bit[5:0]: number of symbols in the symbol FIFO.

IR_DATAL

IR_DATAL is a lower 32-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or IR receive symbol width register (IR_CFG[ir_mode] = 1).

Offset Address	Register Name	Total Reset Value
0x024	IR_DATAL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ir_datal																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ir_datal	Indicates the lower 32 bits of the decoded data received by the IR module when IR_CFG[ir_mode] is 0. Indicates the width of the symbol received by the IR module when IR_CFG[ir_mode] is 1. The definitions of bit[31:16] are as follows: Indicates the high-level width (a multiple of 10 μs) of the symbol received by the IR when the symbol level is from low to high. Indicates the low-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from high to low. The definitions of bit[15:0] are as follows: Indicates the low-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from low to high. Indicates the high-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from high to low.

IR_INT_MASK

IR_INT_MASK is an IR interrupt mask register.

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CAUTION

- Before setting this register, you must set IR_EN[ir_en] to 1. Otherwise, the original value of the register is retained after setting.
- If all interrupts are masked, the IR wake-up function is unavailable.
- When IR_CFG[ir_mode] is 0, IR_INT_MASK bit[3:0] are valid; when IR_CFG[ir_mode] is 1, IR_INT_MASK bit[18:16] are valid.

The definitions of the interrupts related to the register are as follows:

- Receive data overflow interrupt

  If the CPU does not fetch the current frame and the next frame is already received, the next frame overwrites the current frame and a raw receive data overflow error interrupt is reported.
- Receive data frame format error interrupt

  If the received data frame is not complete or the data pulse width does not meet the margin requirements, a raw receive frame format error interrupt is reported.
- Receive data frame interrupt

  After a complete frame data is received, a raw receive data frame interrupt is reported.
- Key release detection interrupt

  For the NEC with simple repeat code and TC9012 code, if the start synchronous code is not detected again within 160 ms after the previously detected start synchronous code, or a valid data frame rather than a simple lead code is detected, a raw key release detection interrupt is reported. Both the NEC with full repeat code and the SONY code do not support the key release detection interrupt.
- Receive symbol overflow interrupt

  If the symbol FIFO is full because the CPU does not fetch the data in time and the subsequent symbol is already received, a raw receive symbol overflow error interrupt is reported.
- Receive symbol interrupt

  If a complete symbol is received and the symbol count of the symbol FIFO is above the threshold configured by IR_CFG[ir_bits], a raw receive symbol interrupt is reported.
- Symbol timeout interrupt

  If no new symbol interrupt is received during the period configured by IR_CFG[ir_max_level_width] after a valid symbol is received, a raw symbol timeout interrupt is reported.

The hardware does not identify the interrupt priority. An interrupt is generated if one or more masked interrupt sources are valid.

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Offset Address	Register Name	Total Reset Value
0x028	IR_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													intm_overrun	intm_time_out	intm_symb_rcv	reserved												intm_release	intm_overflow	intm_framerr	intm_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	-	reserved	Reserved.
[18]	RW	intm_overrun	Symbol overflow interrupt mask when IR_CFG[ir_mode] is 1. 0: not masked 1: masked
[17]	RW	intm_time_out	Symbol timeout interrupt mask when IR_CFG[ir_mode] is 1. 0: not masked 1: masked
[16]	RW	intm_symb_rcv	Receive N symbol interrupt mask when IR_CFG[ir_mode] is 1. 0: not masked 1: masked
[15:4]	-	reserved	Reserved.
[3]	RW	intm_release	Key release interrupt mask when IR_CFG[ir_mode] is 0. 0: not masked 1: masked
[2]	RW	intm_overflow	Receive data overflow interrupt mask when IR_CFG[ir_mode] is 0. 0: not masked 1: masked
[1]	RW	intm_framerr	Receive data frame format error interrupt mask when IR_CFG[ir_mode] is 0. 0: not masked 1: masked
[0]	RW	intm_rcv	Receive data frame interrupt mask when IR_CFG[ir_mode] is 0. 0: not masked 1: masked

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IR_INT_STATUS

IR_INT_STATUS is an IR interrupt status register.

CAUTION

- When IR_CFG[ir_mode] is 0, IR_INT_STATUS bit[3:0] and IR_INT_STATUS bit[19:16] are valid.
- When IR_CFG[ir_mode] is 1, IR_INT_STATUS bit[10:8] and IR_INT_STATUS bit[26:24] are valid.

Offset Address	Register Name	Total Reset Value
0x02C	IR_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					intms_overrun	intms_time_out	intms_symb_rcv	reserved				intms_release	intms_overflow	intms_framerr	intms_rcv	reserved					intrs_overrun	intrs_time_out	intrs_symb_rcv	reserved				intrs_release	intrs_overflow	intrs_framerr	intrs_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved.
[26]	RO	intms_overrun	Masked symbol overflow interrupt status when IR_CFG[ir_mode] is 1. 0: No interrupt is generated. 1: An interrupt is generated.
[25]	RO	intms_time_out	Masked symbol timeout interrupt status when IR_CFG[ir_mode] is 1. 0: No interrupt is generated. 1: An interrupt is generated.
[24]	RO	intms_symb_rcv	Masked receive symbol interrupt status when IR_CFG[ir_mode] is 1. 0: No interrupt is generated. 1: An interrupt is generated.
[23:20]	-	reserved	Reserved.
[19]	RO	intms_release	Masked key release interrupt status when IR_CFG[ir_mode] is 0. 0: No interrupt is generated. 1: An interrupt is generated.

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[18]	RO	intms_overflow	Masked receive data overflow error interrupt status when IR_CFG[ir_mode] is 0. 0: No interrupt is generated. 1: An interrupt is generated.
[17]	RO	intms_framerr	Masked receive data frame format error interrupt status when IR_CFG[ir_mode] is 0. 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RO	intms_rcv	Masked receive data frame interrupt status when IR_CFG[ir_mode] is 0. 0: No interrupt is generated. 1: An interrupt is generated.
[15:11]	-	reserved	Reserved.
[10]	RO	intrs_overrun	Raw symbol overflow interrupt status when IR_CFG[ir_mode] is 1. 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	intrs_time_out	Raw symbol timeout interrupt status when IR_CFG[ir_mode] is 1. 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	intrs_symb_rcv	Raw receive symbol interrupt status when IR_CFG[ir_mode] is 1. 0: No interrupt is generated. 1: An interrupt is generated.
[7:4]	-	reserved	Reserved.
[3]	RO	intrs_release	Raw key release interrupt status when IR_CFG[ir_mode] is 0. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	intrs_overflow	Raw receive data overflow error interrupt status when IR_CFG[ir_mode] is 0. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	intrs_framerr	Raw receive data frame format error interrupt status when IR_CFG[ir_mode] is 0. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	intrs_rcv	Raw receive data frame interrupt status when IR_CFG[ir_mode] is 0. 0: No interrupt is generated. 1: An interrupt is generated.

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IR_INT_CLR

IR_INT_CLR is an IR interrupt clear register.

CAUTION

- When IR_CFG[ir_mode] is 0, IR_INT_CLR bit[3:0] are valid.
- When IR_CFG [ir_mode] is 1, IR_INT_CLR bit[18:16] are valid.

Offset Address	Register Name	Total Reset Value
0x030	IR_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													intc_overrun	intc_time_out	intc_symb_rcv	reserved												intc_release	intc_overflow	intc_framerr	intc_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	-	reserved	Reserved.
[18]	WC	intc_overrun	When IR_CFG[ir_mode] is 1, this bit indicates whether the symbol overflow interrupt request is cleared. 0: no effect 1: cleared
[17]	WC	intc_time_out	When IR_CFG[ir_mode] is 1, this bit indicates whether the symbol timeout interrupt request is cleared. 0: no effect 1: cleared
[16]	WC	intc_symb_rcv	When IR_CFG[ir_mode] is 1, this bit indicates whether the receive symbol interrupt request is cleared. 0: no effect 1: cleared
[15:4]	-	reserved	Reserved.
[3]	WC	intc_release	When IR_CFG[ir_mode] is 0, this bit indicates whether the key release interrupt request is cleared. 0: no effect 1: cleared

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[2]	WC	intc_overflow	When IR_CFG[ir_mode] is 0, this bit indicates whether the receive data overflow error interrupt request is cleared. 0: no effect 1: cleared
[1]	WC	intc_framerr	When IR_CFG[ir_mode] is 0, this bit indicates whether the receive data frame format error interrupt request is cleared. 0: no effect 1: cleared
[0]	WC	intc_rcv	When IR_CFG[ir_mode] is 0, this bit indicates whether the receive data frame interrupt request is cleared. 0: no effect 1: cleared If a receive data frame interrupt is generated and the software writes 1 to the bit without reading the data in IR_DATAL, the interrupt cannot be cleared.

IR_START

IR_START is an IR start configuration register.

After other registers are configured, IR_START can be started when any value is written to the corresponding address during the startup of the IR module.

Offset Address	Register Name	Total Reset Value
0x034	IR_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ir_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	WO	ir_start	IR start configuration register.

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14.5 GPIO

14.5.1 Overview

The Hi3521 supports 15 groups of general purpose input/output (GPIO) pins. Each group of GPIO pins provides eight programmable input/output pins except that group 15 provides only six programmable input/output pins. Each pin can be configured as input or output and these pins are used to generate input signals or output signals for special purposes. As input, each GPIO pin can act as an interrupt source; as output, each GPIO pin can be set to 0 or 1 separately.

CAUTION

For details about the number of GPIO pins and multiplexing relationship between GPIO pins and other pins, see Chapter 2 "Hardware." For details about control modes, see section 2.1.5 "Description of Multiplexing Registers".

For the multiplexed GPIO pins that are output by default, note that the pins that connect to the chip and the components must be input.

14.5.2 Features

The GPIO module has the following features:

- Each GPIO pin can be configured as input or output.
  - As input, each GPIO pin can act as an interrupt source, that is, each GPIO pin can be controlled by an interrupt separately.
  - As output, each GPIO can be set to 0 or 1 separately.
- The GPIO interrupts are controlled by using seven registers such as GPIO_IS. These registers enable you to select the interrupt source, interrupt edge (falling edge or rising edge), and interrupt trigger modes (level-sensitive mode or edge-sensitive mode). For details about the corresponding interrupt registers of GPIO pins, see section 3.3 "Interrupt System."
  - When multiple interrupts occur at the same time, these interrupts are combined as one interrupt to report. For details about the GPIO interrupt mapping, see section 3.3 "Interrupt System".
  - The GPIO_IS, GPIO_IBE, and GPIO_IEV registers determine the features of the interrupt source and interrupt trigger type.

  GPIO_RIS and GPIO_MIS are used to read the raw interrupt status and masked interrupt status respectively. GPIO_IE controls the final report status of each interrupt. In addition, GPIO_IC is provided to clear the interrupt status separately.

14.5.3 Function Description

Each group of GPIO pins consist of eight programmable I/O pins. Each pin can be configured as input or output and these pins are used to generate input signals or output signals for special purposes.

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The GPIO module can generate maskable interrupts based on the level or transition value. The general purpose input output interrupt (GPIOINTR) informs the interrupt controller of the occurrence of interrupts.

14.5.4 Operating Mode

Interface Reset

During power-on reset, all registers are cleared, and therefore the pins work as input pins by default.

When the reset signal is valid, the status of the GPIO is as follows:

- The interrupt becomes invalid after the corresponding bit of GPIO_IE is cleared.
- All registers are cleared.
- All pins are configured as input.
- The raw interrupt register is cleared.
- The triggering mode of the interrupt is set to edge-sensitive.

GPIO

Each pin can be configured as input or output. To configure a GPIO pin, perform the following steps:

Step 1 Enable the required GPIO pins by configuring corresponding pins according to the description of IO_CONFIG.Configure the GPIO as input or output by using the GPIO_DIR register.

- As input: The external signals are transmitted through the GPIO pin. In this case, the values of the input signals can be viewed by checking the GPIO_DATA register.

  Note: The input signals are also transmitted to the pins that are multiplexed with the GPIO pins.
- As output: The values are written to the GPIO_DATA register and output by using the GPIO in sequence.

NOTE
If the GPIO interrupt function is enabled, an interrupt is generated when the output signal meets the triggering condition.

---End

Interrupt Operation

To generate an interrupt rather than a pseudo interrupt, perform the following steps:

Step 1 Select the edge-sensitive mode or level-sensitive mode by configuring the GPIO_IS register.

Step 2 Select the falling-/rising-edge-sensitive mode or high-/low-level-sensitive mode by configuring the GPIO_IEV register.

Step 3 If the edge-sensitive mode is selected, select single-edge-sensitive mode or dual-edge-sensitive mode by configuring the GPIO_IBE register.

Ensure that the GPIO data lines are stable during preceding operations.

Step 4 Write 0xFF to the GPIO_IC register to clear the interrupt.

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Step 5 Set the GPIO_IE to 1 to enable the interrupt.

---End

The GPIO interrupts are controlled by seven registers. When one or more GPIO pins generate interrupts, a combined interrupt is output to the interrupt controller. The differences between the edge-sensitive mode and level-sensitive mode are as follows:

- Edge-sensitive mode: Software must clear this interrupt to enable superior interrupts.
- Level-sensitive mode: The external interrupt source must keep this level until the processor identifies this interrupt.

14.5.5 Register Summary

Table 14-9 lists the base addresses of 15 groups of GPIO registers.

Table 14-9 Base addresses of 15 groups of GPIO registers

Register	Base Address
GPIO14	0x2023_0000
GPIO13	0x2022_0000
GPIO12	0x2021_0000
GPIO11	0x2020_0000
GPIO10	0x201F_0000
GPIO9	0x201E_0000
GPIO8	0x201D_0000
GPIO7	0x201C_0000
GPIO6	0x201B_0000
GPIO5	0x201A_0000
GPIO4	0x2019_0000
GPIO3	0x2018_0000
GPIO2	0x2017_0000
GPIO1	0x2016_0000
GPIO0	0x2015_0000

Table 14-10 describes the offset addresses and definitions of a group of internal GPIO registers. GPIO0 to GPIO14 also have the same internal GPIO registers.

NOTE

- Register address of GPIOn = GPIOn base address + Offset address of the register
- The value of n ranges from 0 to 18.

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Table 14-10 Summary of GPIO registers

Offset Address	Register	Description	Page
0x000 – 0x3FC	GPIO_DATA	GPIO data register	14-83
0x400	GPIO_DIR	GPIO direction control register	14-84
0x404	GPIO_IS	GPIO interrupt trigger register	14-85
0x408	GPIO_IBE	GPIO interrupt dual-edge trigger register	14-85
0x40C	GPIO_IEV	GPIO interrupt trigger event register	14-86
0x410	GPIO_IE	GPIO interrupt mask register	14-86
0x414	GPIO_RIS	GPIO raw interrupt status register	14-87
0x418	GPIO_MIS	GPIO masked interrupt status register	14-87
0x41C	GPIO_IC	GPIO interrupt clear register	14-88

14.5.6 Register Description

GPIO_DATA

GPIO_DATA is a GPIO data register. It is used to buffer the input or output data.

When the corresponding bit of the GPIO_DIR is configured as output, the values written to the GPIO_DATA register are sent to the corresponding pin (note that the pin multiplexing configuration must be correct). If the bit is configured as input, the value of the corresponding input pin is read.

CAUTION

If the corresponding bit of GPIO_DIR is configured as input, the pin value is returned after a valid read; if the corresponding bit is configured as output, the written value is returned after a valid read.

Through PADDR[9:2], the GPIO_DATA register masks the read and write operations on the register. The register corresponds to 256 address spaces. PADDR[9:2] corresponds to GPIO_DATA[7:0]. When the corresponding bit is high, it can be read or written. When the corresponding bit is low, no operations are supported. For example,

- If the address is 0x3FC (0b11_1111_1100), the operations on all the eight bits of GPIO_DATA[7:0] are valid.
- If the address is 0x200 (0b10_0000_0000), only the operation on GPIO_DATA[7] is valid.

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Offset Address	Register Name	Total Reset Value
0x000 – 0x3FC	GPIO_DATA	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_data							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_data	Indicates the GPIO input data when the GPIO is configured as input; indicates the GPIO output data when the GPIO is configured as output. Each bit can be controlled separately. The register is used together with GPIO_DIR.

GPIO_DIR

GPIO_DIR is a GPIO direction control register. It is used to configure the direction of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x400	GPIO_DIR	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_dir							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_dir	GPIO direction control register. Bit[7:0] correspond to GPIO_DATA [7:0] respectively. Each bit can be controlled separately. 0: input 1: output

GPIO_IS

GPIO_IS is a GPIO interrupt trigger register. It is used to configure the interrupt trigger mode.

Offset Address	Register Name	Total Reset Value
0x404	GPIO_IS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_is							

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Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_is	GPIO interrupt trigger control register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: edge-sensitive mode 1: level-sensitive mode

GPIO_IBE

GPIO_IBE is a GPIO interrupt dual-edge trigger register. It is used to configure the edge trigger mode of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x408	GPIO_IBE	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ibe							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_ibe	GPIO interrupt edge control register. Bit[7:0] correspond to GPIO_DATA [7:0] respectively. Each bit is controlled independently. 0: single-edge-sensitive mode. The GPIO_IEV register controls whether the interrupt is rising-edge-sensitive or falling-edge-sensitive. 1: dual-edge-sensitive mode

GPIO_IEV

GPIO_IEV is a GPIO interrupt event register. It is used to configure the interrupt trigger event of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x40C	GPIO_IEV	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_iev							

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Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_iev	GPIO interrupt trigger event register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: falling-edge-sensitive mode or low-level-sensitive mode 1: rising-edge-sensitive mode or high-level-sensitive mode.

GPIO_IE

GPIO_IE is a GPIO interrupt mask register. It is used to mask GPIO interrupts.

Offset Address	Register Name	Total Reset Value
0x410	GPIO_IE	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ie							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_ie	GPIO interrupt mask register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: masked 1: not masked

GPIO_RIS

GPIO_RIS is a GPIO raw interrupt status register. It is used to query the raw interrupt status of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x414	GPIO_RIS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ris							

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Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	gpio_ris	GPIO raw interrupt status register. Bit[7:0] correspond to GPIO_DATA [7:0], indicating the unmasked interrupt status. The status cannot be masked and controlled by the GPIO_IE register. 0: An interrupt is generated. 1: No interrupt occurs.

GPIO_MIS

GPIO_MIS is a GPIO masked interrupt status register. It is used to query the masked interrupt status of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x418	GPIO_MIS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_mis							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	gpio_mis	GPIO masked interrupt status register. Bit[7:0] correspond to GPIO_DATA [7:0], indicating the masked interrupt status. The status is controlled by the GPIO_IE register. 0: The interrupt is invalid. 1: The interrupt is valid.

GPIO_IC

GPIO_IC is a GPIO interrupt clear register. It is used to clear the interrupts generated by GPIO pins and clear the GPIO_RIS and GPIO_MIS registers.

Offset Address	Register Name	Total Reset Value
0x41C	GPIO_IC	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ic							

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Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	WC	gpio_ic	GPIO interrupt clear register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: no effect 1: cleared

14.6 USB 2.0 Host

14.6.1 Overview

The USB 2.0 host controller supports the high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) data transfer modes. It fully complies with the USB 2.0, open host controller interface (OHCI) V1.0a, and enhanced host controller interface (EHCI) V1.0 protocols. The USB 2.0 host controller has a root hub. As a part of the USB system, the root hub is used to extend the USB port. By using most hardware logic in the controller, the following functions are achieved:

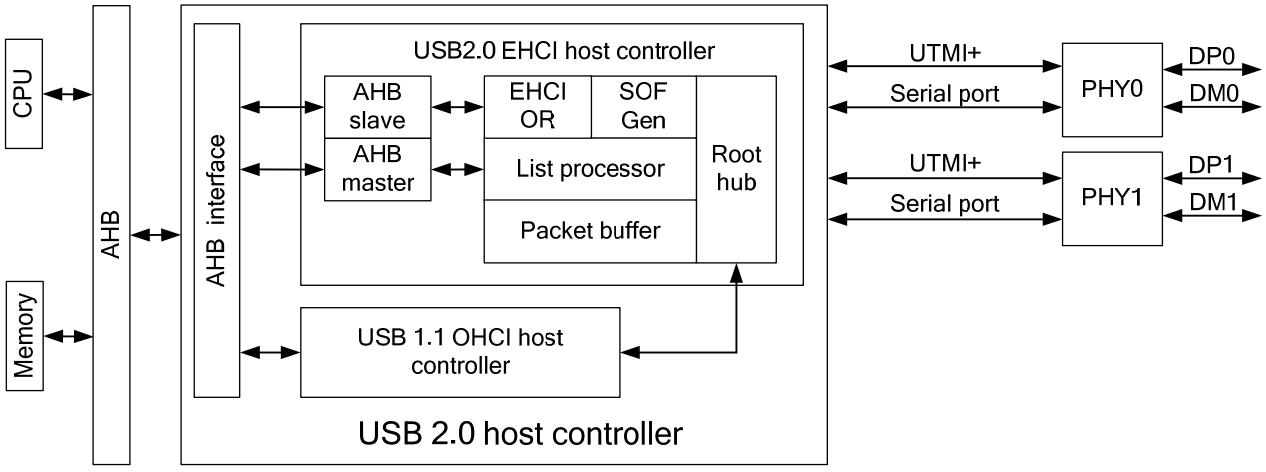
- Controls and processes data transfer.
- Parses data packets and packages data.
- Encodes and decodes the signals transmitted through the USB port.
- Provide interfaces (such as the interrupt vector interface) for the driver.

14.6.2 Function Description

Logic Block Diagram

Figure 14-40 shows the logic block diagram of the USB 2.0 host controller.

Figure 14-40 Logic block diagram of the USB 2.0 host controller



UTMI: USB2.0 Transceiver Macrocell Interface

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EHCI: Enhanced Host Controller Interface
OHCI: Open Host Controller Interface

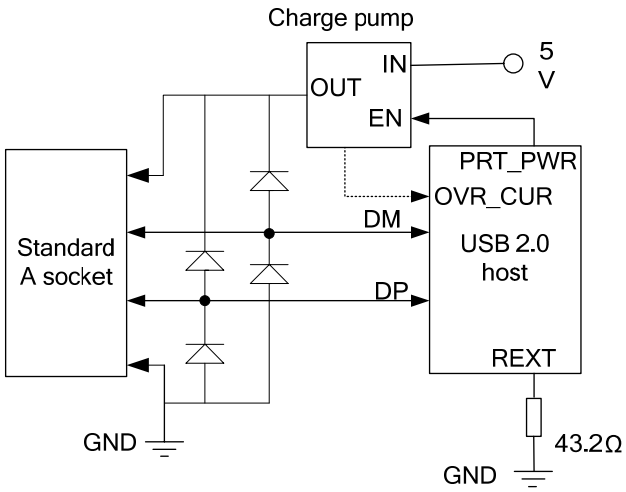
Typical Application

Figure 14-41 shows the reference design of the USB 2.0 host controller.

CAUTION

- The impedance of DP or DM is 45 Ω ±1% and no extra matched resistors are required.
- The REXT resistor is a ±1% resistor.
- If high-speed electro static discharge (ESD) components are used, 1 pF capacitors are recommended.

Figure 14-41 Reference design of the USB 2.0 host controller



Functions

The USB 2.0 host controller has the following features:

- Fully compatible with USB 2.0.
- Complies with OHCI V1.0a and EHCI V1.0 protocols.
- Supports high-speed, full-speed, and low-speed devices.
- Supports low-power solutions.
- Supports four basic data transfer modes including control transfer, bulk transfer, isochronous transfer, and interrupt transfer.
- Supports a maximum of 127 devices by using USB hubs

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Working Principle

The USB 2.0 host controller supports the following four standard transfer modes:

- Control transfer

  This mode is applicable to the data transfer between endpoints 0 of USB host and the USB device. For the USB devices of specific models, other endpoints may be used. The control transfer is bidirectional and the transferred data amount is small. Depending on the device and transfer speed, 8-byte data, 16-byte data, 32-byte data, or 64-byte data can be transferred.

- Bulk transfer

  This mode is applicable to the data transfer in bulk when there is no limit on the bandwidth and time interval. This mode is the best choice when the transfer speed is very low and multiple data transfers are delayed. In this case, bulk transfer is performed after all other types of data transfers are complete. In the bulk transfer mode, data is transferred between the USB host and USB device without errors by using the error detection and retransmission mechanism.

- Isochronous transfer

  This mode is applicable to the stream data transfer with strict time requirements and strong error tolerance or the instant data transfer at a constant transfer rate. This mode provides a fixed bandwidth and time interval.

- Interrupt transfer

  This mode is applicable to the data transfer when the data is scattered, unpredictable, and is of small volume. In this mode, the device is checked whether there is interrupt data to be sent at a fixed interval. The query frequency ranges from 1 ms to 255 ms and it depends on the device endpoint mode. The typical interrupt transfer mode is unidirectional and only input is available for the USB host.

14.6.3 Operating Mode

Pin Polarity Control

The valid polarity of USB0_PWREN and USB1_PWREN can be configured by setting PERIPHCTRL20 [usbpwr_p_ctrl]. For details, see the description of PERIPHCTRL20 [usbpwr_p_ctrl] in section 3.4.5 "Register Description."

Clock Gating

If the USB 2.0 host controller is not used, its clock can be disabled to reduce power consumption.

To disable the clock, perform the following steps:

Step 1 Write 1 to PERI_CRG46 [usbphy_port0_treq], PERI_CRG46[usbphy_port1_treq], PERI_CRG46[usbphy_req], PERI_CRG46[usb_ctrl_utmi0_req], PERI_CRG46[usb_ctrl_utmi1_req], PERI_CRG46[usb_ctrl_hub_req], and PERI_CRG46[usb_ahb_srst_req] respectively to reset the USB controller and PHY.

Step 2 Set PERI_CRG46 [usb_cken] to 0 to disable the clocks of the USB 2.0 host controller.

---End

To enable the clocks, perform the following steps:

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Step 1 Set PERI_CRG46 [usb_cken] to 1 to enable the clocks of the USB 2.0 host controller.

Step 2 Deassert the reset on the USB controller and PHY. For details, see "Reset Clear."

---End

Reset Deassert

By default, the USB controller and PHY are reset after power-on. To deassert reset, perform the following steps:

Step 1 Delay at least 10 μs.

Step 2 Write 0 to PERI_CRG46[usbphy_port0_treq] to deassert the soft reset on USB PHY port0; write 0 to PERI_CRG46[usbphy_port1_treq] to deassert the soft reset on USB PHY port1.

Step 3 Write 0 to PERI_CRG46[usbphy_req] to deassert the reset on the USB PHY.

Step 4 After 250 μs delay, write 0 to PERI_CRG46[usb_ctrl_utmi0_req] to deassert the soft reset on USB controller port0; write 0 to CRG46[usb_ctrl_utmi1_req] to deassert the soft reset on USB controller port1; write 0 to PERI_CRG46[usb_ctrl_hub_req] to deassert the soft reset on the hub of the USB controller.

Step 5 Write 0 to PERI_CRG46[usb_ahb_srst_req] to deassert the soft reset on the USB bus.

---End

Separately Resetting Port0 or Port1 During the Working Process

To reset port0 separately during the working process, perform the following steps:

Step 1 Write 1 to PERI_CRG46[usb_ctrl_utmi0_req] to soft-reset port0 of the USB controller.

Step 2 Write 1 to PERI_CRG46[usbphy_port0_treq] to soft-reset port0 of the USB PHY.

Step 3 After 200 μs delay, write 0 to PERI_CRG46[usbphy_port0_treq] to deassert the reset on port0 of the USB PHY.

Step 4 Write 0 to PERI_CRG46[usb_ctrl_utmi0_req] to deassert the reset on port0 of the USB controller.

---End

To reset port1 separately during the working process, perform the following steps:

Step 1 Write 1 to PERI_CRG46[usb_ctrl_utmi1_req] to soft-reset port1 of the USB controller.

Step 2 Write 1 to PERI_CRG46[usbphy_port1_treq] to soft-reset port1 of the USB PHY.

Step 3 After 200 μs delay, write 0 to PERI_CRG46[usbphy_port1_treq] to deassert the reset on port1 of the USB PHY.

Step 4 Write 0 to PERI_CRG46[usb_ctrl_utmi1_req] to deassert the reset on port1 of the USB controller.

---End

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Suspend and Resume

Suspending PHY 0: Port0 enters the suspend mode after software sets the system mode to suspend mode by using the EHCI and OHCI registers.

Resuming port0: After the software sets the system mode to another mode rather than suspend mode by using the EHCI and OHCI registers, if PERI_USB1 [COMMONONN] is 1, the software can initiate a USB operation at least 225 μs later; if PERIPHCTRL21 [commononn] is 0, the software can initiate a USB operation at least 5 μs later.

NOTE

The operations of suspending or resuming port0 are similar to those of suspending or resuming port1.

Adjusting the Quality of the USB TX Signal

If the USB eye pattern on the board does not meet the requirements of the template defined by the USB protocol, you can adjust the quality of the USB TX signal.

The following is an example using USB port0. Perform the following steps:

Step 1 Write 1 to PERIPHCTRL21[phy0_txpreemphasistune] to enable the preemphasis function of USB port0.

Step 2 Write 1 to PERIPHCTRL21[phy0_txrisetune] to reduce the up or down time of high-speed signals.

Step 3 Write 1111 to PERIPHCTRL21[phy0_txverftune] to increase the DC level.

---End

NOTE

If the USB eye pattern on the board does not meet the requirements of the template defined by the USB protocol, ensure that the preceding registers are configured.

14.6.4 Register Summary

NOTE

The USB module is a standard USB 2.0 host controller and the internal registers are standard EHCI and OHCI registers. For details, see the EHCI and OHCI protocols. The following section describes the registers that are specially defined only by some vendors.

Table 14-11 describes the USB registers.

Table 14-11 Summary of USB registers (base address: 0x100B_0000)

Offset Address	Register	Description	Page
0x90	INTNREG00	Micro-frame length configuration register	14-93
0x94	RESERVED	Reserved	-
0x98	RESERVED	Reserved	-
0x9C	RESERVED	Reserved	-
0xA0	INTNREG04	Debug register	14-94

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Offset Address	Register	Description	Page
0xA4	INTNREG05	Control and status register	14-95
0xA8	INTNREG06	AHB error status register	14-96
0xAC	INTNREG07	AHB error address register	14-96

NOTE

The base address of the EHCI register is 0x100B_0000 and the base address of the OHCI register is 0x100A_0000. The base address of Table 14-11 is that of the EHCI register.

14.6.5 Register Description

INTNREG00

INTNREG00 is a micro-frame length configuration register.

Offset Address	Register Name	Total Reset Value
0x90	INTNREG00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				val											en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	-	reserved	Reserved.
[13:1]	RW	val	Value of the micro-frame counter. This register is used only for emulation. In normal mode, the micro-frame length is 125 μs defined by the protocol. During emulation, you can change the micro-frame length by configuring this register as required to reduce the emulation time.
[0]	RW	en	Register enable. 0: disabled 1: enabled

INTNREG04

INTNREG04 is a debug register.

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Offset Address	Register Name	Total Reset Value
0xA0	INTNREG04	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										auto_en	nak_reldfix_en	reserved	scaledwn_enum_time	hccparam_en	hcsparam_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	-	reserved	Reserved.
[5]	RW	auto_en	Automatic feature enable. 0: enabled. The suspend signal is valid when the run/stop bit is reset by software, but the hchalted bit is not set. 1: disabled. The port is not suspended when software clears the run/stop bit. The default value is 0.
[4]	RW	nak_reldfix_en	NAK reload enable. 0: enabled 1: disabled
[3]	-	reserved	Reserved.
[2]	RW	scaledwn_enum_time	Port enumeration time scale down enable. 0: disabled 1: enabled
[1]	RW	hccparam_en	HCCPARAMS register write enable. 0: disabled 1: enabled
[0]	RW	hcsparam_en	HCSPARAMS register write enable. 0: disabled 1: enabled

INTNREG05

INTNREG05 is a control and status register. It is used to read or write to the PHY.

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Offset Address	Register Name	Total Reset Value
0xA4	INTNREG05	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														vbusy		vport			vcontrol_loadm	vcontrol				vstatus							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	-	reserved	Reserved.
[17]	RO	vbusy	The value 1 indicates that the hardware is writing data. This bit is cleared only when the process ends.
[16:13]	RW	vport	Port ID. It cannot exceed the supported number of ports.
[12]	RW	vcontrol_loadm	Load enable. 0: enabled 1: disabled
[11:8]	RW	vcontrol	Port control signal.
[7:0]	RO	vstatus	Port status signal.

INTNREG06

INTNREG06 is an AHB error status register.

Offset Address	Register Name	Total Reset Value
0xA8	INTNREG06	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_capture	reserved																			hbusrt_err			num_beat_err				num_beat_ok				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	err_capture	AHB error.
[30:12]	-	reserved	Reserved.
[11:9]	RO	hbusrt_err	hbrust value during a control transfer when an AHB error occurs.

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[8:4]	RO	num_beat_err	Number of beats during a burst transfer when an AHB error occurs. The maximum number of beats is 16. 0x00 – 0x10: valid 0x11 – 0x1F: reserved
[3:0]	RO	num_beat_ok	Number of completed beats during a burst transfer when an AHB error occurs.

INTNREG07

INTNREG07 is an AHB error address register.

Offset Address	Register Name	Total Reset Value
0xAC	INTNREG07	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	err_addr	Address during a control transfer when an AHB error occurs.

14.7 MMC/SD/SDIO Controller

14.7.1 Function Description

Functional Block Diagram

The MMC/SD/SDIO controller (MMC controller for short) controls the read/write operations on the secure digital (SD) card and multimedia card (MMC), and supports various extended devices such as Bluetooth and Wi-Fi devices based on the secure digital input/output (SDIO) protocol. The Hi3521 provides one MMC controller for controlling the SD card, MMC, and SDIO device.

The MMC controller can control the devices that comply with the following protocols:

- Secure Digital Memory (SD mem – version 2.00)
- Secure Digital I/O (SDIO – version 2.0)
- MultiMediaCard (MMC – version 4.3)

Figure 14-42 shows the functional block diagram of the MMC controller.

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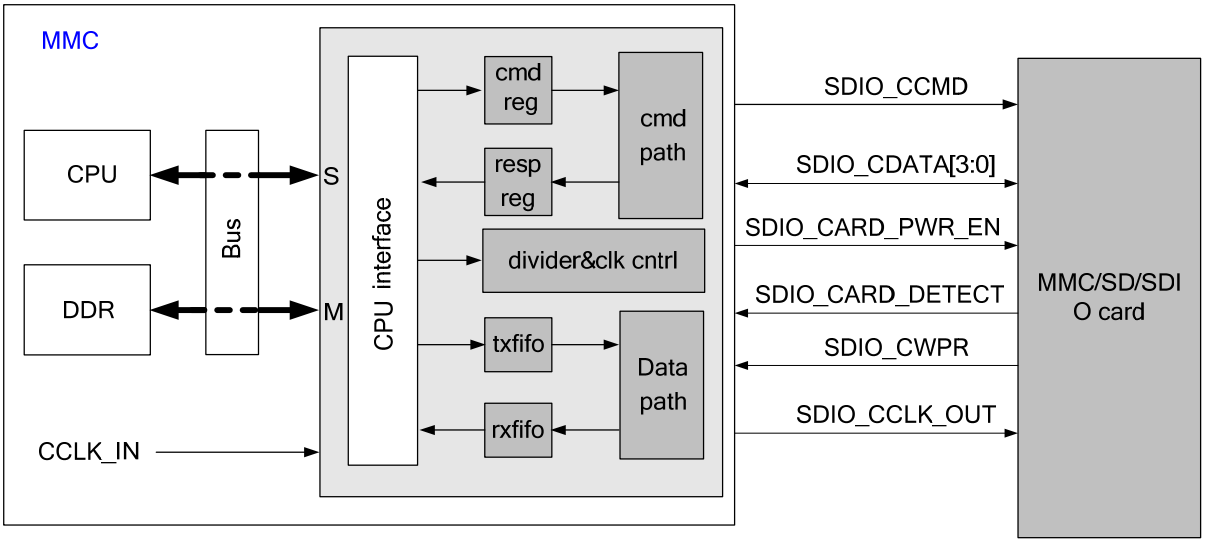
Figure 14-42 Functional block diagram of the MMC controller



NOTE

S indicates slave interface and M indicates master interface.

Connected to the system through the internal bus, the MMC controller consists of the following parts:

- Command path

  It is used to transmit commands and receive responses.
- Data path

  It is used to perform data read and write operations by working with the command path.
- Interface clock control unit

  It is used to change the frequency of the interface clock as required and enable or disable the interface clock. SDIO_CLK_OUT can be generated by dividing CCLK_IN.

The MMC controller has the following features:

- Transfers data by using the internal direct memory access controller (IDMAC).
- Supports one transmit FIFO and one receive FIFO. The depth of each FIFO is 256 words.
- Supports configurable burst size during DMA transfer and configurable FIFO threshold.
- Supports FIFO overflow and underflow interrupts to avoid errors during data transfer.
- Supports the cyclic redundancy check (CRC) generation and check for data and commands.
- Supports programmable frequency of the interface clock.
- Disables the MMC clock and interface clock in low-power mode.
- Supports 1-bit, 4-bit, or 8-bit data width based on the connected component.
- Reads or writes data blocks with the size of 1 byte to 65,535 bytes.
- Reads/writes stream data from/to the MMC card.
- Supports the suspend operation, resume operation, and read wait operation on the SDIO card.

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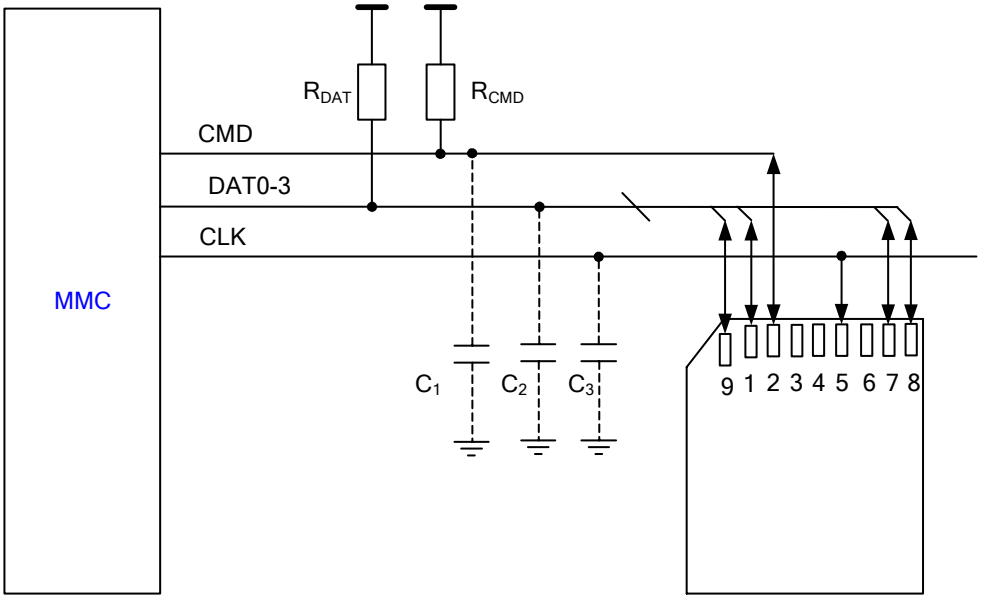
Typical Application

Figure 14-43 shows the typical application circuit of the MMC controller.

Figure 14-43 Typical application circuit of the MMC controller



The MMC controller exchanges commands and data with the connected card over a clock signal line, a bidirectional command signal line, and four bidirectional data signal lines. Both the command signal line and data signal lines work in pull-up mode. Table 14-12 describes the pull-up resistors and the load capacitance of each signal line.

Table 14-12 Load parameters of signal lines

Parameter	Min	Max	Description
R_{DAT} R_{CMD}	10 kΩ	100 kΩ	Pull-up resistors
Load capacitance Cx	None	30 pF	$C_x = C_{mmchost} + C_{bus} + C_{card}$The maximum capacitance of each card (C_{card}) is 10 pF; therefore, the sum of $C_{mmchost}$ and C_{bus} must be less than 30 pF.
Inductance of each signal line	None	16 nH	Fpp ≤ 20 MHz

CAUTION

Besides the signal lines in Figure 14-34, the card slot also provides the mechanical write protection signal and card detection signal. However, the signal interfaces are not provided in Figure 14-34.

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Commands and Responses

All interactions between the MMC controller and the card, including initializing the card, reading/writing to registers, querying the status, and transferring data, are implemented by using commands.

A MMC command is a segment of 48-bit serial data consisting of a start bit, a transmission bit, a command sequence, a CRC bit, and an end bit. After receiving a command, the card returns a 48-bit or a 136-bit response based on the command type.

Figure 14-44 Format of an MMC command

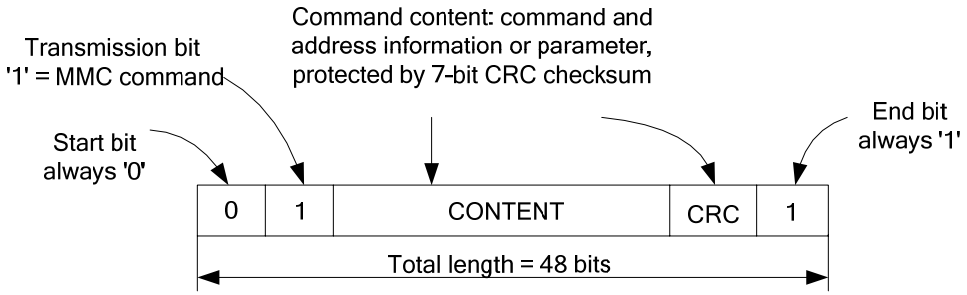
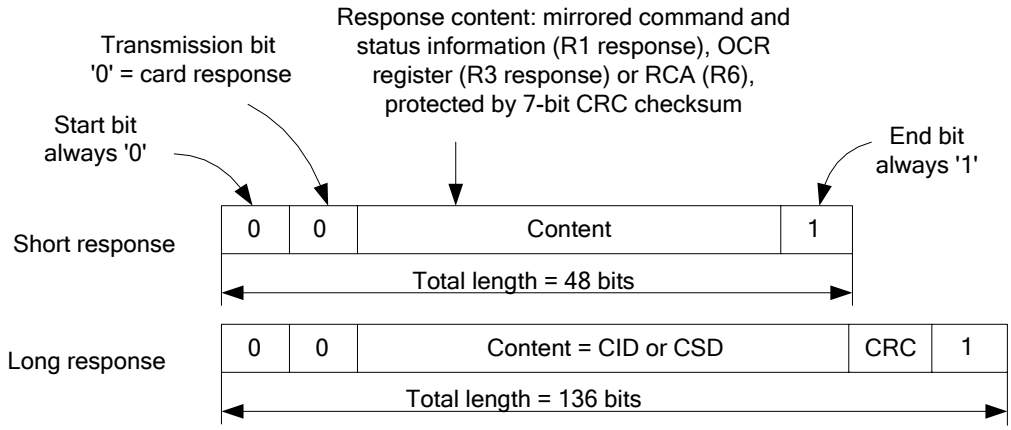


Figure 14-45 Format of the response to an MMC command



Commands are classified into the following two types based on whether data is transferred:

- Non-data transfer command

  The MMC controller transmits/receives commands to/from the card through the command signal line.
- Data transfer command

  Besides the interaction on the command line, data is also transferred through the data lines DAT0 to DAT7.

(1) Non-data transfer command

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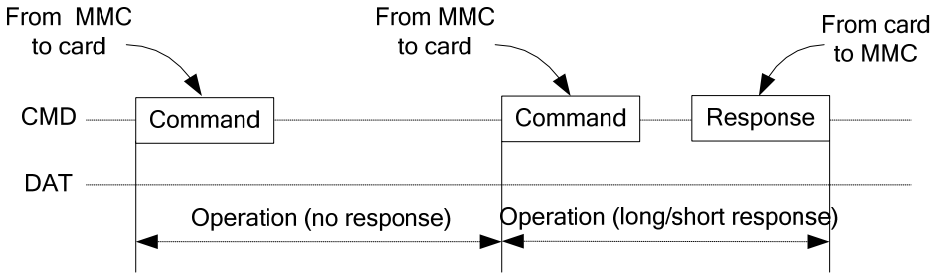
Figure 14-46 shows the operations between the MMC controller and the card by running a non-data transfer command.

Figure 14-46 Operations by running an MMC non-data transfer command



(2) Data transfer command

The MMC supports the following data transfer commands:

- Stream data read/write command

  Only the MMC card supports the stream data read/write command. In this case, only the data line DAT0 is used for data transfer, and no CRC check is performed.
- Single-block read/write command

  After this command is executed, one single data block is read and written each time. No stop command is required for stopping each data transfer.
- Multi-block read/write command
  - Predefined block count mode

    Before the multi-block read/write command is executed, the block count command is transmitted to specify the number of data blocks to be transferred.
  - Open-ended mode

    After a read/write command is transmitted, a stop command is required for stopping data transfer at the end of data transfer.

  The difference between the two modes lies on how the MMC controller notifies the card of the end of each data transfer. The SD card supports only the open-ended mode, whereas the MMC supports both modes.

  The multi-block read/write command for the SDIO card is different from the preceding two modes. To be specific, the command parameter contains the number of data blocks to be transferred when the read/write command is transmitted.

Responses are classified into the following three types:

- Command without response

  For example, the card reset command.
- Short response command

  For example, the data transfer command and card status query command.
- Long response command

  This type of commands are used to read only the information about the card identification (CID) and card specific data (CSD) registers of a card.

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Data Transfer

The single-block read/write command and the multi-block read/write command are widely used during data transfer. The data block during the data transfer of the SD card and MMC is 512 bytes; the block size during the data transfer of the SDIO card can be customized

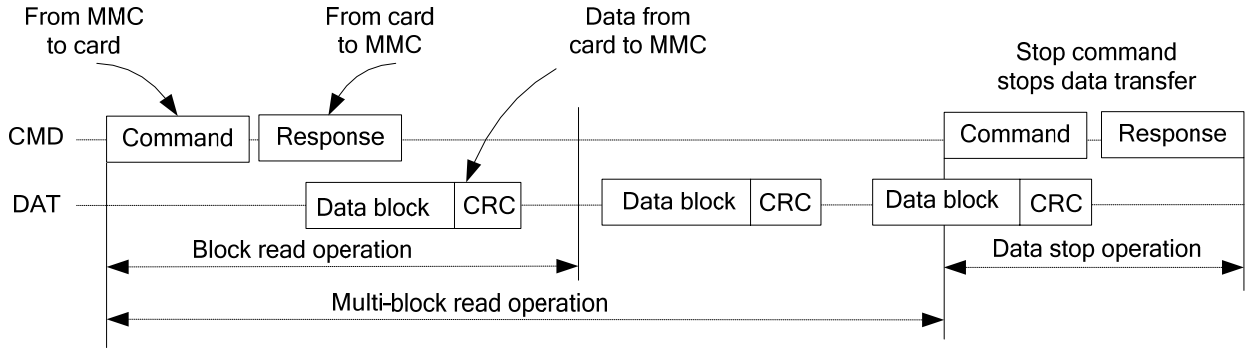
NOTE

During the data transfer by using the block read/write command, the total data amount to be transferred must be an integral multiple of the block size.

All data transfer commands are short response commands with data transferred through data lines. Figure 14-47 and Figure 14-48 show the relationships among the commands, responses, and timings of data lines.

(1) Single-block and multi-block read operations

Figure 14-47 Single-block and multi-block read operations

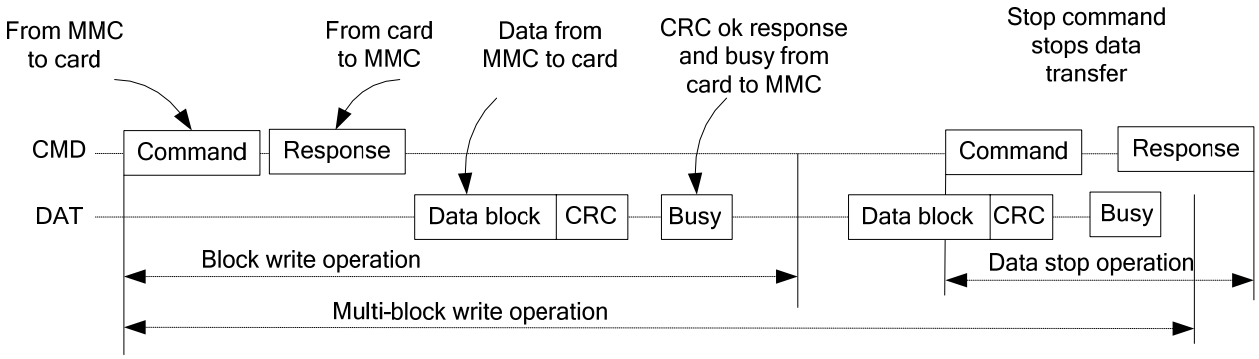


The MMC controller transmits a single-block or multi-block command to a card. When a response is being received, data is received by blocks. Each data block contains a CRC check bit for ensuring the integrity of the transferred data.

In a single-block read operation, the data transfer is completed after the MMC controller receives a data block. In a multi-block read operation, the MMC controller needs to transmit a stop command to end the data transfer after receiving multiple data blocks only in open-ended mode.

(2) Single-block and multi-block read operations

Figure 14-48 Single-block and multi-block write operations



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The MMC controller transmits a single-block or multi-block command to a card. After receiving a response, the MMC controller starts to transmit data to the card by blocks. Each data block contains a CRC bit. The card performs CRC on each data block and transfers the CRC status to the MMC controller. This ensures that data is transferred properly.

In a single-block write operation, the data transfer is completed after the MMC controller transmits a data block. In a multi-block write operation, the MMC controller needs to transmit a stop command to end the data transfer after transmitting multiple data blocks only in open-ended mode. After a write operation, the card may be busy in programming the flash memory. The MMC controller can perform the next operation on the card only after it confirms that the card is not busy by querying the status of the signal line DAT0.

(3) Data transfer format

During the block read/write operations, the 1- or 4-bit data line can be used to transfer data between the MMC controller and the card. Before a data transfer command is transmitted, the data transfer widths of the MMC controller and card must be the same (1 bit or 4 bits). You can set the data bit width of the MMC controller by configuring MMC_CTYPE and set the data bit width of the card by transmitting the corresponding command.

Figure 14-49 shows the data transfer format in 1-bit mode, and Figure 14-50 shows the data transfer format in 4-bit mode.

Figure 14-49 Data transfer format in 1-bit mode

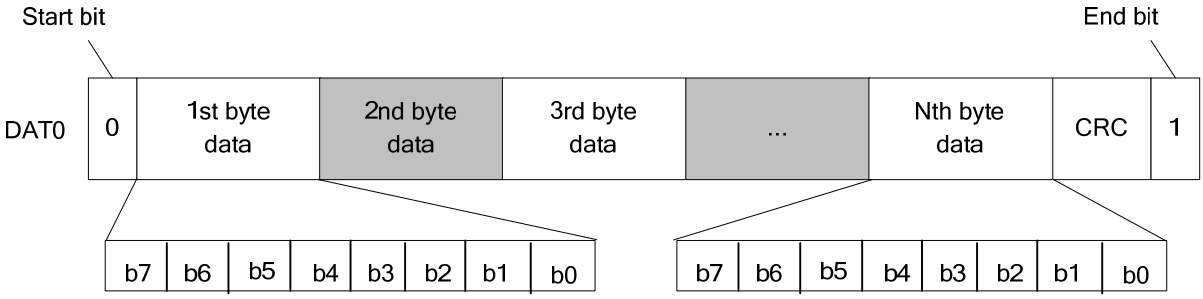
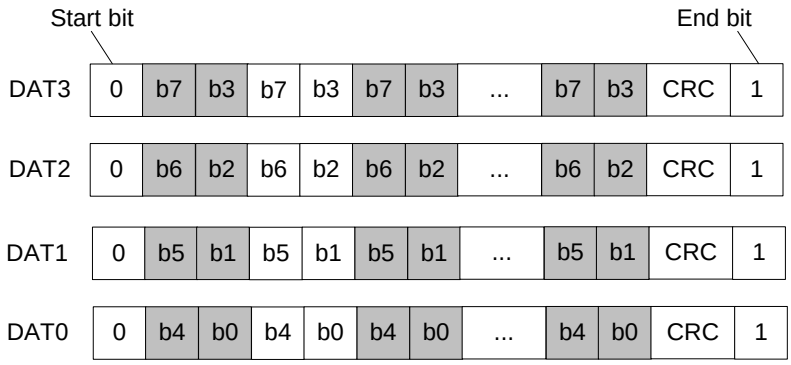


Figure 14-50 Data transfer format in 4-bit mode



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14.7.2 Timing and Parameters

14.7.2.1 Timing Parameters

Table 14-13 describes the timing parameters of the MMC interface.

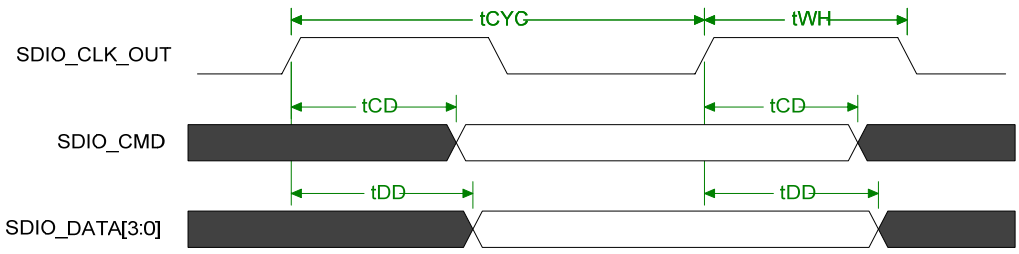
Table 14-13 Timing parameters of the MMC interface

Parameter	Description	Min	Max	Unit
tCYC	Card clock cycle	20	None	ns
tWH	High level duration of the card clock	0.5tCYC	0.5tCYC	ns
tCCLK_IN	Working clock cycle of the MMC module	20 or 41.67		ns
tCD	SDIO_CMD output delay	0.6tCCLK_IN – 5.0	0.6tCCLK_IN + 1.2	ns
tDD	SDIO_DATA output delay	0.6tCCLK_IN – 4.7	0.6tCCLK_IN + 2.1	ns
tCS	SDIO_CMD input setup time	5.0	None	ns
tCH	SDIO_CMD input hold time	0.7	None	ns
tDS	SDIO_DATA input setup time	5.3	None	ns
tDH	SDIO_DATA input hold time	0.7	None	ns

14.7.2.2 Interface Timings

Output Timing

Figure 14-51 Output timing



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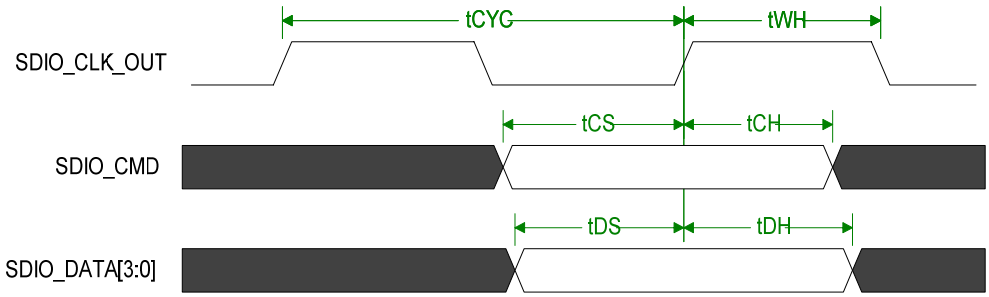
Input Timing

Figure 14-52 Input timing



14.7.3 Application Notes

Clock Gating

When the software completes the current command or data transfer and does not start a new data transfer, the SDIO_CCLK_OUT clock can be disabled if the MMC controller is idle.

Perform the following steps:

Step 1 Read MMC_STATUS.

Step 2 If both MMC_STATUS[Command fsm_states] and MMC_STATUS[data_state_mc_busy] are 0, write 0 to MMC_CTRL to mask the MMC interrupt, enable the DMA request, and go to 3; If any of [Command fsm_states] and [data_state_mc_busy] is not 0, wait with delay, and go to step 1.

Step 3 Write 0 to PERI_CRG49 bit[1] to disable SDIO.

Step 4 If you need to restart the working clock, write 1 to PERI_CRG49 bit[1].

---End

Soft Reset

If the MMC controller cannot restore to the idle state due to exceptions during the data transfer, you can soft-reset the SDIO module by writing 1 toPERI_CRG49 bit[0]. In addition, you can query MMC_STATUS[Data_busy] to check whether the MMC controller is idle.

Before using the MMC controller, you are advised to soft-reset the MMC controller after hot-swapping the card.

Configuring the Working Clock

Before using the MMC controller, you need to configure the frequency of its working clock. You can set the frequency of the MMC working clock to 24 MHz or 50 MHz by configuring PERI_CRG49 bit[2].**Configuring the Interface Clock**

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Clock frequencies vary according to the MMCs complying with different protocols and the status of MMCs. The MMC controller provides an internal even frequency divider that generates appropriate interface clocks by dividing the frequency of the working clock. The relationship between the frequencies of the working clock CCLK_IN and the interface clock SDIO_CCLK_OUT of the MMC controller is as follows:

$F_{SDIO_CCLK_OUT} = F_{CCLK_IN}/(2 \times clk_divider)$

Where, clk_divider is the value of MMC_CLKDIV[clk_divider]. Clock frequencies vary according to card types. The maximum value of $F_{SDIO_CCLK_OUT}$ is 50 MHz.

Before changing the clock frequency of an MMC, ensure that no data or command is being transferred. In addition, to avoid the occurrence of glitches in the output clock of the MMC, you need to perform the following steps:

Step 1 Disable the interface clock.

Set MMC_CLKNA to 0x0000_0000, set MMC_CMD[Start_cmd], MMC_CMD[Update_clk_regs_only], and MMC_CMD[Wait_prvdata_complete] to 1, and wait until MMC_CMD[Start_cmd] is cleared automatically.

Step 2 Set the clock divider.

Configure MMC_CLKDIV based on the required clock frequency, set MMC_CMD[Start_cmd] and MMC_CMD[Update_clk_regs_only] to 1, and wait until MMC_CMD[Start_cmd] is cleared automatically.

Step 3 Enable the interface clock again.

Set MMC_CLKENA to 0x0000_0001, set MMC_CMD[Start_cmd] and MMC_CMD[Update_clk_regs_only] to 1, and wait until MMC_CMD[Start_cmd] is cleared automatically.

---End

CAUTION

The values of MMC_CMD and MMC_CMD are loaded only after MMC_CLKDIV[Start_cmd] and MMC_CLKENA[Update_clk_only] are set to 1. After the values are loaded successfully, the MMC controller clears MMC_CMD[Start_cmd] automatically. If a command is being executed, a hardware locked error (HLE) interrupt is generated. In this case, you need to clear the interrupt, and then transmit a command again.

When a command is being executed or data is being transferred, the clock parameter values of the card cannot be changed.

Initialization

Before commands and data are exchanged between a card and the MMC controller, the MMC controller needs to be initialized. Perform the following steps:

Step 1 Configure the frequency of the working clock of the MMC controller. For details, see "Working Clock Configuration" in section 14.7.3 "Application Notes."

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Step 2 Soft-reset the MMC controller after the card is powered on and the command and data signal lines are pulled up and become stable. For details, see "Soft Reset" in section 14.7.3 "Application Notes.."

Step 3 Clear interrupts. Set all bits of MMC_RINTSTS bit[15:0] to 1 to clear raw interrupt status bits.

Step 4 Configure MMC_INTMASK. Set all bits of MMC_INTMASK bit[15:0] to 1 to enable all interrupt sources.

If data is transferred in DMA mode, set MMC_INTMASK bit[4] and MMC_INTMASK bit[5] to 0 to mask the transmit/receive FIFO data request interrupts.

Step 5 Set MMC_CTRL[Int_enable] to 1 to enable the MMC interrupt.

Step 6 Configure the timeout parameter register MMC_TMOUT.

Step 7 Configure the FIFO parameter register MMC_FIFOTH.

---End

After the preceding steps, the interface clock can be configured and commands can be transmitted to the card.

Non-Data Transfer Command

If the MMC controller receives a response (correct response, error response, or timeout response) after transmitting a command, the MMC controller sets MMC_RINTSTS bit[2] to 1. Short responses are stored in MMC_RESP0, and long responses are stored in MMC_RESP0 to MMC_RESP3. MMC_RESP3 bit[31] is the MSB, and MMC_RESP0 bit[0] is the LSB. After a command is transmitted, its error status is reflected by the response command and the corresponding error bit of MMC_RINTSTS.

To transmit a non-data transfer command, perform the following steps:

Step 1 Set the corresponding command parameters of MMC_CMDARG.

Step 2 Configure the command register MMC_CMD based on the description in Table 14-14.

Step 3 Wait until the MMC controller runs the command. If the command is executed, the MMC controller clears MMC_CMD[Start_cmd] automatically.

Step 4 Check whether an HLE interrupt is generated by MMC_RINTSTS bit[12].

Step 5 Wait until the command is executed. If the MMC controller receives a response (correct response, error response, or timeout response), the MMC controller sets MMC_RINTSTS bit[2] to 1. This indicates that the command is executed.

Step 6 Check whether there is any response exception and read the response value if necessary.

You can check the response timeout error, response CRC error, and response error by reading MMC_RINTSTS bit[8], MMC_RINTSTS bit[6], and MMC_RINTSTS bit[1] respectively.

---End

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CAUTION

The values of MMC_CMD, MMC_CMDARG, MMC_BYTCNT, and MMC_BLKSIZ are loaded only after MMC_CMDARG[Start_cmd] is set to 1 and MMC_CMD[Update_clock_registes_only] is set to 0. After the values are loaded successfully, the MMC controller clears MMC_CMD[Start_cmd] automatically.

If other commands are being executed, an HLE interrupt is generated. In this case, you need to perform the preceding operations again. When a non-data transfer command is executed, the values of MMC_BYTCNT and MMC_BLKSIZ are ignored.

Table 14-14 Default values of MMC_CMD when a non-data transfer command is executed

Parameter	Value	Description
Start_cmd	1	Indicates that a command starts to be transmitted.
Update_clock_registes_only	0	Indicates a non-clock parameter update command.
data_transfer_expected	0	Indicates a non-data transfer command
card_number	0	-
cmd_index	Cmd index	Command index.
send_initialization	0	Indicates that this bit is set to 1 when a command is a card reset command such as CMD0.
stop_abort_cmd	0	Indicates that this bit is set to 1 when a command is a data transfer stop command such as CMD12.
rsponse_length	0	Indicates that this bit is set to 1 when the response is a long response.
rsponse_expect	1	Indicates that this bit is set to 0 when a command is not responded, such as CMD0, CMD4, or CMD15.
Wait_prvdata_complete	1 or 0	Indicates that the MMC controller must wait until the current data transfer command is executed before transmitting another command. You are advised to set this bit to the fixed value 1 except that the command is used for querying the card status during data transfer or stopping the current data transfer.
Check_response_crc	1 or 0	Indicates whether the MMC controller checks the responded CRC bit.

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Reading a Single Data Block or Multiple Data Blocks

To read a single data block or multiple data blocks, perform the following steps:

Step 1 Write 1 to MMC_CTRL[fifo_reset] to reset the FIFO pointer, and query and wait until this bit is cleared automatically.

Step 2 Write the number of bytes to be transmitted to MMC_BYTCNT.

Step 3 Write the block size to MMC_BLKSIZ.

Step 4 Write the start address for reading data to MMC_CMDARG.

Step 5 Configure MMC_CMD according to the description in Table 14-15.

For the SD card or MMC, you need to read a single data block by running CMD17, and read multiple data blocks by running CMD18; for the SDIO card, you need to read a single data block or multiple data blocks by running CMD53.

The MMC controller starts to run commands after MMC_CMD is written. After commands are transferred to the bus, the cmd_done interrupt is generated.

Step 6 Check the values of MMC_RINTSTS bit[5] and MMC_RINTSTS bit[10]. If any or both of them are 1, read the data in the FIFO by reading MMC_DATA. This ensures that the MMC controller can receive the subsequent data. In addition, check data error interrupts, that is, check the values of MMC_RINTSTS bit[7], MMC_RINTSTS bit[9], MMC_RINTSTS bit[13], and MMC_RINTSTS bit[15]. In this case, you can transmit a stop command to stop the data transfer by using the software.

Step 7 If MMC_RINTSTS bit[3] is 1, data transfer is complete. In this case, read the remaining data in the FIFO by reading MMC_DATA.

Step 8 If MMC_CMD[Send_auto_stop] is set to 1 during the command execution, the MMC controller automatically transmits a stop command to stop the data transfer. For details, see "Configuration for Using the Auto-Stop Function" in section 14.7.3 "Application Notes."

---End

Table 14-15 Default values of MMC_CMD when a single data block or multiple data blocks are read

Parameter	Value	Description
Start_cmd	1	Indicates that a command starts to be transmitted.
Update_clock_registes_only	0	Indicates a non-clock parameter update command.
card_number	0	-
send_initialization	0	Indicates that this bit is set to 1 when a command is a card reset command such as CMD0.
stop_abort_cmd	0	Indicates that this bit is set to 1 when a command is a data transfer stop command such as CMD12.

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Parameter	Value	Description
send_auto_stop	0 or 1	For details, see "Configuration for Using the Auto-Stop Function" in section 14.7.3 "Application Notes."
transfer_mode	0	Indicates block transfer.
read/write	0	Indicates that data is read from the card.
rsponse_length	0	Indicates that all responses to data commands are short responses.
data_transfer_expected	1	Indicates a data transfer command.
rsponse_expect	1	Indicates that this bit is set to 0 when a command is not responded such as CMD0, CMD4, or CMD15.
cmd_index	Cmd index	Indicates the command index.
Wait_prvdata_complete	1 or 0	Indicates that the master device must wait until the current data transfer command is executed before transmitting another command. You are advised to set this bit to the fixed value 1 except that the command is used for querying the card status or stopping the current data transfer.
Check_response_crc	1 or 0	Indicates whether the MMC controller checks the responded CRC bit.

Writing a Single Data Block or Multiple Data Blocks

To write a single data block or multiple data blocks, perform the following steps:

Step 1 Write 1 to MMC_CTRL[fifo_reset] to reset the FIFO pointer, and query and wait until this bit is cleared automatically.

Step 2 Write the size of the data to be transmitted to MMC_BYTCNT.

Step 3 Write the block size to MMC_BLKSIZ.

Step 4 Write the start address for writing data to MMC_CMDARG.

Step 5 Write data to the FIFO by writing to MMC_DATA. The FIFO needs to be filled with data completely at the very beginning.

Step 6 Configure MMC_CMD according to the description in Table 14-16.

For the SD card or MMC, you need to write a single data block by running CMD24, and write multiple data blocks by running CMD25; for the SDIO card, you need to write a single data block or multiple data blocks by running CMD53.

Step 7 Check the values of MMC_RINTSTS bit[4] and MMC_RINTSTS bit[10]. If any or both of them are 1, fill the FIFO with data by writing to MMC_DATA. In addition, check data error interrupts, that is, check the values of MMC_RINTSTS bit[7], MMC_RINTSTS bit[9], MMC_RINTSTS bit[13], and MMC_RINTSTS bit[15]. If necessary, you can transmit a stop

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command to stop the data transfer by using the software. If MMC_RINTSTS bit[3] is 1, the data transfer is complete.

Step 8 If MMC_CMD[Send_auto_stop] is set to 1 during the command execution, the MMC controller automatically transmits a stop command to stop the data transfer. For details, see "Configuration for Using the Auto-Stop Function" in section 14.7.3 "Application Notes."

Step 9 Query and wait until the value of MMC_STATUS[data_busy] is changed from 1 to 0.

---End

Table 14-16 Default values of MMC_CMD when a single data block or multiple data blocks are written

Parameter	Value	Description
Start_cmd	1	Indicates that a command starts to be transmitted.
Update_clock_registes_only	0	Indicates a non-clock parameter update command.
card_number	0	-
send_initialization	0	Indicates that this bit is set to 1 when a command is a card reset command such as CMD0.
stop_abort_cmd	0	Indicates that this bit is set to 1 when a command is a data transfer stop command such as CMD12.
send_auto_stop	0 or 1	For details, see "Configuration for Using the Auto-Stop Function" in section 14.7.3 "Application Notes."
transfer_mode	0	Indicates block transfer.
read_write	1	Indicates that data is written to the card.
rsponse_length	0	Indicates that all responses to data commands are short responses.
data_transfer_expected	1	Indicates a data transfer command.
rsponse_expect	1	Indicates that this bit is set to 0 when a command is not responded such as CMD0, CMD4, or CMD15.
cmd_index	Cmd index	-
Wait_prvdata_complete	1 or 0	Indicates that the master device must wait until the current data transfer command is executed before transmitting another command. You are advised to set this bit to the fixed value 1 except that the command is used for querying the card status or stopping the current data transfer.
Check_response_crc	1 or 0	Indicates whether the MMC controller checks the responded CRC bit.

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Reading/Writing Stream Data

The modes of reading/writing stream data are the same as those of reading/writing data blocks, except that MMC_CMD[Transfer_mode] needs to be set to 1. During a stream data transfer, the auto-stop function is required.

Transferring Data by Using the IDMAC

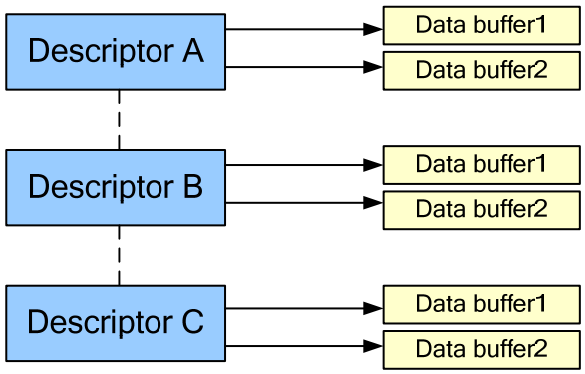
The MMC controller has an embedded IDMAC that transfers data from the original address to the destination address based on the specified descriptor.

Descriptor

The IDMAC supports the following two types of descriptors:

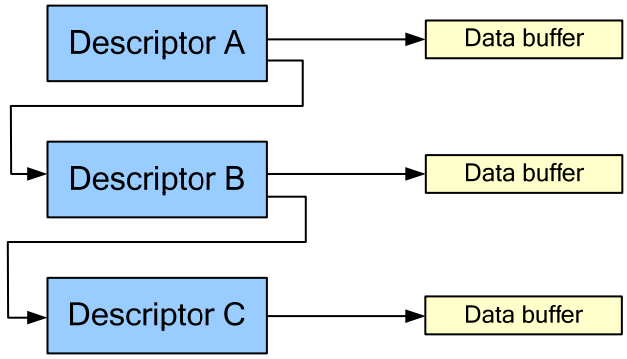
- Dual-buffer descriptor. For this type of descriptor, the span between two descriptors is determined by the DSL bit of MMC_BMOD. Figure 14-53 shows the structure of the dual-buffer descriptor.

Figure 14-53 Structure of the dual-buffer descriptor



- Linked descriptor. For this type of descriptor, each descriptor points to a unique buffer and the next descriptor. Figure 14-54 shows the structure of the linked descriptor.

Figure 14-54 Structure of the linked descriptor



Each descriptor must be word-aligned, and each descriptor contains 16-byte control and status information. Figure 14-55 shows the internal structure of 32-bit descriptors.

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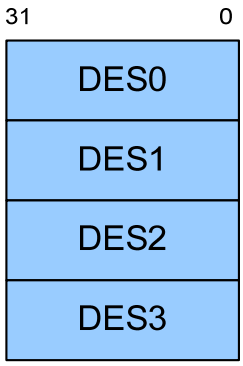
Figure 14-55 Internal structure of 32-bit descriptors



DES0 is used to protect the control and status information. Table 14-17 describes the definition of each bit.

Table 14-17 Definition of each bit of DES0

Bits	Register	Description
31	OWN	Indicates the attributes of the descriptor. 0: The descriptor belongs to the CPU. 1: The descriptor belongs to the IDMAC. After data is transferred by using the IDMAC, the IDMAC clears this bit.
30	CES	Indicates the error status when a card is read. 0: No error occurs. 1: An error occurs.
29:6	RES	Reserved
5	ER	Indicates the link end of the descriptor. 0: The descriptor is not the last one on the link. 1: The descriptor is the last one on the link. This bit is valid only for the dual-buffer descriptor.
4	CH	Indicates the definition of the second address in DES3. 0: The second address in DES3 is the address of the second buffer. 1: The second address in DES3 is the address of the next descriptor. When this bit is 1, DES1[25:13] must be 0.
3	FS	Indicates that the descriptor contains the first data buffer when this bit is 1. If the size of the first data buffer is 0, the next descriptor contains the start data.
2	LD	Indicates that the descriptor points to the last data buffer when this bit is 1.

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Bits	Register	Description
1	DIC	Indicates that the data transfer completion interrupt is masked when this bit is 1.
0	RES	Reserved

DES1 is used to specify the buffer size. Table 14-18 describes the definition of each bit of DES1.

Table 14-18 Definition of each bit of DES1

Bits	Register	Description
31: 26	RES	Reserved
25: 13	BS2	Indicates the number of bytes in the second data buffer. This value must be an integral multiple of 4. This bit is invalid when DES0[4] is 1.
12: 0	BS1	Indicates the number of bytes in the first data buffer. This value must be an integral multiple of 4.

DES2 is the address pointer of the first data buffer. Table 14-19 describes the definition of each bit of DES2.

Table 14-19 Definition of each bit of DES2

Bits	Register	Description
31: 0	BAP1	Indicates the physical address of the first data buffer. The address must be word-aligned.

DES3 indicates the second address. Table 14-20 describes the definition of each bit of DES3.

Table 14-20 Definition of each bit of DES3

Bits	Register	Description
31: 0	BAP2	Indicates the physical address of the second data buffer when dual-buffer descriptors are used, or indicates the physical address of the next descriptor when DES0[4] is 1.

Initialization

Perform the following steps:

Step 1 Configure MMC_BMOD to set bus parameters.

Step 2 Configure MMC_IDINTEN to mask unnecessary registers.

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Step 3 Create transmit/receive descriptor linked lists, configure MMC_DBADDR, and set the start address.

Step 4 The IDMAC attempts to obtain descriptors from the descriptor linked lists.

---End

Transmission

Perform the following steps:

Step 1 Create the descriptors DES0 to DES3 by using the CPU, set DES0 bit[31] (OWN bit) to 1, and provide data buffers.

Step 2 Write data commands to MMC_CMD.

Step 3 Set TX_Wmark by using MMC_FIFOTH.

Step 4 The IDMAC obtains descriptors and check whether the value of the OWN bit is 1. If the OWN bit is not 1, wait until the CPU releases descriptors. During this process, the IDMAC enters the suspend state. Therefore, the CPU needs to configure MMC_PLDMND to enable the IDMAC to obtain descriptors again.

Step 5 The IDMAC transfers data from data buffers to the internal FIFO of the MMC controller when the OWN bit is 1.

Step 6 If the interrupts are enabled, the corresponding bit of the IDMAC status register MMC_IDSTS is updated and the OWN bit is cleared after data transfer.

---End

Reception

Perform the following steps:

Step 1 Create the descriptors DES0 to DES3 by using the CPU, and set the DES0 bit[31] (OWN bit) to 1.

Step 2 Write read commands to MMC_CMD.

Step 3 Set RX_WMark by using MMC_FIFOTH.

Step 4 The IDMAC obtains descriptors and check whether the value of the OWN bit is 1. If the OWN bit is not 1, wait until the CPU releases descriptors. During this process, the IDMAC enters the suspend state. Therefore, the CPU needs to configure MMC_PLDMND to enable the IDMAC to obtain descriptors again.

Step 5 The IDMAC transfers data from the internal FIFO of the MMC controller to the external data buffers when the OWN bit is 1.

Step 6 If the interrupts are enabled, the corresponding bit of the IDMAC status register MMC_IDSTS is updated and the OWN bit is cleared after data transfer.

---End

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Auto-Stop Function Configuration

When multiple data blocks are read or written, a stop command is required to stop each data transfer. The stop command can be transmitted in non-data transfer command mode or by using the auto-stop function.

The auto-stop function is applicable in the following scenarios:

- SD card

  Multi-block read/write operation by running CMD18 or CMD25
- MMC
  - Stream data read/write operation
  - Multi-block read/write operation in open-ended mode by running CMD18 or CMD25

Before using the auto-stop function of the MMC controller, you are advised to perform the followings steps:

Step 1 Set MMC_CMD[Send_auto_stop] to 1 during the block transfer command operation.

Step 2 After data transfer, the MMC controller automatically transmits a stop command to enable the card to restore to the corresponding state.

Step 3 Read MMC_RINTSTS[auto_cmd_done] to check whether the stop command is executed. The response is stored in MMC_RESP1.

---End

Stopping or Aborting the Data Transfer

The stop command is used to interrupt the data transfer between the MMC controller and the card, whereas the abort command is used to interrupt the I/O data transfer only in SDIO_IOONLY or SDIO_COMBO mode.

The two commands are used as follows:

- Stop command

  This command can be transmitted at any time during data transfer, because this command is used to stop the data transfer. In this case, you need to set MMC_CMD bit[5:0] to CMD12, MMC_CMD bit[14] to 1, and MMC_CMD bit[13] to 0.
- Abort command

  This command is available only for SDIO_IOONLY or SDIO_COMBO. To abort the data transfer, you need to configure the CCCR[ASx] register of the SDIO card by running the CMD52 command.

Suspend and Resume Operations

An SDIO card can store the data of a maximum of seven functional devices. The MMC controller can suspend the data transfer of a device by performing the suspend operation. Then the SD interface bus is available for another device with higher priority. After the device with higher priority transfers data, the MMC controller can resume the suspended data transfer of the previous device.

The suspend and resume operations are implemented by configuring the corresponding bits of the CCCR register of the SDIO card. The CCCR register is written or read by running the CMD52 command.

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To implement a suspend operation, perform the following steps:

Step 1 Query the SBS bit of the CCCR register to check whether the SDIO card supports suspend and resume operations.

Step 2 Query the FSx and bus status (BS) bits of the CCCR register to check whether the functional device to be suspended is transferring data.

If the BS bit is 1, the device specified by the FSx bit is transferring data.

Step 3 Set the bus release (BR) bit of the CCCR register to 1 to suspend the current data transfer.

Step 4 Check whether the BS and the BR bits of the CCCR register are cleared.

The BS bit retains 1 when the data bus is being used. The BR bit retains 1 before the bus is released completely. When both the BR and BS bits are 0, the data transfer of the selected functional device is suspended.

Step 5 If the current read operation is suspended, MMC_CTRL[Abort_read_data] needs to be set to 1 to restart the data transfer function of the MMC controller after the suspend operation. Then MMC_CTRL[Abort_read_data] is cleared automatically.

Step 6 Read MMC_TCBCNT to query the number of transferred bytes.

---End

To implement a resume operation, perform the following steps:

Step 1 Query the transfer status of the card to check whether the bus is idle.

Step 2 If the card is disconnected, run the CMD7 command to select it. The card status can be queried by running the CMD52 or CMD53 command.

Step 3 Check whether the device to be resumed is ready for data transfer by querying the RF bit of the CCCR register. If the RF bit is 1, the device is ready for data transfer.

Step 4 Run the CMD52 command to write the device ID to the FS bit of the CCCR register to resume the data transfer, and enable the MMC controller to enter the data transfer state (that is, write the block size to MMC_BLKSIZ, and write the amount of remaining data to be transferred to MMC_BYTCNT).

For details about the configuration of MMC_CMDARG, see Table 14-21. The configuration of MMC_CMD is similar to the configuration during block transfer.

Step 5 The data transfer is resumed after the CMD52 command is transmitted successfully. Read the resume data flag (DF) bit of the SDIO device. If this bit is 1, data transfer starts when the transfer function is resumed. If this bit is 0, no data is ready for transferring.

Step 6 If the DF bit is 0, the MMC generates a data timeout error interrupt a period of time later during data read.

---End

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Table 14-21 Reference configuration of MMC_CMDARG when the resume operation is performed

MMC_CMDARG	Value	Description
Bit[31]	1	Indicates the read/write flag.
Bit[30:28]	0	Indicates the ID of a functional device that accesses the CCCR register.
Bit[27]	1	Indicates the real-time flag, that is, write-to-read.
Bit[26]	None	-
Bit[25:9]	0x0D	Indicates the register address.
Bit[8]	None	-
Bit[7:0]	ID of the functional device that is resumed	Indicates write data.

CAUTION

The MMC controller cannot be woken up after the system enters the low-power mode.

Read Wait Operation

The read wait operation is performed to suspend the data transfer of the device that is using the SDIO card. The MMC controller determines the duration of pausing the data transfer.

To implement a read wait operation, perform the following steps:

Step 1 Check whether the card supports the read wait operation.

You can read the SRW bit of the CCCR register by running the CMD52 command. If the SRW bit is 1, all the devices supporting the card support the read wait operation.

Step 2 Set MMC_CTRL[Read_wait] to 1.

Step 3 If you want to resume the data transfer, clear MMC_CTRL[Read_wait].

---End

14.7.4 Register Summary

Table 14-22 describes the MMC registers.

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Table 14-22 Summary of MMC registers (base address: 0x1002_0000)

Offset Address	Register	Description	Page
0x0000	MMC_CTRL	MMC control register	14-119
0x0004	MMC_PWREN	Power_en control register	14-121
0x0008	MMC_CLKDIV	Clock divider register	14-122
0x000C	MMC_CLKSRC	Clock source select register of the SD card	14-122
0x0010	MMC_CLKENA	Clock enable register	14-123
0x0014	MMC_TMOUT	Timeout register	14-123
0x0018	MMC_CTYPE	Card type register	14-122
0x001C	MMC_BLKSIZ	Block size configuration register	14-123
0x0020	MMC_BYTCNT	Block transfer count register	14-123
0x0024	MMC_INTMASK	Interrupt mask register	14-124
0x0028	MMC_CMDARG	Command parameter register	14-124
0x002C	MMC_CMD	Command register	14-124
0x0030	MMC_RESP0	Response register 0	14-125
0x0034	MMC_RESP1	Response register 1	14-126
0x0038	MMC_RESP2	Response register 2	14-127
0x003C	MMC_RESP3	Response register 3	14-129
0x0040	MMC_MINTSTS	Masked interrupt status register	14-130
0x0044	MMC_RINTSTS	Raw interrupt status register	14-130
0x0048	MMC_STATUS	Status register	14-130
0x004C	MMC_FIFOTH	FIFO threshold register	14-131
0x0050	MMC_CDETECT	Card detection register	14-132
0x0054	MMC_WRTPRT	Card write protection register	14-133
0x005C	MMC_TCBCNT	Count of bytes transmitted to the card register	14-135
0x0060	MMC_TBBCNT	Count of bytes transmitted from the bus interface unit (BIU) FIFO register	14-136
0x0080	MMC_BMOD	Bus mode register	14-136
0x0084	MMC_PLDMND	Poll demand register	14-137
0x0088	MMC_DBADDR	Base address register of the descriptor linked list	14-137
0x008C	MMC_IDSTS	IDMAC status register	14-137

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Offset Address	Register	Description	Page
0x0090	MMC_IDINTEN	IDMAC interrupt enable register	14-138
0x0094	MMC_DSCADDR	Address register of the current descriptor	14-139
0x0098	MMC_BUFADDR	Address register of the current data buffer	14-139
0x0100	MMC_DATA	Data register (entrance address of the FIFO)	14-140

14.7.5 Register Description

MMC_CTRL

MMC_CTRL is a MMC control register.

Offset Address	Register Name	Total Reset Value
0x0000	MMC_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						Use_internal_dmac	Enable_OD_pullup	reserved															Abort_read_data	Send_irq_response	Read_wait	Dma_enable	Int_enable	reserved	Dma_reset	Fifo_reset	Controller_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25]	RW	Use_internal_dmac	Whether to transfer data by using the IDMAC. 0: The CPU transfers data by using the slave interface. 1: The CPU transfers data by using the IDMAC.
[24]	RW	Enable_OD_pullup	External open-drain pull-up. 0: disabled 1: enabled This value is inverted internally, and transmitted to the SDIOn_CCMD_ODPULLUP_EN_N (n = 0 or 1) pin.
[23:9]	-	reserved	Reserved.

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[8]	RW	Abort_read_data	Whether to abort the data transfer during data read. 0: invalid 1: After transmitting a suspend command during data read, the software polls the card to check when suspend occurs. After the suspend occurs, the software sets the bit to 1. This enables the data transfer state machine to be restored to idle state for the next block transfer. After the state machine restores to the idle status, this bit is cleared automatically.
[7]	RW	Send_irq_response	Transmit interrupt response control. 0: invalid 1: An interrupt request (IRQ) response is transmitted automatically. After the response is transmitted, this bit is cleared automatically. To wait for the interrupt generated by the MMC controller, the host transmits the CMD40 command and waits for the interrupt response from the MMC controller. If you do not want the host to keep in the interrupt wait state, set this bit to 1 and transmit the CMD40 command to restore the host to the idle state.
[6]	RW	Read_wait	Read wait control. 0: disabled 1: enabled This bit is valid only for the SDIO card that supports the read wait function.
[5]	RW	Dma_enable	Reserved. The system uses the IDMAC.
[4]	RW	Int_enable	Global interrupt enable. 0: disabled 1: enabled The interrupt output is valid only when this bit is valid and the interrupt source is enabled.
[3]	-	reserved	Reserved.
[2]	RW	Dma_reset	Soft reset control for the IDMAC. 0: invalid 1: reset the internal DMA interface This bit is automatically reset after two AHB clock cycles.
[1]	RW	Fifo_reset	Soft reset control for the internal FIFO. 0: invalid 1: reset the FIFO pointer This bit is reset automatically after the reset operation is complete.

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[0]	RW	Controller_reset	Soft reset control for the controller. 0: invalid 1: reset the MMC/SD/SDIO host module

MMC_PWREN

MMC_PWREN is a Power_en control register.

Offset Address	Register Name	Total Reset Value
0x0004	MMC_PWREN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Power_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	Power_enable	Power control. 0: power off 1: power on This value is used to drive the SDIOn_CARD_POWER_EN (n = 0 or 1) pin.

MMC_CLKDIV

MMC_CLKDIV is a clock divider register that shows the ratio of the frequency of the module output clock to the frequency of the input clock. For example, if the module input clock is 40 MHz and the register value is set to 1, the output clock is 20 MHz.

The clock divider is 2 x N. If the value of *N* is 0x0, it indicates no frequency division (2 x 0 = 0); if the value of *N* is 0x1, the frequency is divided by 2; if the value of *N* is 0xFF, the frequency is divided by 510.

Offset Address	Register Name	Total Reset Value
0x0008	MMC_CLKDIV	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Clk_divider0							

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	RW	Clk_divider0	Clock divider 0. The clock divider is 2 x N. If the value of N is 0, it indicates no frequency division; if the value of N is 0x1, the frequency is divided by 2; if the value of N is 0xFF, the frequency is divided by 510.

MMC_CLKSRC

MMC_CLKSRC is a clock source select register of the SD card.

Offset Address	Register Name	Total Reset Value
0x000C	MMC_CLKSRC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Clk_source
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	Clk_source	This bit must be set to 0.

MMC_CLKENA

MMC_CLKENA is a clock enable register.

Offset Address	Register Name	Total Reset Value
0x0010	MMC_CLKENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															Cclk_low_power	reserved															Cclk_enable

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16]	RW	Cclk_low_power	Card low-power control for disabling the card clock. 0: non lower-power mode 1: low-power mode When the card is idle, the card clock is disabled. This function is used only for the MMC and SD card, because the card clock of the SDIO card must be retained for detecting interrupts.
[15:1]	RW	reserved	Reserved.
[0]	RW	Cclk_enable	Card clock enable. 0: disabled 1: enabled

MMC_TMOUT

MMC_TMOUT is a timeout register.

Offset Address	Register Name	Total Reset Value
0x0014	MMC_TMOUT	0xFFFF_FF40

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Data_timeout																								response_timeout							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	Data_timeout	Timeout during the data transfer of the card, in unit of the mmc_clk cycle of the card. The timeout is also the data starvation timeout of the CPU
[7:0]	RW	response_timeout	Response timeout, in unit of the mmc_clk cycle of the card.

MMC_CTYPE

MMC_CTYPE is a card type register.

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Offset Address	Register Name	Total Reset Value
0x0018	MMC_CTYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															Card_width	reserved															Card_width1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16]	RW	Card_width_0	Bus width of the card. 0: non-8-bit mode 1: 8-bit mode The details are as follows: If bit[16] is 1, the bus width of the card is set to 8-bit mode, and the value of bit[0] is ignored. If bit[16] is 0, the bus width of the card is set to 1-bit mode or 4-bit mode. In this case, the bus width depends on the value of bit[0].
[15:1]	RW	reserved	Reserved.
[0]	RW	Card_width_1	Bus width of the card. 0: 1-bit mode 1: 4-bit mode

MMC_BLKSIZ

MMC_BLKSIZ is a block size configuration register.

Offset Address	Register Name	Total Reset Value
0x001C	MMC_BLKSIZ	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Block_size															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	Block_size	Block size. The initial size of each block is 512 bytes.

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MMC_BYTCNT

MMC_BYTCNT is a block transfer count register.

Offset Address	Register Name	Total Reset Value
0x0020	MMC_BYTCNT	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Byte_count																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	Byte_count	Number of transferred bytes. The number must be an integral multiple of the block size. If the data transfer is not block transfer, this register must be set to 0. In this case, the software needs to transmit a stop or an abort command to control the data transfer.

MMC_INTMASK

MMC_INTMASK is an interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0024	MMC_INTMASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	17	16	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												Sdio_int_mask			Int_mask															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16]	RW	Sdio_int_mask	SDIO interrupt mask. 0: masked 1: enabled

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[15:0]	RW	Int_mask	Interrupt mask. 0: masked 1: enabled Bit[15]: end-bit error (read)/write no CRC (EBE) Bit[14]: auto command done (ACD) Bit[13]: start-bit error (SBE) Bit[12]: hardware locked write error (HLE) Bit[11]: FIFO underrun/overrun error (FRUN) Bit[10]: data starvation-by-host timeout (HTO) Bit[9]: data read timeout (DTO) Bit[8]: response timeout (RTO) Bit[7]: data CRC error (DCRC) Bit[6]: response CRC error (RCRC) Bit[5]: receive FIFO data request (RXDR) Bit[4]: transmit FIFO data request (TXDR) Bit[3]: data transfer over (DTO) Bit[2]: command done (CD) Bit[1]: response error (RE) Bit[0]: card detect (CD)

MMC_CMDARG

MMC_CMDARG is a command parameter register.

Offset Address	Register Name	Total Reset Value
0x0028	MMC_CMDARG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Cmd_arg																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	Cmd_arg	Command parameter that is transferred to the card. The command parameter is related to the protocol, and each command corresponds to a command parameter.

MMC_CMD

MMC_CMD is a command register.

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Offset Address	Register Name	Total Reset Value
0x002C	MMC_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Start_cmd	reserved			Boot_mode	Disable_boot	Expect_boot_ack	Enable_boot	reserved		Update_clock_registes_only	Card_number					Send_initialization	Stop_abort_cmd	wait_prvdata_complete	Send_auto_stop	Transfer_mode	Read_write	data_transfer_expected	Check_repsonse_crc_	Response_length	Response_expect	Cmd_index					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	Start_cmd	Start control. 0: do not start 1: start a command After the command is transferred to the card interface unit (CIU), this bit is cleared. The CPU does not allow modifications to this register. Otherwise, an HLE interrupt is generated. After transmitting a command, the CPU queries this bit, and transmits the next command when the value of this bit changes to 0.
[30:28]	-	reserved	Reserved.
[27]	RW	Boot_mode	Boot mode. 0: boot mode 1: alternative boot mode
[26]	RW	Disable_boot	Boot disable. If the software enables this bit and the Start_cmd bit at the same time, the controller aborts the boot operation. The Enable_boot and Disable_boot bits cannot be enabled at the same time.
[25]	RW	Expect_boot_ack	Boot response enable. If the software enables this bit and the Enable_boot bit at the same time, the controller detects the boot response signal in "0 – 1 – 0" sequence.

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[24]	RW	Enable_boot	Boot enable. This bit is available when the boot mode is mandatory. If the software enables this bit and the Start_cmd bit, the controller pulls down the CMD signal to start the boot process. The Enable_boot and Disable_boot bits cannot be enabled at the same time.
[23:22]	-	reserved	Reserved.
[21]	RW	Update_clock_registes_only	Automatic update. 0: The normal command sequence is used. That is, the values of MMC_CMD, MMC_CMDARG, MMC_TMOUT, MMC_CTYPE, MMC_BLKSIZ, and MMC_BYTCNT are transferred from the BIU to the CIU. The CIU uses the new values of registers when running new commands. 1: No command is transmitted, and only the clock register values in the card clock domain are updated. The values of MMC_CLKDIV, MMC_CLKSRC, and MMC_CLKENA are transferred to the card clock domain. The card clock can be changed (frequency change and clock enable) even no command is transmitted. Each time the card clock is changed; this bit must be set to 1. In this case, no command is transmitted to the card, and no command done interrupt is generated.
[20:16]	RW	Card_number	Serial number of the card that is being used.
[15]	RW	Send_initialization	Whether to transmit the initialization sequence. 0: do not transmit the initialization sequence before transmitting the Send_initialization command (high level in 80 clock cycles) 1: transmit the initialization sequence before transmitting the Send_initialization command When a card is powered on, the initialization sequence must be transmitted for initialization before any command is transmitted. That is, this bit must be set to 1.
[14]	RW	Stop_abort_cmd	Whether to transmit the stop/abort command when data is being transferred in open-ended mode or in fixed length mode. 0: do not transmit the stop/abort command 1: transmit the stop/abort command for stopping the current data transfer
[13]	RW	wait_prvdata_complete	Whether to transmit a command immediately. 0: transmit a command immediately even though the previous data transfer is not complete 1: transmit a command only when the previous data transfer is complete The typical value is 0. If this bit is set to 0, the transfer status can be read during data transfer, and the interrupt transfer is supported.

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[12]	RW	Send_auto_stop	Whether to transmit the stop command. 0: do not transmit the stop command after data transfer 1: transmit the stop command after data transfer In non-data transfer mode, this bit is ignored.
[11]	RW	Transfer_mode	Transfer mode. 0: block transfer mode 1: stream transfer mode In non-data transfer mode, this bit is ignored.
[10]	RW	Read_write	Read/write control. 0: read data from the card 1: write data to the card In non-data transfer mode, this bit is ignored.
[9]	RW	data_transfer_expected	Data transfer indicator. 0: No data is output from the card. 1: Data is output from the card.
[8]	RW	Check_repsonse_crc_	Whether to perform the CRC check. 0: do not check the CRC response 1: check the CRC response No valid CRC is returned when some commands are responded. To prevent the host from performing CRC, the software needs to disable this function based on related commands.
[7]	RW	Response_length	Response length. 0: Short responses are output from the card 1: Long responses are output from the card The length of a long response is 128 bits, whereas the length of a short response is 32 bits.
[6]	RW	Response_expect	Whether to output response. 0: No response is output from the card. 1: Responses are output from the card.
[5:0]	RW	Cmd_index	Command index.

MMC_RESP0

MMC_RESP0 is response register 0.

Offset Address	Register Name	Total Reset Value
0x0030	MMC_RESP0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Response0																															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	Response0	Bit[31:0] of a response.

MMC_RESP1

MMC_RESP1 is response register 1.

Offset Address	Register Name	Total Reset Value
0x0034	MMC_RESP1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Response1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	Response1	Bit[63:32] of a long response. After the CIU transmits an auto-stop command, the corresponding response is stored in this register, and the response to the previous command is still stored in MMC_RESP0. The auto-stop command is available only during data transfer, and the corresponding response is always a short response.

MMC_RESP2

MMC_RESP2 is response register 2.

Offset Address	Register Name	Total Reset Value
0x0038	MMC_RESP2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Response2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	Response2	Bit[95:64] of a long response.

MMC_RESP3

MMC_RESP3 is response register 3.

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Offset Address	Register Name	Total Reset Value
0x003C	MMC_RESP3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Response3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	Response3	Bit[127:96] of a long response.

MMC_MINTSTS

MMC_MINTSTS is a masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0040	MMC_MINTSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															Sdio_interrupt	Int_status															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16]	RO	Sdio_interrupt	SDIO interrupt mask status. The SDIO interrupt is valid only when MMC_INTMASK [sdio_int_mask] is enabled. 0: No SDIO interrupt is output from the card. 1: An SDIO interrupt is output from the card.

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[15:0]	RO	Int_status	Status of each interrupt. Bit[15]: end-bit error (read)/write no CRC (EBE) Bit[14]: auto command done (ACD) Bit[13]: start-bit error (SBE) Bit[12]: hardware locked write error (HLE) Bit[11]: FIFO underrun/overrun error (FRUN) Bit[10]: data starvation by the host timeout (HTO) Bit[9]: data read timeout (DTO) Bit[8]: response timeout (RTO) Bit[7]: data CRC error (DCRC) Bit[6]: response CRC error (RCRC) Bit[5]: receive FIFO data request (RXDR) Bit[4]: transmit FIFO data request (TXDR) Bit[3]: data transfer over (DTO) Bit[2]: command done (CD) Bit[1]: response error (RE) Bit[0]: card detect (CD)

MMC_RINTSTS

MMC_RINTSTS is a raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0044	MMC_RINTSTS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17	16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				Sdio_interrupt	Int_status			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16]	RW	Sdio_interrupt	Raw SDIO interrupt status. 0: No SDIO interrupt is output from the card. 1: An SDIO interrupt is output from the card. The value of the interrupt status bit is independent of the interrupt mask status.

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[15:0]	RW	Int_status	Raw status of each interrupt. Writing 1 clears the bits, and writing 0 has no effect. The value of the interrupt status bit is independent of the interrupt mask status. Bit[15]: end-bit error (read)/write no CRC (EBE) Bit[14]: auto command done (ACD) Bit[13]: start-bit error (SBE) Bit[12]: hardware locked write error (HLE) Bit[11]: FIFO underrun/overrun error (FRUN) Bit[10]: data starvation by the host timeout (HTO) Bit[9]: data read timeout (DRTO)/Boot Data Start (BDS) Bit[8]: response timeout (RTO)/Boot Ack Received (BAR) Bit[7]: data CRC error (DCRC) Bit[6]: response CRC error (RCRC) Bit[5]: receive FIFO data request (RXDR) Bit[4]: transmit FIFO data request (TXDR) Bit[3]: data transfer over (DTO) Bit[2]: command done (CD) Bit[1]: response error (RE) Bit[0]: card detect (CD)

MMC_STATUS

MMC_STATUS is a status register.

Offset Address	Register Name	Total Reset Value
0x0048	MMC_STATUS	0x0000_0106

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				FIFO_count												Response_index					data_state_mc_busy	Data_busy	Data_3_status	Commandfsm_states					Fifo_full	Fifo_empty	Fifo_tx_watermark	Fifo_rx_watermark
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved.
[29:17]	RO	FIFO_count	FIFO count.
[16:11]	RO	Response_index	Serial number of the previous response, including the response to the auto-stop command.

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[10]	RO	data_state_mc_busy	0: The data transmit/receive state machine is idle. 1: The data transmit/receive state machine is busy.
[9]	RO	Data_busy	This field value depends on the reverse level of DATA0. 0: idle (DATA0 is high level) 1: busy (DATA0 is low level)
[8]	RO	Data_3_status	Card detection signal. This field value depends on the level of DATA3. 0: No card is inserted (DATA3 is low level). 1: A card is inserted (DATA3 is high level).
[7:4]	RO	Commandfsm_states	Status of the command state machine. 0x0: idle 0x1: send init sequence 0x2: Tx cmd start bit 0x3: Tx cmd tx bit 0x4: Tx cmd index +arg 0x5: Tx cmd crc7 0x6: Tx cmd end bit 0x7: Rx resp start bit 0x8: Rx resp IRQ response 0x9: Rx resp tx bit 0xA: Rx resp cmd idx 0xB: Rx resp data 0xC: Rx resp crc7 0xD: Rx resp end bit 0xE: Cmd path wait NCC 0xF: wait, CMD-to-response turnaround
[3]	RO	Fifo_full	FIFO full flag. 0: empty 1: full
[2]	RO	Fifo_empty	FIFO empty flag. 0: not empty 1: empty
[1]	RO	Fifo_tx_watermark	Whether the FIFO reaches the transmit watermark level. 0: no 1: yes
[0]	RO	Fifo_rx_watermark	Whether the FIFO reaches the receive watermark level. 0: no 1: yes

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MMC_FIFOTH

MMC_FIFOTH is a FIFO threshold register.

Offset Address	Register Name	Total Reset Value
0x004C	MMC_FIFOTH	0x00FF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				RX_Wmark												reserved				TX_Wmark											
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	RX_Wmark	FIFO threshold watermark level during data read. If the data amount in the FIFO is above the threshold, a DMA request is enabled. After a data transfer, a DMA request is raised for transferring the remaining data no matter whether the threshold is reached. In non-DMA mode, the RXDR interrupt is enabled. If the data amount in the FIFO is not above the threshold after a data transfer, no interrupt is generated. In this case, the software needs to read the remaining data by querying the DTD interrupt. If a data transfer is complete in DMA mode, the DMA raises a single transfer request to read data until the DTD interrupt is generated even though the remaining data amount is below the threshold. Restriction: RX_WMark ≤ FIFO_DEPTH – 2 Recommendation: A request is raised when the value of [(FIFO_DEPTH/2) – 1] is above the threshold.
[15:12]	RW	reserved	Reserved.
[11:0]	RW	TX_Wmark	FIFO threshold watermark level during data transmit. If the data amount in the FIFO is below the threshold, a DMA request is enabled. After a data transfer, a DMA request is raised for transferring the remaining data no matter whether the threshold is reached. In non-DMA mode, the RXDR interrupt is enabled. If the data amount in the FIFO is not above the threshold after a data transfer, no interrupt is generated. In this case, the software needs to read the remaining data by querying the DTD interrupt. If a data transfer is complete in DMA mode, the DMA raises a single transfer request to read data until the DTD interrupt is generated even though the remaining data amount is below the threshold. Restriction: TX_WMark ≤ FIFO_DEPTH – 2 Recommendation: This filed must be less than or equal to FIFO_DEPTH/2.

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MMC_CDETECT

MMC_CDETECT is a card detection register.

Offset Address	Register Name	Total Reset Value
0x0050	MMC_CDETECT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Card_detect_n
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	Card_detect_n	Card detection signal. The value depends on the SDIO_CARD_DETECT pin.

MMC_WRTPRT

MMC_WRTPRT is a card write protection register.

Offset Address	Register Name	Total Reset Value
0x0054	MMC_WRTPRT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Write_protect
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	Write_protect	Card write protection signal. The value depends on the SDIO_CWPR pin.

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MMC_TCBCNT

MMC_TCBCNT is a count of bytes transmitted to the card register.

Offset Address	Register Name	Total Reset Value
0x005C	MMC_TCBCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	trans_card_byte_count																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	trans_card_byte_count	Count of bytes transmitted from the CIU to the card. When this register is accessed through a 32-bit AHB, the 32-bit data needs to be read at a time. This avoids the read-coherency error.

MMC_TBBCNT

MMC_TBBCNT is a count of bytes transmitted from the BIU FIFO register.

Offset Address	Register Name	Total Reset Value
0x0060	MMC_TBBCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	trans_fifo_byte_count																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	trans_fifo_byte_count	Count of bytes transferred between the CPU/DMA and BIU FIFO. When this register is accessed through a 32-bit AHB, the 32-bit data needs to be read at a time. This avoids the read-coherency error.

MMC_BMOD

MMC_BMOD is a bus mode register.

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Offset Address	Register Name	Total Reset Value
0x0080	MMC_BMOD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					PBL			DE	DSL					FB	SWR
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved.
[10:8]	RW	PBL	Length of the IDMAC burst transfer. 000: 1 001: 4 010: 8 011: 16 1xx: reserved
[7]	RW	DE	IDMAC enable. 0: disabled 1: enabled
[6:2]	RW	DSL	Span between two descriptors, that is, number of words between two non-linked descriptors. This field is valid only for the dual-buffer descriptors.
[1]	RW	FB	Fixed burst length type. 0: single and INCR burst types 1: single, INCR4, INCR8, and INCR16 burst types
[0]	RW	SWR	Soft reset control for the internal register of the IDMAC. 0: not reset 1: reset After reset, this bit is automatically cleared one clock cycle later.

MMC_PLDMND

MMC_PLDMND is a poll demand register.

Offset Address	Register Name	Total Reset Value
0x0084	MMC_PLDMND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PD																															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	PD	If DES0[OWN] is 0, the IDMAC enters the suspend state. The CPU can write any value to this register to enable the IDMAC to obtain descriptors again.

MMC_DBADDR

MMC_DBADDR is a base address register of the descriptor linked list.

Offset Address	Register Name	Total Reset Value
0x0088	MMC_DBADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SDL																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	SDL	Start address of the descriptor linked list, that is, the base address of the first descriptor.

MMC_IDSTS

MMC_IDSTS is an IDMAC status register.

Offset Address	Register Name	Total Reset Value
0x008C	MMC_IDSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																FSM				EB		AIS	NIS	reserved			CES	DU	reserved	FBE	RI	TI
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.

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[16:13]	RW	FSM	Current state of the IDMAC state machine. 0: DMA_IDLE 1: DMA_SUSPEND 2: DESC_RD 3: DESC_CHK 4: DMA_RD_REQ_WAIT 5: DMA_WR_REQ_WAIT 6: DMA_RD 7: DMA_WR 8: DESC_CLOSE This bit is read-only.
[12:10]	RW	EB	Bus error type. 001: The transmit operation is aborted. 010: The receive operation is aborted. Other values: reserved
[9]	RW	AIS	Abnormal total interrupt. The value of this bit is obtained after the values of FBE, DU, and CES bits are ORed. Writing 1 clears this bit.
[8]	RW	NIS	Normal total interrupt. The value of this bit is obtained after the values of the TI and RI bits are ORed. Writing 1 clears this bit.
[7:6]	-	reserved	Reserved.
[5]	RW	CES	Card error indicator. This bit indicates the card status when data is being received.
[4]	RW	DU	Descriptor invalid interrupt. When DES0[OWN] is 0, this bit is set to 1. Writing 1 clears this bit.
[3]	-	reserved	Reserved.
[2]	RW	FBE	Fatal bus error interrupt. If this bit is set to 1, the IDMAC stops all accesses through the bus. Writing 1 clears this bit.
[1]	RW	RI	Receive done interrupt. This bit indicates that the data of a descriptor is received. Writing 1 clears this bit.
[0]	RW	TI	Transmit done interrupt. This bit indicates that a descriptor finishes transmitting data. Writing 1 clears this bit.

MMC_IDINTEN

MMC_IDINTEN is an IDMAC interrupt enable register.

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Offset Address	Register Name	Total Reset Value
0x0090	MMC_IDINTEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						AI	NI	reserved		CES	DU	reserved	FBE	RI	TI
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	-	reserved	Reserved.
[9]	RW	AI	Abnormal interrupt enable. 0: disabled 1: The FBE, DU, and CES interrupts are enabled.
[8]	RW	NI	Normal interrupt enable. 0: disabled 1: The TI and RI interrupts are enabled.
[7:6]	-	reserved	Reserved.
[5]	RW	CES	Card error interrupt enable. 0: disabled 1: enabled
[4]	RW	DU	Descriptor invalid interrupt enable. 0: disabled 1: enabled
[3]	-	reserved	Reserved.
[2]	RW	FBE	Fatal bus error interrupt enable. 0: disabled 1: enabled
[1]	RW	RI	Receive interrupt enable. 0: disabled 1: enabled
[0]	RW	TI	Transmit interrupt enable. 0: disabled 1: enabled

MMC_DSCADDR

MMC_DSCADDR is an address register of the current descriptor.

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Offset Address	Register Name	Total Reset Value
0x0094	MMC_DSCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HAD																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	HAD	Descriptor pointer. The value is automatically refreshed during data transfer. The register points to the start address of the descriptor that will be used by the IDMAC.

MMC_BUFADDR

MMC_BUFADDR is an address register of the current data buffer.

Offset Address	Register Name	Total Reset Value
0x0098	MMC_BUFADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HBA																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	HBA	Data buffer pointer. The value is automatically refreshed during data transfer. The register points to the start address of the data buffer that is being used by the IDMAC.

MMC_DATA

MMC_DATA is a data register for storing the FIFO entrance address. Before the FIFO is read or written, MMC_STATUS[fifo_count] must be read to query the remaining space of the FIFO. This confirms the data bytes to be read or written based on the remaining space. In this way, FIFO overflow is avoided.

Offset Address	Register Name	Total Reset Value
0x0100	MMC_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA																															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	DATA	Address for reading/writing to the FIFO. If the address ranges from 0x100 to 0x100+FIFO_DEPTH, the FIFO is selected.

14.8 SATA

14.8.1 Overview

The serial advanced technology attachment (SATA) interface of the Hi3521 is an advanced high-performance bus (AHB) interface that complies with advanced microcontroller bus architecture (AMBA) 2.0. This interface is used to implement rapid integration on the system-on-chip (SoC) system. With the drivers developed in Linux, the SATA interface helps software engineers customize and develop the drivers of the SoC subsystem rapidly. The Hi3521 supports a maximum of two SATA interfaces. At the controller layer, the SATA interface supports native command queuing (NCQ), hot plugging, port multiplier and eSATA.

14.8.2 Features

The SATA interface of the Hi3521 provides the following features:

- Provides the ARM AHB slave interface that complies with AMBA Spec 2.0. Only the 32-bit access mode is supported.
- Provides the ARM AHB master interface that complies with AMBA Spec 2.0. Only the 32-bit access mode is supported.
- Provides a standard signal interface for connecting to the PHY.
- Supports the protocols SATA2.5 and Advanced Host Controller Interface 1.2 (AHCI1.2).
- Supports programmable input/output (PIO), legacy DMA, NCQ, and advanced technology attachment packet interface (ATAPI) operations.
- Supports power supply management.
- Supports the port multiplier.
- Supports a maximum of two SATA ports.
- Supports automatic rate negotiation: 1.5 Gbps or 3.0 Gbps.
- Supports the interrupt report mechanism.

14.8.3 Signal Description

Table 14-23 describes the signals of the SATA interface.

Table 14-23 Signals of the SATA interface

Signal	Direction	Description	Corresponding Pin
SREFCKM	I	SATA negative differential clock input	SREFCKM

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Signal	Direction	Description	Corresponding Pin
SREFCKP	I	SATA positive differential clock input	SREFCKP
SRESREF	I/O	SATA extended resistor pin, connected to external extended resistors	SRESREF
SRXM0	I	Negative differential data input of SATA port0	SRXM0
SRXM1	I	Negative differential data input of SATA port1	SRXM1
SRXP0	I	Positive differential data input of SATA port0	SRXP0
SRXP1	I	Positive differential data input of SATA port1	SRXP1
STXM0	O	Negative differential data output of SATA port0	STXM0
STXM1	O	Negative differential data output of SATA port1	STXM1
STXP0	O	Positive differential data output of SATA port 0	STXP0
STXP1	O	Positive differential data output of SATA port1	STXP1

14.8.4 Function Description

Typical Application

Figure 14-56, Figure 14-57, and Figure 14-58 show the typical application modes of the SATA interface.

Figure 14-56 Typical application mode 1

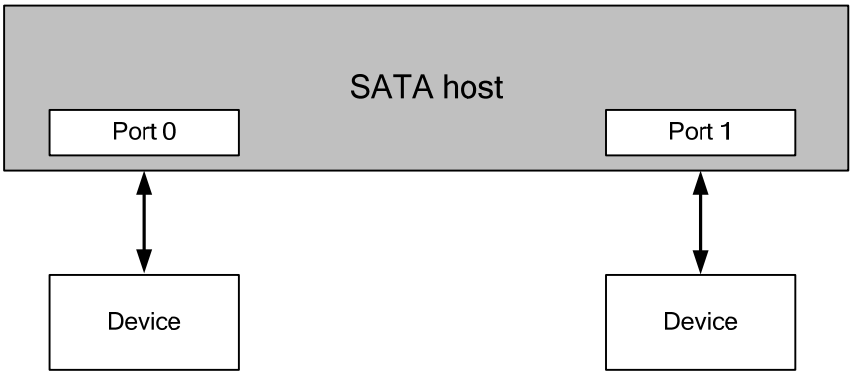

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Figure 14-57 Typical application mode 2

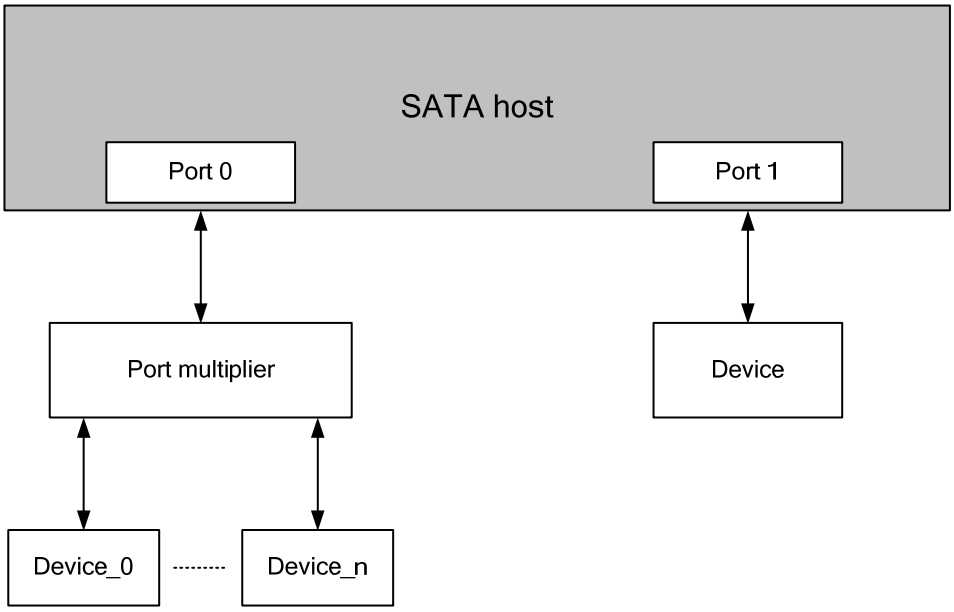
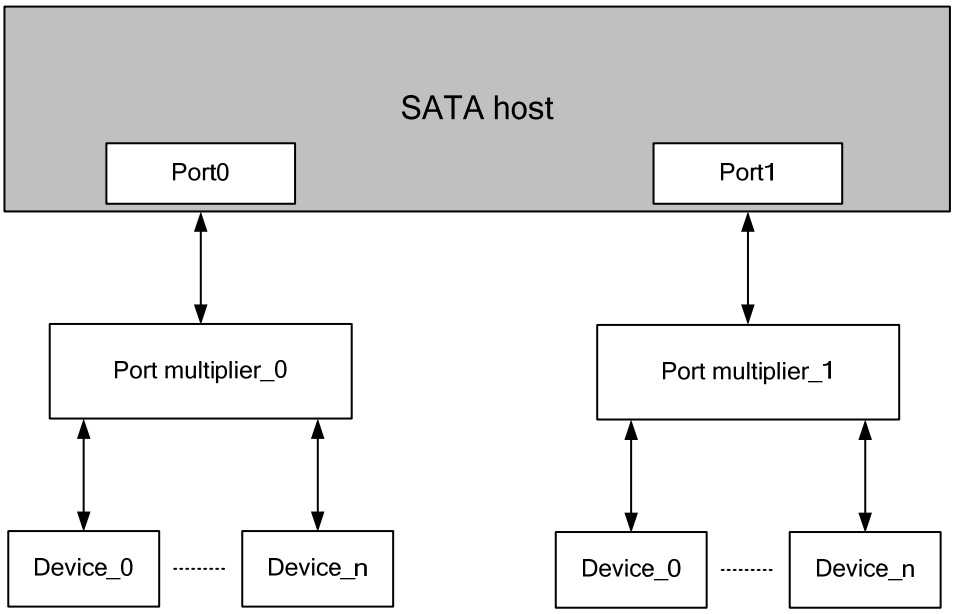


Figure 14-58 Typical application mode 3



The SATA Host can be directly connected to a maximum of two devices such as the hard disk and drive. In addition, any of the port of the SATA Host can be connected to the port multiplier. The number of connected external devices depends on the expansion capability of the port multiplier.

Function Principle

Figure 14-59 shows the architecture of the Hi3521 SATA module.

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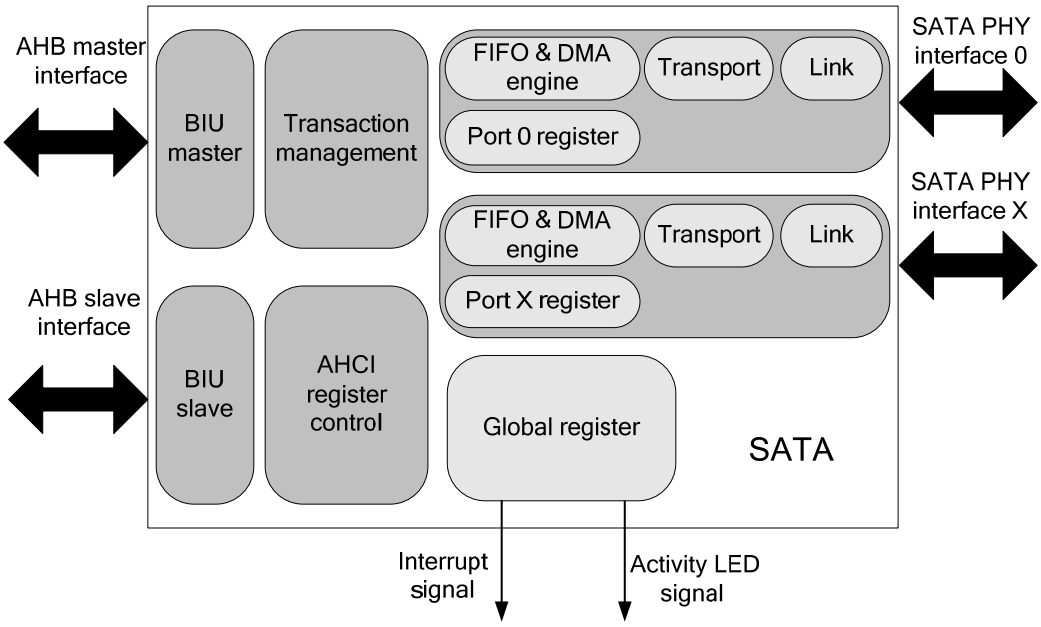
Figure 14-59 Architecture of the Hi3521 SATA module



The AHB master and AHB slave interfaces are mounted on the system bus AHB that complies with ARM AMBA2.0. The ARM CPU and system memory controller are also located on the system bus. The software configures the SATA module by using the AHB slave interface. Through the AHB master interface, the dynamic random access memory (DRAM) of the system memory controller is accessed to read commands and data and write data.

The SATA Host supports the PIO, legacy DMA, NCQ, and ATAPI operations.

The interrupt signal is connected to the system interrupt controller.

In the Hi3521, the SATA PHY interface is connected to the SATA PHY. Outside the Hi3521, the SATA PHY can be connected to the hard disk or drive with the SATA interface or be connected to a SATA port multiplier for port expansion.

The activity light emitting diode (LED) signal can be directly transferred from the Hi3521. You can choose this function as required.

14.8.5 Operating Mode

14.8.5.1 Clock Gating

WhenPERI_CRG45[sata0_cken] and PERI_CRG45[sata1_cken] is set to 1, the SATA clock is enabled. You can disable the SATA clock by setting PERI_CRG45[sata0_cken] and PERI_CRG45[sata1_cken] to 1.

14.8.5.2 Clock Configuration

You can configure the internal control register SATA_PHY0_CTLH bit[13] of the SATA Host to select the reference clock source of the SATA PHY. That is, you can control whether the clock of the SATA PHY is generated in the Hi3521 or supplied by the external clock source. The details are as follows:

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- When SATA_PHY0_CTLH bit[13] is set to 1, the clocks SREFCKM and SREFCKP are generated in the Hi3521.
- When SATA_PHY0_CTLH bit[13] is set to 0, the clocks SREFCKM and SREFCKP are supplied by the external clock source.

The reference clock supported by the SATA PHY ranges from 25 MHz to 156.25 MHz. The input clock supported by the internal multiplying phase-locked loop (MPLL) of the PHY ranges from 50 MHz to 78.125 MHz. Therefore, when the reference clock is changed, you must configure SATA_PHY0_CTLL bit[31:30] of the SATA Host to meet the clock requirement of the internal MPLL of the SATA PHY. For details, see the description of SATA_PHY0_CTLL bit[31:30].

14.8.5.3 Soft Reset

The following shows multiple soft reset control modes of the SATA Host:

- Set PERI_CRG45 bit[7] to 1 to soft-reset only the sata_alive clock domain.
- Set PERI_CRG45 bit[6] to 1 to soft-reset only the sata_rx clock domain of port1.
- Set PERI_CRG45 bit[5] to 1 to soft-reset only the sata_rx clock domain of port0.
- Set PERI_CRG45 bit[4] to 1 to soft-reset only the sata_tx clock domain of port1.
- Set PERI_CRG45 bit[3] to 1 to soft-reset only the sata_tx clock domain of port0.
- Set PERI_CRG45 bit[0] to 1 to soft-reset only the SATA PHY.
- Set PERI_CRG45 bit[1] to 1 to soft-reset only the HCLK clock domain.
- Set PERI_CRG45 bit[2]to 1 to soft-reset the SATA Host.

The SATA Host controller also provides the following two synchronous reset modes:

- When SATA_GHC_GHC bit[0] of the SATA Host controller is set to 1, the SATA Host switches to the reset mode. In this case, the logic of all internal modules is restored to initial values. After reset, SATA_GHC_GHC bit[0] is cleared automatically.
- When the value of SATA_PORT_CMD bit[0] corresponding to port0 or port1 is changed from 1 to 0, port0 or port1 enters the reset mode.

14.8.5.4 Setting the Operating Mode

Before starting the SATA Host, you must initialize the SATA PHY to ensure proper running of the SATA PHY and perform initialization negotiation between the SATA Host and SATA Device.

Initializing the SATA PHY

The following is an example using the 125 MHz internal PHY reference clock. To initialize 1.5 Gbps port0, perform the following steps:Set PERI_CRG45 bit [11] to 0 to select the 125 MHz CRG output reference clock.

Step 2 Set PERI_CRG45 bit [1] to 0 to deassert the soft reset on the SATA controller bus.

Step 3 Set PERI_CRG45 bit [0] to 0 to deassert the soft reset on the SATA PHY.

Step 4 Set SATA_PHY0_CTLH bit[12] to disable the provided PHY reference clock.

Step 5 Set SATA_PHY0_CTLL to 0x8A0E_C788 (set SATA_PHY0_CTLL to 0x8A0E_C888 when the SATA interface works in 3G mode).

Step 6 Set SATA_PHY0_CTLH to 0x2121.

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Step 7 Set SATA_OOB_CTL to 0x8406_0C15.

Step 8 Set SATA_PORT_PHYCTL to 0x0E26_2709 (set SATA_PORT_PHYCTL to 0x0E66_2709 when the SATA interface works in 3G mode).

Step 9 Set PERI_CRG45 bit[0] to 1 to soft-reset the SATA PHY.

Step 10 Set PERI_CRG45 bit [0] to 0 to deassert the soft reset on the SATA PHY.

Step 11 Set PERI_CRG45 bit [2] to 0 to deassert the soft reset on the SATA controller interface.

Step 12 Set PERI_CRG45 bit [3] to 0 to deassert the soft reset on the SATA controller tx0 clock domain.

Step 13 SetPERI_CRG45 bit [5] to 0 to deassert the soft reset on the the SATA controller rx0 clock domain.

Step 14 Set PERI_CRG45 bit [7] to 0 to deassert the soft reset on the SATA controller alive clock domain.

---End

Initialization Negotiation

After the PLL of the SATA PHY works properly, initialization negotiation is performed between the SATA Host and SATA Device as follows:

Step 1 Set SATA_PORT_CMD[cmd_sud] to 1.

Step 2 Wait until the indication signal phyrdy from the SATA PHY is valid and check whether SATA_PORT_SSTS[pxssts_det] is 3. If SATA_PORT_SSTS[pxssts_det] is 3, the corresponding port works properly and initialization is successful.

---End

Running Services

After initialization negotiation, start services as follows:

Step 1 Clear interrupts (skip this step after reset or if services are started initially). To be specific, set the values of SATA_PORT_SERR, SATA_PORT_IS, and SATA_GHC_IS to 0xFFFFFFFF.

Step 2 Configure the interrupt mask register SATA_PORT_IE to mask the interrupts that do not need to be reported.

Step 3 Enable the global interrupt by setting SATA_GHC_GHC to 0x80000002.

Step 4 Set up a linked list based on SATA command linked list format of the appendix A.

Step 5 Set the base address of the port command lists in the memory by configuring SATA_PORT_CLB[port_clb] and notify the transmit DMAC of the position for storing the commands and data to be read. The configured base address is the memory base address allocated for the port command lists.

Step 6 Set the base address in the memory for storing the frames received through the port by configuring SATA_PORT_FB[port_fb] and notify the receive DMAC of the position for storing the received frame information structures (FISs). The configured base address is the memory base address allocated for the port receive frames.

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Step 7 Set SATA_PORT_CMD[st] to 1 to enable the transmit DMAC to transmit commands and data; set SATA_PORT_CMD[cmd_fre] to 1 to enable the receive DMAC to receive FISs and write them to the system memory.

Step 8 Configure the port command transmit control register SATA_PORT_CI to specify the command to be transmitted.

Step 9 Transmit the commands and data.

Step 10 Check whether the current command is complete through the interrupt bit and command execution status. When interrupts are received, check whether all the CI bits are cleared for the PIO or DMA operation and check the CI and SACT bits are cleared for the NCQ operation.

Step 11 Repeat step 1 to step 10 for the next transfer if necessary.

---End

NOTE

Perform the operations of legacy DMA, PIO, and ATAPI according to the preceding steps. The linked lists (such as the command codes and flag bits), however, are different for theses operations.

For the NCQ operation, besides a different linked list, SATA_PORT_SACT also needs to be configured to indicate the number of executed commands during the NCQ operation. To be specific, configure SATA_PORT_SACT after step 7, and ensure that the positions of the commands configured by SATA_PORT_SACT map to those of the commands in SATA_PORT_CI.

14.8.6 Register Summary

The letter *n* in the offset addresses of registers indicates the port ID of the controller and its value is 0 or 1.

SATA Register Summary

Table 14-24 describes the SATA registers.

Table 14-24 Summary of the SATA registers (base address: 0x1008_0000)

Offset Address	Register	Description	Page
0x0000	SATA_GHC_CAP1	Feature support register 1	14-151
0x0004	SATA_GHC_GHC	Global Control Registers	14-152
0x0008	SATA_GHC_IS	Interrupt status register	14-153
0x000C	SATA_GHC_PI	Port implementation register	14-154
0x0010	SATA_GHC_VS	AHCI version identifier register	14-154
0x0014	SATA_GHC_CCC_CTL	Command completion coalescing (CCC) control register	14-155
0x0018	SATA_GHC_CCC_PORTS	CCC port enable register	14-156
0x0024	SATA_GHC_CAP2	Feature support register 2	14-156

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Offset Address	Register	Description	Page
0x0028	SATA_GHC_BOHC	Basic input/output system (BIOS)/operating system (OS) handoff control register	14-157
0x0050	SATA_GHC_TM	TM test status register	14-158
0x0054	SATA_PHY0_CTLL	PHY0 global register for lower bits	14-159
0x0058	SATA_PHY0_CTLH	PHY0 global register for upper bits	14-160
0x005C	SATA_PHY0_STS	PHY0 global status register	14-161
0x006C	SATA_OOB_CTL	PHY out of band (OOB) control register	14-162

SATA_PORT_CFG Register Summary

Table 14-25 describes the SATA_PORT_CFG registers.

Table 14-25 Summary of the SATA_PORT_CFG registers (base address: 0x1008_0100)

Offset Address	Register	Description	Page
0x000+nx0x80	SATA_PORT_CLB	Command list base address register	14-162
0x008+nx0x80	SATA_PORT_FB	Receive FIS base address register	14-163
0x010+nx0x80	SATA_PORT_IS	Port interrupt status register	14-163
0x014+nx0x80	SATA_PORT_IE	Port interrupt mask register	14-165
0x018+nx0x80	SATA_PORT_CMD	Port command and status register	14-167
0x20+nx0x80	SATA_PORT_TFD	Port task file register	14-169
0x24+nx0x80	SATA_PORT_SIG	Port signature register	14-170
0x028+nx0x80	SATA_PORT_SSTS	Port status register	14-171
0x02C+nx0x80	SATA_PORT_SCTL	Port control register	14-171
0x30+nx0x80	SATA_PORT_SERR	Error diagnosis status register	14-172
0x034+nx0x80	SATA_PORT_SACT	NCQ command identifier control register	14-174
0x38+nx0x80	SATA_PORT_CI	Command transmit control register	14-174
0x3C+nx0x80	SATA_PORT_SNTF	Async notification event indication register	14-175
0x044+nx0x80	SATA_PORT_FIFOTH	Receive FIFO threshold register	14-175

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Offset Address	Register	Description	Page
0x050+nx0x80	SATA_PORT_HBA	Host bus adapter (HBA) test status register	14-176
0x054+nx0x80	SATA_PORT_LINK	Link test status register	14-177
0x058+nx0x80	SATA_PORT_DMA1	DMAC test status register 1	14-178
0x05C+nx0x80	SATA_PORT_DMA2	DMAC test status register 2	14-179
0x060+nx0x80	SATA_PORT_DMA3	DMAC test status register 3	14-179
0x064+nx0x80	SATA_PORT_DMA4	DMAC test status register 4	14-179
0x068+nx0x80	SATA_PORT_DMA5	DMAC test status register 5	14-180
0x6C+nx0x80	SATA_PORT_DMA6	DMAC test status register 6	14-181
0x070+nx0x80	SATA_PORT_DMA7	DMAC test status register 7	14-181
0x074+nx0x80	SATA_PORT_PHYCTL	PHY control register	14-182
0x078+nx0x80	SATA_PORT_PHYSTS	PHY test status register	14-184

14.8.7 Register Description

SATA_GHC_CAP1

SATA_GHC_CAP1 is feature support register 1.

Offset Address	Register Name	Total Reset Value
0x0000	SATA_GHC_CAP1	0x6F26_FFA1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s64a	sncq	ssntf	smps	sss	salp	sal	sclo	iss				reserved	sam	spm	fbss	pmd	ssc	psc	ncs					cccs	ems	sxs	np				
Reset	0	1	1	0	1	1	1	1	0	0	1	0	0	1	1	0	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	1

Bits	Access	Name	Description
[31]	RO	s64a	Fixed at 0, indicating that the 64-bit data structure cannot be accessed.
[30]	RO	sncq	Fixed at 1, indicating that NCQ is supported.
[29]	RO	ssntf	Fixed at 1, indicating that the port SNTF register is supported.
[28]	RO	smps	Fixed at 0, indicating that mechanical hot-plugging is not supported.
[27]	RO	sss	Fixed at 1, indicating that staggered spin-up is supported.

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[26]	RO	salp	Fixed at 1, indicating that power supply management is supported.
[25]	RO	sal	Fixed at 1, indicating that the LED pin is supported.
[24]	RO	sclo	Fixed at 1, indicating that command linked list override is supported.
[23:20]	RO	iss	Fixed at 0x2, indicating that the maximum rate of 3 Gbit/s is supported.
[19]	RO	reserved	Reserved.
[18]	RO	sam	Fixed at 1, indicating that only the AHCI mode is supported.
[17]	RO	spm	Fixed at 1, indicating that the port multiplier is supported.
[16]	RO	fbss	Fixed at 0, indicating that FIS-based switching is not supported.
[15]	RO	pmd	Fixed at 1, indicating that multiple DRQ blocks cannot be transferred in PIO mode.
[14]	RO	ssc	Fixed at 1, indicating that the transition to the slumber status is supported.
[13]	RO	psc	Fixed at 1, indicating that the transition to the partial status is supported.
[12:8]	RO	ncs	Fixed at 0x1F, indicating that 32 command slots are supported.
[7]	RO	cccs	Fixed at 1, indicating that the CCC function is supported.
[6]	RO	ems	Fixed at 0, indicating that enclose management is not supported.
[5]	RO	sxs	Fixed at 1, indicating that the external SATA interface is supported.
[4:0]	RO	np	Fixed at 0x01, indicating that a maximum of two ports are supported.

SATA_GHC_GHC

SATA_GHC_GHC is a global control register.

Offset Address	Register Name	Total Reset Value
0x0004	SATA_GHC_GHC	0x8000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ahci_en	reserved																													int_enable	hba_rst

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Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	ahci_en	Fixed at 1, indicating that the software can interact with the controller only through the AHCI mechanism.
[30:2]	RO	reserved	Reserved.
[1]	RW	int_enable	Controller interrupt enable. 0: disabled 1: enabled
[0]	RW	hba_rst	Soft reset control for the controller. 0: not reset 1: reset Writing 1 resets the controller and this bit is automatically cleared after reset; writing 0 has no effect. In addition, reset has no effect on the registers SATA_GHC_BOHC, SATA_PORT_FB, and SATA_PORT_CLB.

SATA_GHC_IS

SATA_GHC_IS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0008	SATA_GHC_IS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ips_ccc	reserved																													ips_port1	ips_port0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	WC	ips_ccc	CCC interrupt status. 0: No CCC interrupt is generated. 1: A CCC interrupt is generated.
[30:2]	RO	reserved	Reserved.
[1]	WC	ips_port1	Interrupt status of port 1. 0: No interrupt is reported. 1: An interrupt is reported.
[0]	WC	ips_port0	Interrupt status of port 0. 0: No interrupt is reported. 1: An interrupt is reported.

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SATA_GHC_PI

SATA_GHC_PI is a port implementation register.

Offset Address	Register Name	Total Reset Value
0x000C	SATA_GHC_PI	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												port_imp			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3:0]	RO	port_imp	Port validity indication. If the value is 0x3, the four ports, port 0 to port 1, are valid. The bits, bit[1] to bit[0], map to port 1 to port 0 respectively. 0: The ports are invalid. 1: The ports are valid.

SATA_GHC_VS

SATA_GHC_VS is an AHCI version identifier register.

Offset Address	Register Name	Total Reset Value
0x0010	SATA_GHC_VS	0x0001_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	achi_vs																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	achi_vs	The supported AHCI version is V1.2.

SATA_GHC_CCC_CTL

SATA_GHC_CCC_CTL is a CCC control register.

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Offset Address	Register Name	Total Reset Value
0x0014	SATA_GHC_CCC_CTL	0x0001_01F8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ccc_tv																ccc_cc								ccc_int						reserved	ccc_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:16]	RW	ccc_tv	CCC timeout parameter, in the unit of ms. When the CCC function is enabled, the timeout counter loads this parameter value. If a command is executed on a port involved in CCC counting, the counter decreases by 1 every 1 ms until a CCC interrupt is generated when the counter reaches 0. Then the counter reloads the parameter value for the next counting. Note that these bits cannot be set to 0s.
[15:8]	RW	ccc_cc	CCC command completion upper limit. When the CCC function is enabled, the counter is cleared after commands are executed. Then the counter starts to count the number of completed commands on the ports involved in CCC counting. If the count value is greater than or equal to the parameter value, a CCC interrupt is generated. In this case, the counter is cleared again for the next counting. If the value 0 is written, the command completion interrupt is disabled and the CCC interrupt is generated only after timeout.
[7:3]	RO	ccc_int	CCC interrupt vector ID. If the value is 0x1F (31), SATA_GHC_IS bit[31] indicates the CCC interrupt status.
[2:1]	RO	reserved	Reserved.
[0]	RW	ccc_en	CCC function enable. 0: disabled 1: enabled When the CCC function is enabled, the values of ccc_tv and ccc_cc cannot be changed.

SATA_GHC_CCC_PORTS

SATA_GHC_CCC_PORTS is a CCC port enable register.

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Offset Address	Register Name	Total Reset Value
0x0018	SATA_GHC_CCC_PORTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														ccc_prt	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1:0]	RW	ccc_prt	Specifies the port that is involved in CCC counting. Bit[1] to bit[0] map to port 1 to port 0 respectively. If the related bit is 1, the port is involved in CCC counting. If the related bit is 0. The port is not involved in CCC counting. The value of this register can be changed at any time and the changed value takes effect immediately.

SATA_GHC_CAP2

SATA_GHC_CAP2 is feature support register 2.

Offset Address	Register Name	Total Reset Value
0x0024	SATA_GHC_CAP2	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														cap_boh	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	cap_boh	Fixed at 1, indicating that BIOS/OS handoff control is supported.

SATA_GHC_BOHC

SATA_GHC_BOHC is a BIOS/OS handoff control register.

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Offset Address	Register Name	Total Reset Value
0x0028	SATA_GHC_BOHC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											bohc_bb	bohc_ooc	bohc_sooe	bohc_oos	bohc_bos
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4]	RW	bohc_bb	BIOS status indication. 0: The BIOS is not busy. 1: The BIOS is busy in performing certain operations and is ready to hand the control permission off to the OS.
[3]	WC	bohc_ooc	When the value of bohc_oos is changed from 0 to 1, this bit is fixed at 1. Writing 1 clears this bit and writing 0 has no effect.
[2]	RW	bohc_sooe	Message interrupt enable. 0: No message interrupt is generated. 1: When bohc_ooc is set to 1, a message interrupt is generated.
[1]	RW	bohc_oos	Request applied by the OS for controlling the controller. 0: The OS does not apply for the control permission on the controller. 1: The OS applies for the control permission on the controller. If bohc_oos is 1 and bios_bos is 0, it indicates that the OS has obtained the control permission on the SATA controller. Resetting the SATA controller through SATA_GHC_GHC[hab_rst] has no effect on this bit.
[0]	RW	bohc_bos	Flag that indicates that the BIOS has the control permission on the controller. 0: The BIOS does not have the control permission on the controller. 1: The BIOS has the control permission on the controller. If the OS applies for the control permission on the controller, the BIOS clears this bit. Resetting the SATA controller through SATA_GHC_GHC[hab_rst] has no effect on this bit.

SATA_GHC_TM

SATA_GHC_TM is a TM test status register.

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Offset Address	Register Name	Total Reset Value
0x0050	SATA_GHC_TM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														req_sel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2:0]	RO	req_sel	Current DMAC that has the right to use the AHB master. 0x0: transmit DMAC of port 0 0x1: receive DMAC of port 0 0x2: transmit DMAC of port 1 0x3: receive DMAC of port 1 Other values: reserved

SATA_PHY0_CTLL

SATA_PHY0_CTLL is a PHY0 global status register for lower bits.

Offset Address	Register Name	Total Reset Value
0x0054	SATA_PHY0_CTLL	0x8D0E_C88A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mpll_prescale		mpll_ncy					mpll_ncy5	mpll_int_ctl				mpll_prop_ctl				tx_lvl				los_lvl				acjt_lvl				fast_tech		pddq_h	
Reset	1	0	0	0	1	1	0	1	0	0	0	0	1	1	1	0	1	1	0	0	1	0	0	0	1	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:30]	RW	mpll_prescale	When the reference clock is changed, this value also needs to be changed. 00: ref_clk is used as it is. 01: ref_clk is multiplied by 2. 10: ref_clk is divided by 2. 11: reserved
[29:25]	RW	mpll_ncy	Operating parameter of the internal MPLL of the PHY. This field needs to be used with mpll_ncy5 and indicates the used multiplier.

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[24:23]	RW	mpll_ncy5	Operating parameter of the internal MPLL of the PHY. This field needs to be used with mpll_ncy and indicates the used multiplier.
[22:20]	RW	mpll_int_ctl	Internal bandwidth control and select signal of the MPLL. This field must be set to 0b000.
[19:17]	RW	mpll_prop_ctl	Internal proportional bandwidth control signal of the MPLL. This field must be set to 0b111 and can be written only when the register is reset or the MPLL is invalid.
[16:12]	RW	tx_lvl	Transmit level parameter that is related to the selected SATA protocol. This field must be set to 0b01100.
[11:7]	RW	los_lvl	LOS detection level control signal. This field must be set to 0b10001.
[6:2]	RW	acjt_lvl	ACJTAG receiver comparator level control signal. This field must be set to 0b00010.
[1]	RW	fast_tech	Signal that indicates that the IP is processed in a fast technology variant. This bit must be set to 0.
[0]	RW	pddq_h	IDDQ test signal. To perform an IDDQ test, all the lanes and support blocks must be powered off before pddq_h is valid. In normal mode, this bit must be set to 0.

SATA_PHY0_CTLH

SATA_PHY0_CTLH is a PHY0 global register for upper bits.

Offset Address	Register Name	Total Reset Value
0x0058	SATA_PHY0_CTLH	0x0000_2121

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		use_refclk_alt	mpll_ck_off	mpll_pwron	mpll_ss_en	cko_word_con				cko_alive_con		rtune_do_tune		reserved		reserved		reset_n	wide_xface
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	1

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.
[13]	RW	use_refclk_alt	PHY reference clock select. 0: refclk differential signals 1: refclk_alt differential signals

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[12]	RW	mpll_ck_off	Power-on control signal of the MPLL. Control this signal by conforming to the following rules: 1. Before providing refclk to the MPLL, set mpll_ck_off to 0. 2 Before setting mpll_ck_off to 0, set mpll_ncy, mpll_ncy5, and, pll_prescale to proper values. 3 If refclk is paused or switched or the values of mpll_ncy, mpll_ncy5, and mpll_prescale need to be changed, set mpll_ck_off to 1 first.
[11]	RW	mpll_pwron	MPLL power-on. 0: The cko_word clock is invalid. 1: The internal MPLL is reset and the cko_word clock signal is generated based on the frequency of refclk. Before the MPLL is disabled, tx_en must be OFF or in the CM status and rx_en and rx_pll_pwron must be set to 0.
[10]	RW	mpll_ss_en	Spread spectrum enable signal. 0: disabled 1: enabled If the refclk spectrum has been spread, this bit must be set to 0.
[9:7]	RW	cko_word_con	cko_word output select signal. This field must be set to 0b111.
[6:5]	RW	cko_alive_con	cko_alive output signal select. 00: invalid. 01: retain the output frequency of the prescaler. 10: low-frequency output, that is, 1/16 of the prescaler. 11: reserved
[4]	RW	rtune_do_tune	Resistor tune enable signal. 0: do not tune 1: retune the resistor
[3]	RO	reserved	Reserved.
[2]	RO	reserved	Reserved.
[1]	RW	reset_n	Reset signal. This signal must be retained for 5 ns at least.
[0]	RW	wide_xface	Interface bit width control signal. 0: 10 bits 1: 20 bits

SATA_PHY0_STS

SATA_PHY0_STS is a PHY0 global status register.

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Offset Address	Register Name	Total Reset Value
0x005C	SATA_PHY0_STS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	phy0_sts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	phy0_sts	SATA PHY0 common status register.

SATA_OOB_CTL

SATA_OOB_CTL is a PHY OOB control register.

Offset Address	Register Name	Total Reset Value
0x006C	SATA_OOB_CTL	0x8406_0C15

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	oob_ctrl_valid	min_comiwake							max_comwake								min_cominit								max_cominit							
Reset	1	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	0	0	0	0	1	0	1	0	1

Bits	Access	Name	Description
[31]	RW	oob_ctrl_valid	Configuration bit of the OOB detection parameter. For high level, this bit is used to select the parameter configurations of this register.
[30:24]	RW	min_comiwake	Minimum space required for the COMWAKE space detection.
[23:16]	RW	max_comwake	Maximum space required for the COMWAKE space detection.
[15:8]	RW	min_cominit	Minimum space required for the COMINIT space detection.
[7:0]	RW	max_cominit	Maximum space required for the COMINIT space detection.

SATA_PORT_CLB

SATA_PORT_CLB is a command list base address register.

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Offset Address	Register Name	Total Reset Value
0x000+nx0x80	SATA_PORT_CLB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	port_clb																						reserved									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RW	port_clb	Base address for storing the port command list in the memory. Resetting the SATA controller through SATA_GHC_GHC[hab_rst] has no effect on this field.
[9:0]	RO	reserved	Reserved.

SATA_PORT_FB

SATA_PORT_FB is a receive FIS base address register.

Offset Address	Register Name	Total Reset Value
0x008+nx0x80	SATA_PORT_FB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	port_fb																								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	port_fb	Base address in the memory for storing the frames received through the port. Resetting the SATA controller through SATA_GHC_GHC[hab_rst] has no effect on this field.
[7:0]	RO	reserved	Reserved.

SATA_PORT_IS

SATA_PORT_IS is a port interrupt status register.

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Offset Address	Register Name	Total Reset Value
0x010+nx0x80	SATA_PORT_IS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	pxis_tfes	reserved	pxis_hbds	pxis_ifs	pxis_infs	reserved	pxis_ofs	pxis_ipms	pxis_prcs	reserved															pxis_pcs	pxis_dps	pxis_ufs	pxis_sdbs	pxis_dss	pxis_pss	pxis_drhs
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30]	WC	pxis_tfes	Task file data (TFD) error interrupt status. 0: The value of SATA_PORT_TFD bit[0] is not 1. 1: The value of SATA_PORT_TFD bit[0] is 1.
[29]	RO	reserved	Reserved.
[28]	WC	pxis_hbds	Internal bus error interrupt. 0: The DMAC accesses the memory properly. 1: An error occurs when the DMAC accesses the memory.
[27]	WC	pxis_ifs	Fatal error interrupt status. 0: No error occurs during the data frame transfer. 1: An error occurs during the data frame transfer.
[26]	WC	pxis_infs	Non-fatal error interrupt status. 0: No error occurs during the non-data frame transfer. 1: An error occurs during the non-data frame transfer.
[25]	RO	reserved	Reserved.
[24]	WC	pxis_ofs	Data transfer overflow interrupt status. 0: No overflow is detected. 1: During the data frame transfer, if the size of the data memory occupied by commands is smaller than the actual data amount, an interrupt is reported at the end of the data transfer.
[23]	WC	pxis_ipms	PM port number error interrupt status. 0: No PM port number error is detected during data reception. 1: A PM port number error is detected during data reception.
[22]	RO	pxis_prcs	PHY status change interrupt status. 0: No changes of the phyrdy signal are detected. 1: Changes of the phyrdy signal are detected. This bit directly reflects the value of SATA_PORT_SERR[diag_n].
[21:7]	RO	reserved	Reserved.

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[6]	RO	pxis_pcs	Port connection change interrupt status. 0: No COMINIT signal transmitted from the device is detected. 1: A COMINIT signal transmitted from the device is detected. This bit directly reflects the value of SATA_PORT_SERR[diag.x].
[5]	WC	pxis_dps	Linked list transfer completion interrupt status. 0: The transfer of the linked list data is complete when no I bit in the PRD is 1. 1: The transfer of the linked list data is complete when an I bit in the PRD is 1.
[4]	RO	pxis_ufs	Unknown FIS interrupt status. 0: No unknown FIS is received. 1: An unknown FIS is received.
[3]	WC	pxis_sdbs	Set device bits FIS interrupt status. 0: no effect 1: A set device bits FIS is received and the I bit is 1.
[2]	WC	pxis_dss	DMA setup FIS interrupt status. 0: no effect 1: A DMA setup FIS is received and the I bit is 1.
[1]	WC	pxis_pss	PIO setup FIS interrupt status. 0: no effect 1: A PIO setup FIS is received and the I bit is 1.
[0]	WC	pxis_drhs	D2H register FIS interrupt status. 0: no effect 1: A D2H register FIS is received and the I bit is 1.

SATA_PORT_IE

SATA_PORT_IE is a port interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x014+nx0x80	SATA_PORT_IE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	pxie_tfee	reserved	pxie_hbde	pxie_ife	pxie_infe	reserved	pxie_ofe	pxie_ipme	pxie_prce	reserved														pxie_pce	pxie_dpe	pxie_ufe	pxie_sdbe	pxie_dse	pxie_pse	pxie_drhe
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.

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[30]	RW	pxie_tfee	TFD error interrupt mask. 0: masked 1: not masked
[29]	RO	reserved	Reserved.
[28]	RW	pxie_hbde	Internal bus error interrupt mask. 0: masked 1: not masked
[27]	RW	pxie_ife	Fatal error interrupt mask. 0: masked 1: not masked
[26]	RW	pxie_infe	Non-fatal error interrupt mask. 0: masked 1: not masked
[25]	RO	reserved	Reserved.
[24]	RW	pxie_ofe	Data transfer overflow interrupt mask. 0: masked 1: not masked.
[23]	RW	pxie_ipme	PM port error interrupt mask. 0: masked 1: not masked
[22]	RW	pxie_prce	PHY status change interrupt mask. 0: masked 1: not masked
[21:7]	RO	reserved	Reserved.
[6]	RW	pxie_pce	Port connection change interrupt mask. 0: masked 1: not masked
[5]	RW	pxie_dpe	Linked list transfer completion interrupt mask. 0: masked 1: not masked
[4]	RW	pxie_ufe	Unknown FIS interrupt mask. 0: masked 1: not masked
[3]	RW	pxie_sdbe	Set device bits FIS interrupt mask. 0: masked 1: not masked

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[2]	RW	pxie_dse	DMA setup FIS interrupt mask. 0: masked 1: not masked
[1]	RW	pxie_pse	PIO setup FIS interrupt mask. 0: masked 1: not masked
[0]	RW	pxie_drhe	D2H register FIS interrupt mask. 0: masked 1: not masked

SATA_PORT_CMD

SATA_PORT_CMD is a port command and status register.

Offset Address	Register Name	Total Reset Value
0x018+nx0x80	SATA_PORT_CMD	0x0020_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cmd_icc				cmd_asp	cmd_alpe	cmd_dlae	cmd_atapi	reserved		cmd_esp	reserved			cmd_pma	reserved	cmd_cr	cmd_fr	reserved		cmd_ccs				reserved				cmd_fre	cmd_clo	reserved	cmd_sud	cmd_st
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:28]	RW	cmd_icc	Port communication control signal. 0x0: No operation. It indicates that the next port status request is allowed. 0x1: Request to enable the port to be in the active status. 0x2: Request to enable the port to be in the partial status. 0x6: Request to enable the port to be in the slumber status. Other values: reserved When the software writes any of the preceding values rather than the reserved value, the controller clears the cmd_icc bit after performing related operations. When the software requests the current status of the port, the controller clears the cmd_icc bit directly. If the software requests the port status change from a low-power status to another low-power status, such as from the partial status to the slumber status, it needs to request the status change from the partial status to the active status, and then to the slumber status.
[27]	RW	cmd_asp	Slumber or partial status select for power management. 0: proactively enter the partial status. 1: proactively enter the slumber status.

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[26]	RW	cmd_alpe	Automatic power management enable. 0: disabled 1: enabled If SATA_PORT_CI and SATA_PORT_SACT are cleared, the controller enters the power-management status automatically. To be specific, if cmd_asp is 1, the controller enters the partial status; if cmd_asp is 0, the controller enters the slumber status.
[25]	RW	cmd_dlae	LED drive enable in ATAPI mode. 0: The LED pin can be driven when cmd_atapi is 0 and commands are being executed. 1: The LED pin can be driven when commands are being executed.
[24]	RW	cmd_atapi	ATAPI device indication. 0: The current device is not an ATAPI device. 1: The current device is an ATAPI device.
[23:22]	RO	reserved	Reserved.
[21]	RO	cmd_esp	Fixed at 1, indicating that the external SATA device is supported.
[20:18]	RO	reserved	Reserved.
[17]	RW	cmd_pma	Port multiplier detection indication. 0: No port multiplier is connected to the port. 1: A port multiplier is connected to the port.
[16]	RO	reserved	Reserved.
[15]	RO	cmd_cr	Command list processing indication. 0: No command is being executed. 1: A command is being executed.
[14]	RO	cmd_fr	FIS receive processing indication. 0: No FIS is being received. 1: An FIS is being received.
[13]	RO	reserved	Reserved.
[12:8]	RO	cmd_ccs	Slot number of the current command. This field is valid when cmd_st is 1 and is cleared when cmd_st is 0.
[7:5]	RO	reserved	Reserved.
[4]	RW	cmd_fre	FIS receive enable control. 0: forbid to write the received FISs to the system memory 1: enable the received FISs and write them to the system memory The software needs to set the receive FIS base address register SATA_PORT_FB before enabling this bit to receive FISs. When cmd_st is 1, this bit must be set to 1.

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[3]	RW	cmd_clo	BSY/DQR clear control. The software can forcibly clear the BSY and DRQ bits through this bit and transmit commands to the device. 0: no effect 1: Clear the BSY and DRQ bits of SATA_PORT_TFD[tfd_sts]. After the BSY and DRQ bits are 0, the cmd_clo bit is cleared automatically. The cmd_clo bit can be written as 1 only before the value of cmd_st is changed from 0 to 1. In addition, the software must write 1 to cmd_st after the cmd_clo bit is cleared.
[2]	RO	reserved	Reserved.
[1]	RW	cmd_sud	Spin-up device control. 0: When SATA_PORT_SCTL[det] is 0, the controller enters the listen mode. 1: After the system is powered on or the HBA is reset, the controller is enabled to transmit a COMRESET sequence to initialize the hardware device.
[0]	RW	cmd_st	Command list processing enable. 0: The controller enters the idle status. 1: The controller processes the commands from slot 0 that are identified as valid slots by SATA_PORT_CI. Note: The cmd_st bit can be set to 1 only after cmd_fre is 1.

SATA_PORT_TFD

SATA_PORT_TFD is a port task file register.

Offset Address	Register Name	Total Reset Value
0x20+nx0x80	SATA_PORT_TFD	0x0000_007F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tfd_err								tfd_sts							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:8]	RO	tfd_err	Task file error. The controller updates this field after receiving a D2H register FIS, a PIO setup FIS, or an SDB FIS.

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[7:0]	RO	tfd_sts	Task file status. bit[7]: BSY bit. It indicates that the device is busy. bit[6:4]: The meaning of this field varies according to commands. bit[3]: DRQ bit. It indicates that there is the data to be transferred in the device. bit[2:1]: The meaning of this field varies according to commands. bit[0]: ERR bit. It indicates that an error occurs during the data transfer. The controller updates this field after receiving a D2H register FIS, a PIO setup FIS, or an SDB FIS.

SATA_PORT_SIG

SATA_PORT_SIG is a port signature register.

Offset Address	Register Name	Total Reset Value
0x24+nx0x80	SATA_PORT_SIG	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	signature																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	signature	LBA address and sector addressing. The allocated addresses are as follows: bit[31:24]: LBA upper-bit address bit[23:16]: LBA middle-bit address bit[15:8]: LBA lower-bit address bit[7:0]: number of sectors The controller updates this register when receiving the first D2H register FIS after the hardware device is reset.

SATA_PORT_SSTS

SATA_PORT_SSTS is a port status register.

Offset Address	Register Name	Total Reset Value
0x028+nx0x80	SATA_PORT_SSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				pxssts_ipm				pxssts_spd				pxssts_det			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:8]	RO	pxssts_ipm	Current port status. 0x0: No devices exist or no communication is set up. 0x1: active 0x2: partial 0x6: slumber Other values: reserved
[7:4]	RO	pxssts_spd	Port negotiation speed. 0x0: No devices exist or no communication is set up. 0x1: Rate 1 is negotiated for communication. 0x2: Rate 2 is negotiated for communication. 0x3: Rate 3 is negotiated for communication. Other values: reserved
[3:0]	RO	pxssts_det	Device detection and PHY status. 0x0: No device is detected and no PHY communication is set up. 0x1: A device is detected but no PHY communication is set up. 0x3: A device is detected but the PHY communication is set up. 0x4: The PHY is offline or in the built-in self test (BIST) status. Other values: reserved

SATA_PORT_SCTL

SATA_PORT_SCTL is a port control register.

Offset Address	Register Name	Total Reset Value
0x02C+nx0x80	SATA_PORT_SCTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				pxsctl_ipm				pxsctl_spd				pxsctl_det			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.

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[11:8]	RW	pxsctl_ipm	Port power management status control. 0x0: no requirements 0x1: forbid to enter the partial status. 0x2: forbid to enter the slumber status 0x3: Forbid to enter the partial or slumber state. Other values: reserved
[7:4]	RW	pxsctl_spd	Port communication speed control. 0x0: no requirements 0x1: limit the communication speed to rate 1 0x2: limit the communication speed to rate 2 0x3: limit the communication speed to rate 3 Other values: reserved
[3:0]	RW	pxsctl_det	Device detection and port initialization control. 0x0: no device detection or initialization request 0x1: request the port to reset the initialization sequence COMRESET 0x4: force the port to be offline Other values: reserved When pxsctl_det is set to 1, the controller transmits the COMRESET sequence to the device. In this case, to ensure that the device receives the COMRESET sequence, the software must retain the value 1 of pxsctl_det for at least 1 ms.

SATA_PORT_SERR

SATA_PORT_SERR is an error diagnosis status register.

Offset Address	Register Name	Total Reset Value
0x30+nx0x80	SATA_PORT_SERR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					diag_x	diag_f	reserved	diag_s	diag_h	diag_c	reserved	diag_b	diag_w	diag_i	diag_n	reserved					err_p	reserved	err_t	reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26]	WC	diag_x	Device detection status. 0: No COMINIT signal transmitted from the device is detected. 1: A COMINIT signal transmitted from the device is detected.

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[25]	WC	diag_f	Detection status of the unknown FIS. 0: No unknown FIS is received. 1: An unknown FIS is received and this bit is set to 1 when the cyclic redundancy check (CRC) is correct.
[24]	RO	reserved	Reserved.
[23]	WC	diag_s	Link layer error status. 0: No status transition error occurs at the link layer. 1: A status transition error occurs at the link layer.
[22]	WC	diag_h	Handshake error status. 0: No R_ERR primitive transmitted from the device is received. 1: One or more R_ERR primitives transmitted from the device are received.
[21]	WC	diag_c	CRC error status. 0: No CRC error occurs during FIS receiving. 1: A CRC error occurs during FIS receiving.
[20]	RO	reserved	Reserved.
[19]	WC	diag_b	Decoding error status. 0: No 8B/10B decoding error is detected. 1: An 8B/10B decoding error is detected.
[18]	WC	diag_w	COMWAKE status. 0: No COMWAKE signal transmitted from the device is detected. 1: A COMWAKE signal transmitted from the device is detected.
[17]	WC	diag_i	PHY internal error status. 0: No PHY internal error is detected. 1: A PHY internal error is detected.
[16]	WC	diag_n	PhyRdy signal change status. 0: The PhyRdy signal is not changed. 1: The PhyRdy signal is changed. This bit is set to 1 when the value of the PhyRdy signal is changed from 1 to 0 or from 0 to 1.
[15:11]	RO	reserved	Reserved.
[10]	WC	err_p	SATA protocol incompliance error status. 0: No device behaviors do not comply with the SATA protocol. 1: Some device behaviors do not comply with the SATA protocol.
[9]	RO	reserved	Reserved.
[8]	WC	err_t	Data integrity error status. 0: No data integrity error is detected. 1: A data integrity error is detected.

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[7:0]	RO	reserved	Reserved.

SATA_PORT_SACT

SATA_PORT_SACT is an NCQ command identifier control register.

Offset Address	Register Name	Total Reset Value
0x034+nx0x80	SATA_PORT_SACT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	port_sact																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	port_sact	NCQ command identifier control. Each bit of this register maps to a tag ID and an NCQ command in the memory. To be specific, bit[31:0] map to the commands of slot 31 – 0 and tag 31 – 0 respectively. The following describes the meaning of each bit by taking bit[3] as an example: 0: The slot 3 command is a non-NCQ command. 1: The slot 3 command is an NCQ command. Before setting SATA_PORT_SACT bit[3] to 1, the software must clear SATA_PORT_CI bit[3]. After the command data transfer, the device transmits an SDB FIS. Then, the controller clears SATA_PORT_SACT bit[3] based on the SActive in the FIS. The software can set SATA_PORT_SACT only when cmd_st is 1. When cmd_st is 0, all bits of SATA_PORT_SACT are cleared.

SATA_PORT_CI

SATA_PORT_CI is a command transmit control register.

Offset Address	Register Name	Total Reset Value
0x38+nx0x80	SATA_PORT_CI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	port_ci																															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	port_ci	Control for the commands to be transmitted. Each bit of this register maps to a command in the memory. To be specific, bit[31:0] map to the commands of slot 31 – 0 respectively. The following describes the meaning of each bit by taking bit[3] as an example: 0: There is no slot 3 command to be transmitted and executed. 1: A slot 3 command is created in the memory. Then the controller can transmit this command. After running this command and receiving a corresponding FIS, the controller clears SATA_PORT_CI bit[3] and the BSY, DRQ, and ERR bits of SATA_PORT_TFD. The bits of SATA_PORT_CI can be set to 1 only when cmd_st is 1 and all bits of SATA_PORT_CI are cleared when cmd_st is 0.

SATA_PORT_SNTF

SATA_PORT_SNTF is an async notification event indication register.

Offset Address	Register Name	Total Reset Value
0x3C+nx0x80	SATA_PORT_SNTF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																pxsntf_pmn															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	WC	pxsntf_pmn	Async notification event status. If the controller receives an SDB FIS from the device on the PM port and the N bit of this FIS is 1, the controller sets the bit of this register corresponding to this port number to 1. The following describes the meaning of each bit by taking bit[3] as an example: 0: No async notification event occurs on the device whose PM port number is 3. 1: An async notification event occurs on the device whose PM port number is 3.

SATA_PORT_FIFOTH

SATA_PORT_FIFOTH is a receive FIFO threshold register.

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Offset Address	Register Name	Total Reset Value
0x044+nx0x80	SATA_PORT_FIFOTH	0x0000_0724

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								dmac_rxfifo_th				rxfifo_th_sel	link_rxfifo_th		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:9]	RW	reserved	Reserved.
[8:4]	RW	dmac_rxfifo_th	Flow control threshold of the DMAC receive FIFO. During data reception, if the data amount in the DMAC FIFO is above the threshold, the controller starts to control the data flow.
[3]	RW	rxfifo_th_sel	Flow control FIFO select. 0: The flow control for the link receive FIFO is valid. 1: The flow control for the DMAC receive FIFO is valid.
[2:0]	RW	link_rxfifo_th	Flow control threshold of the link receive FIFO. During data reception, if the data amount in the DMAC FIFO is above the threshold, the controller starts to control the data flow.

SATA_PORT_HBA

SATA_PORT_HBA is an HBA test status register.

Offset Address	Register Name	Total Reset Value
0x050+nx0x80	SATA_PORT_HBA	0x0100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				p_curr_st				reserved				ndr_curr_st				cfis_curr_st				reserved	pio_curr_st			reserved	pm_curr_st			reserved	err_curr_st		
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:24]	RO	p_curr_st	Current status of the HBA_PINIT_STATE state machine.
[23:21]	RO	reserved	Reserved.

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[20:16]	RO	ndr_curr_st	Current status of the HBA_NDR_STATE state machine.
[15:12]	RO	cfis_curr_st	Current status of the HBA_CFIS_STATE state machine.
[11]	RO	reserved	Reserved.
[10:8]	RO	pio_curr_st	Current status of the HBA_PIO_STATE state machine.
[7]	RO	reserved	Reserved.
[6:4]	RO	pm_curr_st	Current status of the HBA_PM_STATE state machine.
[3]	RO	reserved	Reserved.
[2:0]	RO	err_curr_st	Current status of the HBA_ERR_STATE state machine.

SATA_PORT_LINK

SATA_PORT_LINK is a link test status register.

Offset Address	Register Name	Total Reset Value
0x054+nx0x80	SATA_PORT_LINK	0x0020_2020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				link_curr_st				reserved	link_df_fifo_full	link_df_fifo_empty	link_df_fifo_count					reserved	link_rx_fifo_full	link_rx_fifo_empty	link_rx_fifo_count					reserved	link_tx_fifo_full	link_tx_fifo_empty	link_tx_fifo_count				
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:24]	RO	link_curr_st	Current status of the LINK_CTL_STATE state machine.
[23]	RO	reserved	Reserved.
[22]	RO	link_df_fifo_full	Full flag of the link frequency difference FIFO. 0: not full 1: full
[21]	RO	link_df_fifo_empty	Empty flag of the link frequency difference FIFO. 0: not empty 1: empty
[20:16]	RO	link_df_fifo_count	Data amount in the link frequency difference FIFO.
[15]	RO	reserved	Reserved.

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[14]	RO	link_rx_fifo_full	Full flag of the link receive FIFO. 0: not full 1: full
[13]	RO	link_rx_fifo_empty	Empty flag of the link receive FIFO. 0: not empty 1: empty
[12:8]	RO	link_rx_fifo_count	Data amount in the link receive FIFO.
[7]	RO	reserved	Reserved.
[6]	RO	link_tx_fifo_full	Full flag of the link transmit FIFO. 0: not full 1: full
[5]	RO	link_tx_fifo_empty	Empty flag of the link transmit FIFO. 0: not empty 1: empty
[4:0]	RO	link_tx_fifo_count	Data amount in the link transmit FIFO.

SATA_PORT_DMA1

SATA_PORT_DMA1 is DMAC test status register 1.

Offset Address	Register Name	Total Reset Value
0x058+nx0x80	SATA_PORT_DMA1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23	22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	txdmac_cur_state	txdmac_prd_i		tx_entry_dbc_cnt				
Reset	0 0 0 0	0 0 0 0	0	0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:24]	RO	txdmac_cur_state	Current status of the SATA_TX_DMAC state machine.
[23]	RO	txdmac_prd_i	I bit in the entry of the PRD linked list of SATA_TX_DAMC.
[22:0]	RO	tx_entry_dbc_cnt	Down counter in SATA_TX_DMAC. It indicates the number of data bytes in the current entry.

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SATA_PORT_DMA2

SATA_PORT_DMA2 is DMAC test status register 2.

Offset Address	Register Name	Total Reset Value
0x05C+nx0x80	SATA_PORT_DMA2	0x0020_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_data_fis_cnt																tx_cmdh_prdtl							
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:8]	RO	tx_data_fis_cnt	Down counter in SATA_TX_DMAC. It indicates the number of data FIS bytes during the operation of PIO, legacy DMA, or first party DMA. For the PIO operation, the initial value is equal to the value of transcount in the PIO setup FIS; for the legacy DMA or first party DMA operation, the initial value is 16'h2000 (2048 DWORD).
[7:0]	RO	tx_cmdh_prdtl	Down counter in SATA_TX_DMAC. The parameter in the command header indicates the number of entries in the PRDT.

SATA_PORT_DMA3

SATA_PORT_DMA3 is DMAC test status register 3.

Offset Address	Register Name	Total Reset Value
0x060+nx0x80	SATA_PORT_DMA3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_fpdma_tran_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	tx_fpdma_tran_cnt	Down counter in SATA_TX_DMAC. It indicates the number of data FIS bytes during the first party DMA operation.

SATA_PORT_DMA4

SATA_PORT_DMA4 is DMAC test status register 4.

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Offset Address	Register Name	Total Reset Value
0x064+nx0x80	SATA_PORT_DMA4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				rxdmac_cur_state				rxdmac_prd_i	rx_entry_dbc_cnt																						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:24]	RO	rxdmac_cur_state	Current status of the SATA_RX_DMAC state machine.
[23]	RO	rxdmac_prd_i	I bit in the entry of the PRD linked list of SATA_RX_DAMC.
[22:0]	RO	rx_entry_dbc_cnt	Down counter in SATA_RX_DMAC. It indicates the number of data bytes in the current entry.

SATA_PORT_DMA5

SATA_PORT_DMA5 is DMAC test status register 5.

Offset Address	Register Name	Total Reset Value
0x068+nx0x80	SATA_PORT_DMA5	0x0020_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_data_fis_cnt																rx_cmdh_prdtl							
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:8]	RO	rx_data_fis_cnt	Down counter in SATA_RX_DMAC. It indicates the number of data FIS bytes during the operation of PIO, legacy DMA, or first party DMA. For the PIO operation, the initial value is equal to the value of transcount in the PIO setup FIS; for the legacy DMA or first party DMA operation, the initial value is 0x2000 (2048 DWORD).
[7:0]	RO	rx_cmdh_prdtl	Down counter in SATA_RX_DMAC. The parameter in the command header indicates the number of entries in the PRDT.

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SATA_PORT_DMA6

SATA_PORT_DMA6 is DMAC test status register 6.

Offset Address	Register Name	Total Reset Value
0x6C+nx0x80	SATA_PORT_DMA6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_fpdma_tran_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rx_fpdma_tran_cnt	Down counter in SATA_RX_DMAC. It indicates the number of data FIS bytes during the first party DMA operation. The initial value is equal to the value of transcount in the DMA setup FIS.

SATA_PORT_DMA7

SATA_PORT_DMA7 is DMAC test status register 7.

Offset Address	Register Name	Total Reset Value
0x070+nx0x80	SATA_PORT_DMA7	0x0005_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										pio_op	fpdma_op	dmac_rx_fifo_full	dmac_rx_fifo_empty	dmac_tx_fifo_full	dmac_tx_fifo_empty	dmac_rx_fifo_cnt								dmac_tx_fifo_cnt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RO	pio_op	PIO operation indication. 0: The current command is not used for the PIO operation. 1: The current command is used for the PIO operation.
[20]	RO	fpdma_op	First party DMA operation indication. 0: The current command is not used for the first party DMA operation. 1: The current command is used for the first party DMA operation.

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[19]	RO	dmac_rx_fifo_full	Full status of SATA_DMAC_RX_FIFO. 0: not full 1: full
[18]	RO	dmac_rx_fifo_empty	Empty status of SATA_DMAC_RX_FIFO. 0: not empty 1: empty
[17]	RO	dmac_tx_fifo_full	Full status of SATA_DMAC_TX_FIFO. 0: not full 1: full
[16]	RO	dmac_tx_fifo_empty	Empty status of SATA_DMAC_TX_FIFO. 0: not empty 1: empty
[15:8]	RO	dmac_rx_fifo_cnt	Number of data segments in SATA_DMAC_RX_FIFO (in DWORD).
[7:0]	RO	dmac_tx_fifo_cnt	Number of data segments in SATA_DMAC_TX_FIFO (in DWORD).

SATA_PORT_PHYCTL

SATA_PORT_PHYCTL is a PHY control register.

Offset Address	Register Name	Total Reset Value
0x074+nx0x80	SATA_PORT_PHYCTL	0x0E63_6159

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			phy_disable	phy_calibrated	spd_change_ack	dp_rdy	bist_tx_fspd	neg_mode_b	gen2_en	los_ctl		rx_dpll_mode				rx_eq_val				rx_term_en	tx_calc	tx_edgerate		tx_cko_en	rx_align_en	tx_clk_align	tx_atten				tx_boost
Reset	0	0	0	0	1	1	1	0	0	1	1	0	0	0	1	1	0	1	1	0	0	0	0	1	0	1	0	1	1	0	0	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28]	RW	phy_disable	Whether to use the PHY. 0: used 1: not used
[27]	RW	phy_calibrated	Whether to calibrate the PHY. 0: not calibrated 1: calibrated

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[26]	RW	spd_change_ack	Whether the rate is allowed to switch. 0: not allowed 1: allowed
[25]	RW	dp_rdy	Whether the PHY is ready to transmit data. 0: not ready 1: ready
[24]	RW	bist_tx_fspd	Whether the clock frequency is forced to transmit in BIST mode. 0: not forced 1: forced
[23]	RW	neg_mode_b	Negotiation mode B select. 0: not supported 1: supported
[22]	RW	gen2_en	Transmit control signal. It indicates whether to support the 3G mode. 0: not supported 1: supported
[21:20]	RW	los_ctl	LOS detection control. 00: The LOS detection is disabled. 01: reserved 10: The OOB signal is being detected. 11: reserved
[19:17]	RW	rx_dpll_mode	Control mode of the receive DPLL. 000: indicates PHUG is 1 and FRUG is 1. 010: indicates PHUG is 2 and FRUG is 2. 010: indicates PHUG is 1 and FRUG is 4. 011: indicates PHUG is 2 and FRUG is 4. Other values: reserved
[16:14]	RW	rx_eq_val	Receive equalization control. The internal balancing value is ~ (rx_eq_val + 1) x 0.5 dB.
[13]	RW	rx_term_en	Receive termination enable. 0: disabled 1: enabled
[12]	RW	tx_calc	Reserved, fixed at 0.
[11:10]	RW	tx_edgerate	Edge control for the transmitted signal. The default value is 0x0.
[9]	RW	tx_cko_en	tx_cko_clk clock enable. 0: disabled 1: enabled

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[8]	RW	rx_align_en	Received data alignment. 0: not supported 1: supported
[7]	RW	tx_clk_align	Transmit clock alignment. 0: do not align 1: align
[6:4]	RW	tx_atten	Transmit attenuation control. 000: 16/16 001: 14/16 010: 12/16 011: 10/16 100: 9/16 101: 8/16 11X: reserved
[3:0]	RW	tx_boost	Transmit boost control. The value is －20 log [1 － (tx_boost[3:0] + 0.5)/32] dB.

SATA_PORT_PHYSTS

SATA_PORT_PHYSTS is a PHY test status register.

Offset Address	Register Name	Total Reset Value
0x078+nx0x80	SATA_PORT_PHYSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													tx_cko_word	tx_rxpres	tx_done	spd_change	link_rdy	init_compl	pwr_state	rx_pll_pwron	rx_en	tx_en			mpll_pwron	phy_comwake	phy_cominit	half_rate	phyrdy	los	op_done
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved.
[18]	RW	tx_cko_word	Indicates the word receive clock of each lane, reserved currently.
[17]	RW	tx_rxpres	Indicates the receive detection, reserved currently.
[16]	RW	tx_done	Indicates that the operation of transmitting part of requests is complete, active high and reserved currently.
[15]	RW	spd_change	Indicates the rate change, active high.
[14]	RW	link_rdy	Indicates that sufficient D10.2 is transmitted in high level.

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[13]	RW	init_compl	Indicates that non-align primitive is received in high level and initialization is complete.
[12]	RW	pwr_state	Indicates the low-power mode (partial or slumber status) when the bit is 1; indicates the active status in other cases.
[11]	RW	rx_pll_pwron	Indicates the power-on control signal of the received PLL.
[10]	RW	rx_en	Indicates the control status of the rx_en signal.
[9:7]	RW	tx_en	Indicates the control status of the tx_en signal.
[6]	RW	mpll_pwron	Indicates the power-on control signal of the MPLL.
[5]	RW	phy_comwake	Indicates that the PHY detects the COMWAKE signal, active high.
[4]	RW	phy_cominit	Indicates that the PHY detects the COMINIT signal, active high.
[3]	RW	half_rate	Indicates the rate of 1.5 Gbit/s when the bit is 1.
[2]	RW	phyrdy	Indicates that the PHY is initialized and then the PHY can communicate with the link layer, active high.
[1]	RW	los	Indicates the loss of signal output, active high.
[0]	RW	op_done	Indicates that the operations requested by the MPLL are complete, active high.

14.8.8 Appendix A Format of the SATA Command Linked List

Figure 14-60 shows the structure of the FIS linked list. The linked list refers to spaces that are created in the system memory by the software. The base address of the linked list is stored in the PxFB and PxFBU registers in the AHCI register group. The DMAC uses this base address as its destination address and transfer the received frames to different memory spaces.

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Figure 14-60 Structure of the linked list

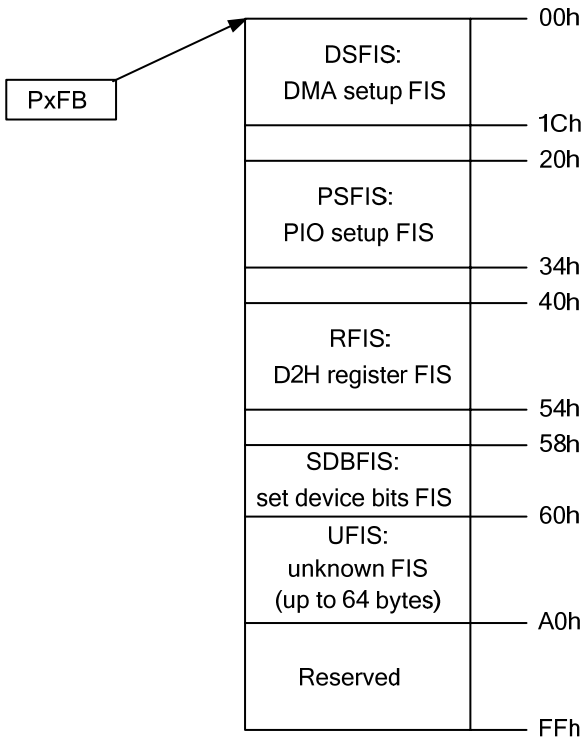

Figure 14-61 shows the structures of a command list and a data list. Such lists refer to the areas that are created in the system memory by the software. A command list contains a maximum of 32 commands and its base address is specified by the PxCLB and PxCLBU registers in the AHCI register group. Each command has a command header in which the CTBA0 part specifies the base address of the command table. The command table contains the commands to be read and the data space linked list to be read and written.

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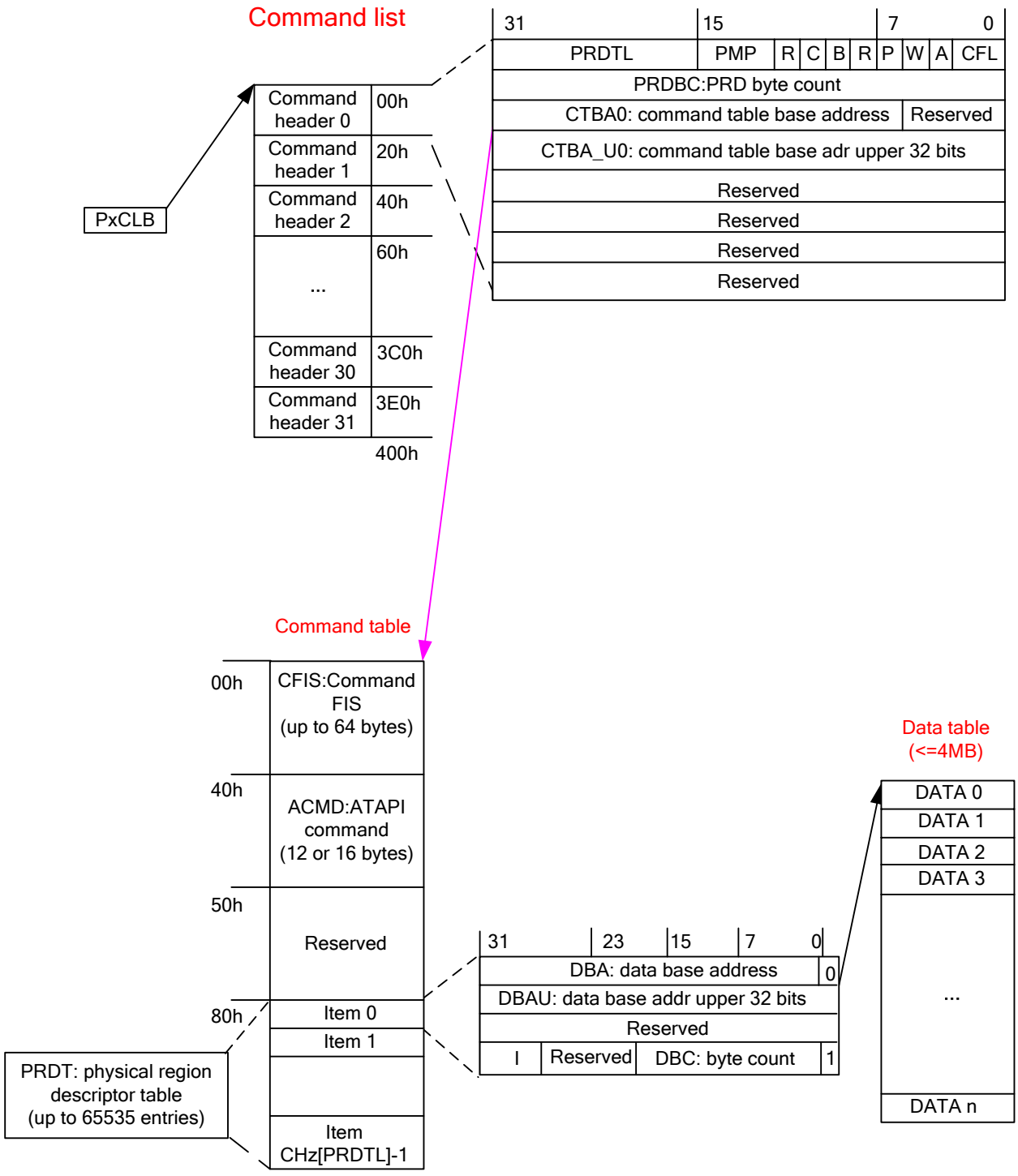
Figure 14-61 Structures of the command list and data list



Each time before a command is executed; the preceding two lists must be created in the memory. For details about the meaning of the lists, see the AHCI1.2 protocol. The CFIS area is used to store the H2D register FISs. For details, see the SATA2.5 protocol. The ACMD area is used to store the commands related to the ATAPI operation. For details, see the protocols about the DVD devices and CD-ROMs provided by the Small Form Factor (SSF) Committee.

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Contents

A Ordering Information A-1

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A Ordering Information

Figure A-1 shows the Hi3521 mark, and Figure A-2 shows the Hi3520A mark.

Figure A-1 Hi3521 mark

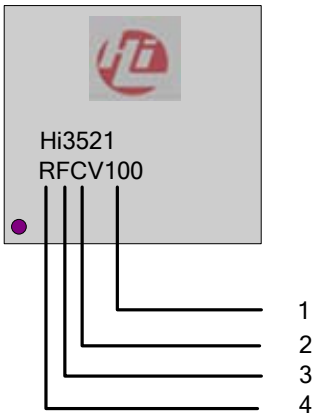

Figure A-2 Hi3520A mark

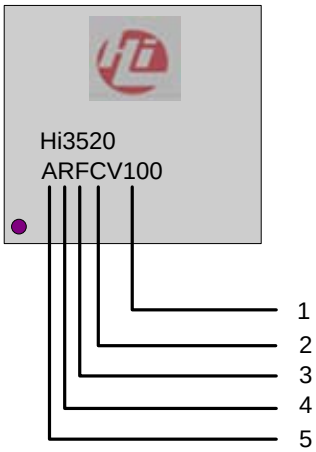

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Table A-1 describes the Hi3521 and Hi3520A marks.

Table A-1 Meaning of Hi3521 and Hi3520A marks

No.	Item	Description
1	Version number	It indicates the chip version number.
2	Temperature flag	The letter C stands for commercial. It indicates that the chip is for commercial use.
3	Package flag	The letter F stands for flip-chip ball grid array (FC-BGA).
4	Environmental protection flag	The letter R stands for restriction of the use of certain hazardous substances (RoHS).
5	Product differentiation flag (only for the Hi3520A)	It is the last character of a chip name for differentiating one chip from another one.

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